Using the CodeTEST Probe with Freescale™ MPC8260 and MPC8255 Processors

This document describes the requirements for connecting the CodeTEST Probe to the local bus of the MPC8260 and MPC8255 processors

Purpose

This document supplements the *Setup and Installation Guide for the CodeTEST Probe*, which provides generic information on setting up, connecting, and configuring the CodeTEST Probe, and describes CodeTEST address and data port requirements, and bus and timing requirements.

Use the information in this document to make the physical connection between the CodeTEST Probe and local bus of the MPC8260 and MPC8255 processors and to configure the Probe with the CodeTEST Manager.

For help on connecting the CodeTEST unit to the 60X bus of the MPC8260 and MPC8255, see the PPC6xx application note.

Hardware Connections

The CodeTEST Probe supports targets with bus clocks up to 100 MHz with no wait states and 100-133 MHz with one wait state.

The Probe supports 16- and 32-bit port sizes. You will need to identify data and address tag ports to be used for data transfers to the Probe.

The following connections are required:

Probe	Processor	Notes
A31:18	NC	Address bits not available externally.
A17:0	LA14:31	Note the bit-wise inversion of the bus.
D31:0	LD0:31	Note the bit-wise inversion of the bus.
X15:0	NC	
C0	VCC	VCC – not required
C1	CLKIN	CLK
C2	NC	DS
C3	CSx*	AS - Connect to the chip select for the memory region in which the tag-ports are located.
C4	HRESET*	RST2
C5	SRESET*	RST1
C6	NC	CYC

CodeTEST Development Team

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Probe	Processor	Notes
C7	LWR*	WS

Probe Configuration

This section identifies the settings you should use in the **Probe Config Utility** in the CodeTEST Manager when you configure the Probe.

Use the Universal Probe type and select the following settings:

Field	Setting	Notes
Port Address		Enter address of the Probe tag port.
Port Address Mask	0xFFFc0000	
Extended Bus	0x0	
Extended Bus Mask	0xFFFF	
Bus Type	Non-multiplexed	
Port Size		Select appropriately for target hardware.
Reset Configuration	Both	
Strobe Configuration	1 Strobe	
Address Strobe Polarity	Low	
Write Strobe Polarity	Low	
Bus Arbitration Polarity	Disabled	
Endianess	Big	
Word Swap	No	
Frequency Range		Set to the frequency range of the clock being monitored.
Phase Shift	0	Adjust as necessary to obtain accurate data.
Invert Clock	No	
Routing Image		Select appropriate routing image.

Note: If there is an unused chip select pin on the target, you can program a dedicated chip select for the CodeTEST Probe. To do this, program base register BRx with (`ct_port | 0x1821`), and the option register with `0xFFFF8000`. This will set aside an 8K x 32-bit memory region for the Probe. If you are using the memory management unit, you will need to ensure this memory region is correctly mapped.

Limitations

Processors with bus frequencies over 100 MHz must use the Mictor-38 connection method and have at least two clock cycles per bus cycle.

The Probe does not support the following memory activities:

- Pipelined accesses: Multiple or overlapping address cycles in relation to the data portion of a bus cycle.
- Burst accesses: The tag ports must be located in a non-burst memory region.
- Misaligned accesses: The tag ports must be on 64-bit aligned memory locations.
- Cache: The tag ports must be located in non-cached or cached write-through memory.
- DRAM: The tag ports cannot be located in DRAM on processors with built-in DRAM controllers.
- 8-bit ports: 8-bit ports are not correctly reconstructed into 32-bit tags.