NXP Semiconductors
Application Note

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i.MX 6ULL Migration Guide

Migrating from i.MX 6UL to i.MX 6ULL

1. Introduction

1.1. Purpose

This application note provides an introduction to the i.MX 6ULL architecture by highlighting the differences from the i.MX 6 series processor upon which it is based (namely the i.MX 6UL). This document is a migration guide for developers that migrate from the i.MX 6UL to the i.MX 6ULL.

Contents

1.2. Scope

The i.MX 6ULL was developed with an extensive reuse of the existing NXP designs, including:

- Extensive reuse and alignment of the i.MX 6UL
- Modules reused/modified from the i.MX 6UL

Due to a close alignment to the i.MX 6UL design, this document is structured as a summary of changes to the i.MX 6UL features. It provides references to modules that are reused or modified on the i.MX 6ULL.

The i.MX 6ULL architecture introduces new features which are different from the i.MX 6UL. The key differences include:

- The EPD display support with the EPDC/PXP for the low-end eReader market is added. It is less powerful when compared to the i.MX 6SL or i.MX 7D, but it also has a lower cost and a lower power consumption.
- The advanced security features that are mainly used by the POS applications (including CAAM/BEE/DryICE) are removed. The basic security (such as the HAB) is still supported.
- The ESAI with a multi-channel audio input/output is added to provide a better support for audio applications.
- The power consumption is optimized.
- The EMV SIM module is removed.

1.3. Audience

This document is intended for system integrators and software developers migrating from the platforms based on the i.MX 6ULL.

2. Feature Change Summary

2.1. BSP support

The i.MX 6ULL is supported by the Linux_4.1.15-2.0.0_GA BSP release.

2.2. Module change list

This section summarizes the architectural changes of the i.MX 6ULL with respect to the i.MX 6UL.

Table 1. Architectural changes

Category	Feature	Change from i.MX 6UL	Board impact	Software impact
ARM® Cortex®-A7 core platform	Cortex-A7 core	Updated	None	None
Audio	ESAI	New	None (the SAI interface is still provided on the 6ULL-EVK).	None
General connectivity interfaces	EMV	Removed	The EMV driver is removed.	None
Memory/busses	NIC301	Updated	None	None
	AIPS-3	New	None	None
SNVS MIX	SNVS_LP	Updated	None	None
	IOMUXC_SNVS	New	None	None
	SNVS_GPR	New	None	None
MIX repartitioning	MEGAMIX	Updated	None	None
	SNVSMIX	Updated	None	None
PINMUX	CAAM	Removed	The CAAM PINMUX is removed.	The CAAM PINMUX config code is removed.
	EPDC and ESAI	New	The PINMUX option for the EPDC display interface and the ESAI interface is added.	The EPDC PINMUX config code is added.
Power	Power consumption	Optimized	- The power consumption for the low-power modes is optimized. Some of the IP modules are moved from the wakeupmix to the megamix. - The Vmin = 0.9 V DVFS set point for both the SOC and the ARM in the run mode is supported to achieve lower power at a low-frequency operation.	The maximum ARM frequency is adjusted in the DVFS driver based on the latest datasheet.
	Internal LDO	Updated	The VDD_SOC_CAP and VDD_ARM_CAP can be up to 1.3 V only in the commercial grade and up to 1.26 V in the industrial grade.	None
Security	CAAM	Removed	None	The CAAM support code is removed.
	BEE	Removed	None	The BEE support code is removed.
	RNGB	New	None	The RNGB support code is added.
	DCP	New	None	The DCP support code is added.
	OCOTP_CTRL	Updated	None	The fuse box size is reduced from 4 KB to 2 KB.
Display	PXP	Updated	The PXP is updated to support EPD displays.	The “repeat” feature is removed and the EPD processing support is added.
	EPDC	New	The EDPC IP is added to support E-Ink displays.	The EPDC driver is added.

2.3. EPDC and ESAI PINMUX

When designing hardware boards, consider the EPDC and ESAI changes to the PINMUX for the i.MX 6ULL with respect to the i.MX 6UL. The EPDC multiplexes the LCD/ENET/UART pins and the ESAI multiplexes the CSI pins.

The detailed EPDC PINMUX is shown in this table:

Table 2. EPDC PINMUX

Pin name	Alt9
UART4_RXD	epdc.PWRCTRL[1]
UART5_TXD	epdc.PWRCTRL[2]
UART5_RXD	epdc.PWRCTRL[3]
ENET1_RXD0	epdc.SDCE[4]
ENET1_RXD1	epdc.SDCE[5]
ENET1_CDS_DV	epdc.SDCE[6]
ENET1_TXD0	epdc.SDCE[7]
ENET1_TXD1	epdc.SDCE[8]
ENET1_TXEN	epdc.SDCE[9]
ENET1_TXCLK	epdc.SDOED
ENET1_RXER	epdc.SDOEZ
ENET2_RXD0	epdc.SDDO[8]
ENET2_RXD1	epdc.SDDO[9]
ENET2_CRS_DV	epdc.SDDO[10]
ENET2_TXD0	epdc.SDDO[11]
ENET2_TXD1	epdc.SDDO[12]
ENET2_TXEN	epdc.SDDO[13]
ENET2_TXCLK	epdc.SDDO[14]
ENET2_RXER	epdc.SDDO[15]
LCD_CLK	epdc.SDCLK
LCD_ENABLE	epdc.SDLE
LCD_HSYNC	epdc.SDOE
LCD_VSYNC	epdc.SDCE[0]
LCD_RESET	epdc.GDOE
LCD_DATA00	epdc.SDDO[0]
LCD_DATA01	epdc.SDDO[1]
LCD_DATA02	epdc.SDDO[2]
LCD_DATA03	epdc.SDDO[3]
LCD_DATA04	epdc.SDDO[4]
LCD_DATA05	epdc.SDDO[5]
LCD_DATA06	epdc.SDDO[6]
LCD_DATA07	epdc.SDDO[7]
LCD_DATA08	epdc.PWRIRQ
LCD_DATA09	epdc.PWRWAKE
LCD_DATA10	epdc.PWRCOM
LCD_DATA11	epdc.PWRSTAT
LCD_DATA12	epdc.PWRCTRL[0]
LCD_DATA13	epdc.BDR[0]
LCD_DATA14	epdc.SDSHR
LCD_DATA15	epdc.GDRL
LCD_DATA16	epdc.GDCLK
LCD_DATA17	epdc.GDSP
LCD_DATA18	epdc.BDR[1]
LCD_DATA19	epdc.VCOM[0]
LCD_DATA20	epdc.VCOM[1]

Table 2. EPDC PINMUX

Pin name	Alt9
LCD_DATA21	epdc.SDCE[1]
LCD_DATA22	epdc.SDCE[2]
LCD_DATA23	epdc.SDCE[3]

The detailed ESAI PINMUX is shown in this table:

Table 3. ESAI PINMUX

Pin name	Alt9
CSI_MCLK	esai.TX3_RX2
CSI_PIXCLK	esai.TX2_RX3
CSI_VSYNC	esai.TX4_RX1
CSI_HSYNC	esai.TX1
CSI_DATA00	esai.TX_HF_CLK
CSI_DATA01	esai.RX_HF_CLK
CSI_DATA02	esai.RX_FS
CSI_DATA03	esai.RX_CLK
CSI_DATA04	esai.TX_FS
CSI_DATA05	esai.TX_CLK
CSI_DATA06	esai.TX5_RX0
CSI_DATA07	esai.TX0

The EPDC connector is only for the NXP DC-4 board, whose part number is X-IMXEBOOKDC4. If using the SD1 to boot up, it is not needed to connect the EPDC_PWRSTAT signal to the EPDC connector. The detailed connector design is shown in this figure:

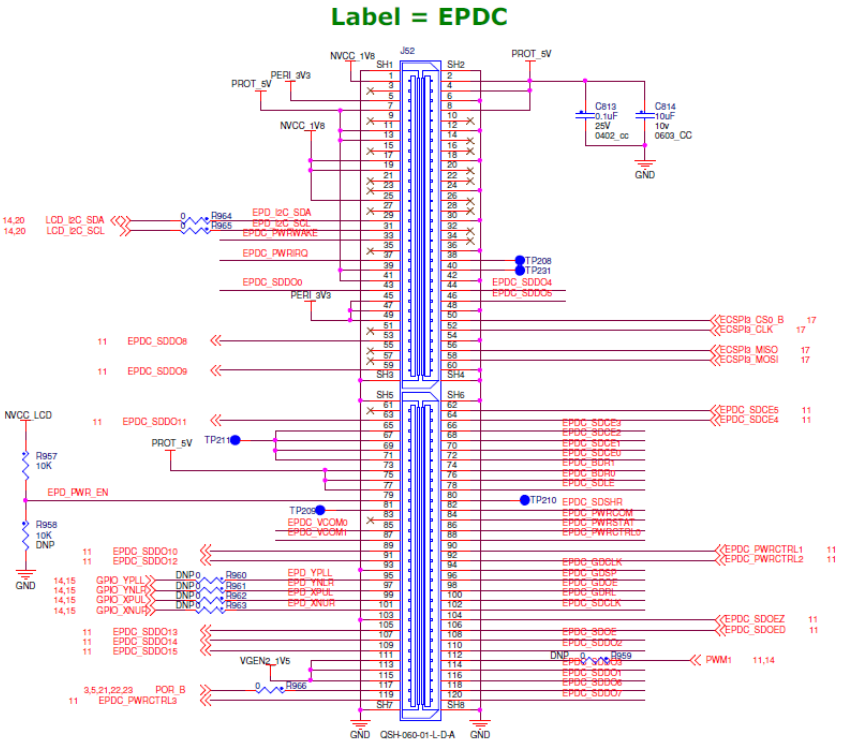

Figure 1. Connector design

3. Revision History

This table summarizes the changes done to this document since the initial release:

Revision number	Date	Sunstantive changes
0	10/2016	Initial release

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