Average Current Mode Interleaved PFC Control

Theory of operation and the Control Loops design

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1. Introduction

Power Factor Correction (PFC) systems are used for AC/DC conversion to compensate the power factor. There are many topologies and control techniques incorporated in the PFC systems. The boost converter is the most popular topology due to a simple control of the input current while keeping the output voltage constant. For medium power levels, the 1-phase PFC operating in the average current-control mode is the optional solution. Increasing the output power and looking for improvement of the overall efficiency leads to the use of several converters in a parallel connection. In the presented solution, there are two boost converters connected in parallel, feeding one DC-bus circuit. The converters are shifted by 180° to one another to reduce the input current ripple. This topology is also called interleaved PFC.

The interleaved boost PFC converter has several advantages over the single boost converter, such as increased power density, reduced EMI filter due to a smaller input current ripple, reduced capacitor RMS current, and increased overall efficiency. This application note describes the average current mode interleaved PFC operation, the control theory, and the Control Loops design based on a small-signal system model.

Contents

2. Interleaved PFC Basics

The interleaved PFC consists of two boost converters connected in parallel. The benefit of this approach is a reduced input current ripple, because the inductor currents I_{L1} and I_{L2} are shifted by 180° to one another (see Figure 1). Figure 1 also shows that when the converter is operating at 50 % of its duty cycle, the input current ripple is zeroed. The interleaved operation also decreases the output capacitor current ripple. These features optimize the components of the design. When compared to the single boost converter, the PFC inductors handle half the current, and the DC-bus capacitor, MOSFETs, and diodes are calculated for half the current ripple. All these advantages lead to a higher power density per watt. Furthermore, you can increase the efficiency by disabling one leg of operation at lower power.
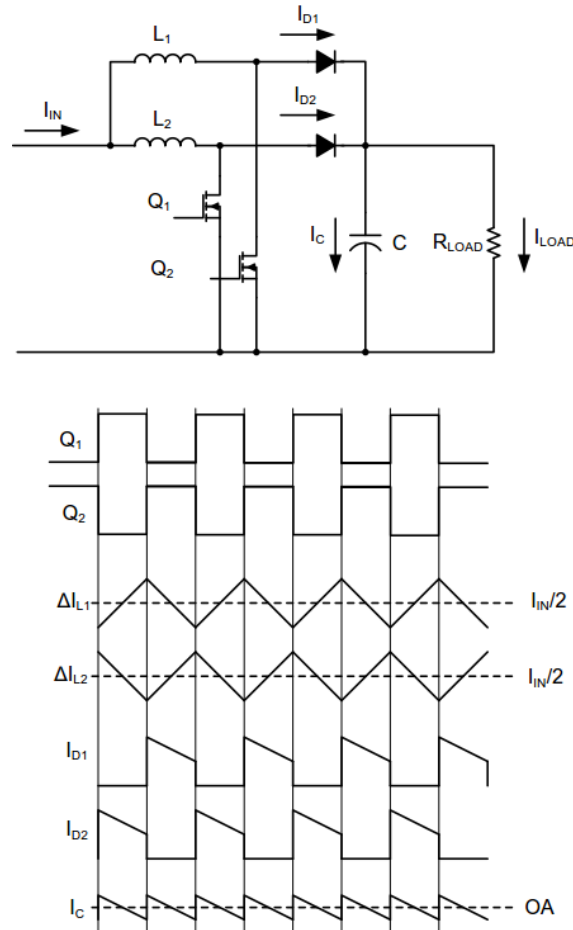

Figure 1. PFC control structure

On the other hand, the software control structure of the interleaved PFC is more complicated (see the following figure).
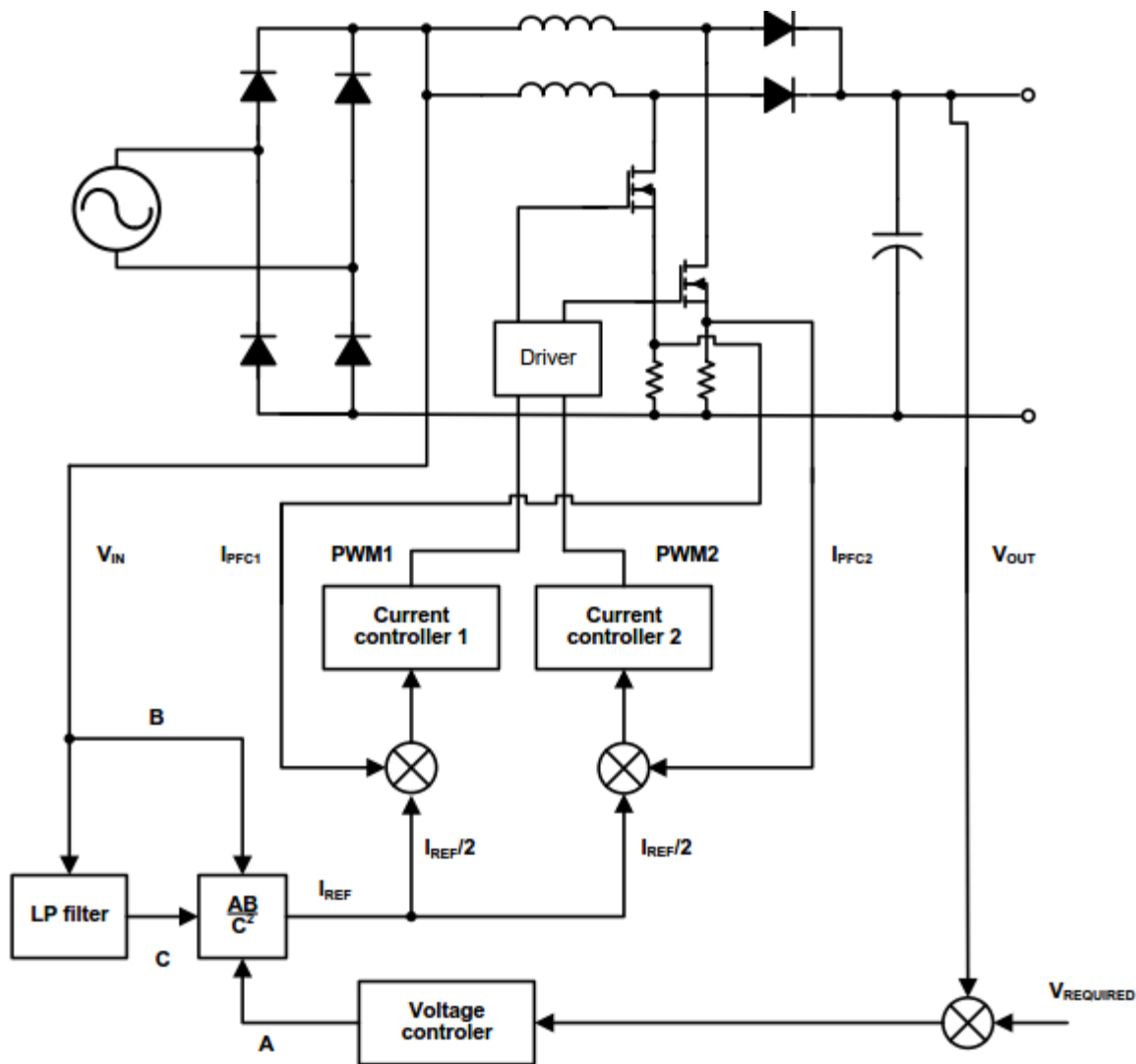
Figure 2. Control structure

In the 2-phase interleaved PFC application, sense these four quantities: the input voltage V_{in}, two boost currents I_{pfc1} and I_{pfc2}, and the output voltage V_{out}. The control structure consists of two current-control loops, one voltage loop, the input voltage feed-forward block, and the phase management logic. In the outer control loop, compare the actual DC-bus voltage to the desired one. The control error is processed by the PI (proportional-integral) controller, which generates the amplitude of the reference current. The required amplitude is multiplied (A) by the reference sinewave (B), which is derived from the shape of the input voltage. When both converter phases run in parallel, the current reference for each phase is half of the voltage controller output. When deriving the sinewave reference from the input voltage, add the voltage feed-forward block (C) to eliminate the input voltage variation. This block consists of a low-pass filter, which calculates the average value of the input voltage. For a sinusoidal shape, the average value is recalculated to the RMS value, and it is used for compensation.

Compare the current reference to the actual currents sensed on the shunt resistors. The current difference is processed by the PI controllers. The outputs from these controllers are the duty cycles of the PWM

signals for the PFC MOSFET transistors. Shift the PWM signal for the second transistor to the PWM signal of the first leg by 180°.

Control the input current to achieve the desired input-current shape and the desired level of DC output voltage on the DC-bus capacitors. The inner current-control loop must be fast enough to track the current changes. The maximum bandwidth of the current controller is limited by the controller's performance. The outer voltage loop keeps the output voltage at the required level. The MCU load required for the voltage-control loop is low. Set the bandwidth of the voltage-control loop below 20 Hz to eliminate the second harmonic of the DC-bus voltage.

3. Control Loops Design

The PFC Control Loops design consists of the inner current loop, the outer output-voltage loop, and the voltage feed-forward block design. The design includes a derivation of the small-signal models for the inner and outer control loops, the design of constants for the PI controllers, and the design of a second-order filter for the voltage feed-forward block.

This application note uses the so-called "analog approach" for the Control Loops design, where the whole design is made in the continuous-time domain. Finally, the controller parameters are scaled into the discrete domain to be used by the discretized controllers.

3.1. Current-control loop design

3.1.1. Boost converter small-signal model

The design of the inner current-control loop starts with the derivation of the transfer function of the inner current loop circuit. The inner current loop is represented by the boost converter, as shown in the following figure. Using the averaging method over the switching cycle followed by a small-signal perturbation, the nonlinear circuit shown in the following figure can be simplified into the small-signal model that describes the operation of the converter around the steady-state operation point. The resulting transfer function is used as a model of the boost converter for the design of the inner current-control loop.
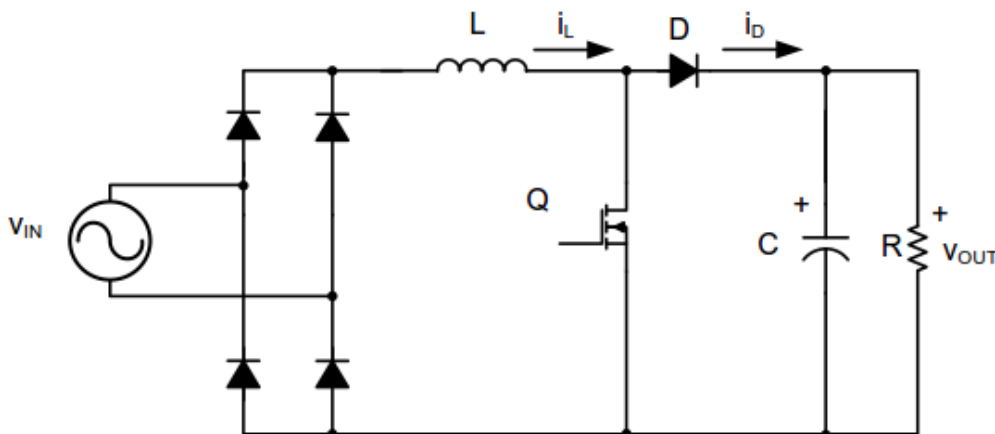

Figure 3. Boost converter schematic

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The averaging over the switching period is based on the fact that the current change in an inductor or the voltage change in a capacitor is zero over the switching period in the steady state. Therefore, the equations for the inductor current i_L and the capacitor voltage v_{OUT} can be written for both the ON and the OFF states of the MOSFET transistor. The subsequent summation of equations for the ON and OFF states gives these equations for the inductor current i_L and the capacitor voltage v_{OUT}:

Eq. 1
$$L\frac{di_L}{dt} = v_{IN} - (1-d) \cdot v_{OUT}$$

Eq. 2
$$C\frac{dv_{OUT}}{dt} = (1-d) \cdot i_L - \frac{v_{OUT}}{R}$$

Assuming that all variables (i_L, v_{IN}, v_{OUT}, and d) consist of steady-state values in the selected operational point (I_L, V_{IN}, V_{OUT}, V_C, and D) and small-signal AC variation ($\hat{i}_L$, $\hat{v}_{IN}$, and $\hat{v}_{OUT}$), Eq. 1 and Eq. 2 can be rewritten into this form:

Eq. 3
$$i_L = I_L + \hat{i}_L; v_{IN} = V_{IN} + \hat{v}_{IN}; v_{OUT} = V_{OUT} + \hat{v}_{OUT}; d = D + \hat{d}$$

Eq. 4
$$L\frac{d(I_L + \hat{i}_L)}{dt} = (V_{IN} + \hat{v}_{IN}) - (1 - D - \hat{d}) \cdot (V_{OUT} + \hat{v}_{OUT})$$

Eq. 5
$$C\frac{d(V_{OUT} + \hat{v}_{OUT})}{dt} = (1 - D - \hat{d}) \cdot (I_L + \hat{i}_L) - \frac{(V_{OUT} + \hat{v}_{OUT})}{R}$$

Considering that the product of two small AC signals results in an even smaller signal, these small AC signal products are eliminated, and Eq. 4 and Eq. 5 can be rewritten as Eq. 6 and Eq. 7.

Eq. 6
$$L\frac{d\hat{i}_L}{dt} = \hat{v}_{IN} - (1-D) \cdot \hat{v}_{OUT} + V_{OUT} \cdot \hat{d}$$

Eq. 7
$$C\frac{d\hat{v}_{OUT}}{dt} = (1-D) \cdot \hat{i}_L - I_L \cdot \hat{d} - \frac{\hat{v}_{OUT}}{R}$$

Rearranging the equations using Laplace transformation leads to the small-signal model equations Eq. 8 and Eq. 9, and the matrix in Eq. 10.

Eq. 8
$$sL \cdot \hat{i}_L(s) = \hat{v}_{IN}(s) - (1-D) \cdot \hat{v}_{OUT}(s) + V_{OUT} \cdot \hat{d}(s)$$

Eq. 9
$$\left(sC + \frac{1}{R}\right)\hat{v}_{OUT}(s) = (1-D) \cdot \hat{i}_L(s) - I_L \cdot \hat{d}(s)$$

Eq. 10
$$\begin{bmatrix} sL & 1-D \\ 1-D & -\left(sC + \frac{1}{R}\right) \end{bmatrix} \cdot \begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_{OUT}(s) \end{bmatrix} = \begin{bmatrix} V_{OUT} \\ I_L \end{bmatrix} \cdot \hat{d}(s) + \begin{bmatrix} 1 \\ 0 \end{bmatrix} \cdot \hat{v}_{IN}(s)$$

The control to the input-current transfer functions is obtained as:

$$\text{Eq. 11} \qquad G_{id}(s) = \frac{sCV_{OUT} + 2(1-D)I_L}{(1-D)^2 + \dfrac{sL}{R} + s^2LC}$$

This transfer function can be further simplified using the high-frequency approximation, in which the capacitor is replaced by a shortcut for high frequencies, and the transfer function in Eq. 11 is simplified as:

$$\text{Eq. 12} \qquad G_{id}(s) \approx \frac{V_{OUT}}{sL}$$

3.1.2. Inner current loop controller design

This application note uses the so-called "analog approach" to design the digital control loop. This method is based on a design in a continuous-time domain. This method is adopted by analog engineers, but it has some drawbacks when used to design a digital control loop. The digital implementation of a control loop introduces transport delay, which is not reflected in the analog design approach. It results in a control loop that has worse performance than expected. However, this issue is eliminated by considering this delay during the analog design of the control loop. The digital implementation introduces two significant delays. The first delay relates to the sampling and processing time. The second delay relates to a digital implementation of the PWM modulator. The total transport delay is approximated by a first-order Pade polynomial:

$$\text{Eq. 13} \qquad G_{TD}(s) = \frac{1 - \dfrac{sT_D}{2}}{1 + \dfrac{sT_D}{2}}$$

This equation shows an example of a total delay calculation, where the inductor current is sampled in the middle of the PWM period, and a center-aligned PWM is used:

$$\text{Eq. 14} \qquad T_D = \frac{T_{PWM}}{2} + \frac{T_{PWM}}{2} = T_{PWM}$$

The controller used for the control loops compensation is a well-known PI controller described by Eq. 15. The PI controller is implemented in Embedded Software Libraries (FSLESL) and described in *GFLIB User's Guide* (document CM4GFLIBUG). The disadvantage of the PI controller in the AC system is the permanent tracking error, which can be eliminated by the fast current loop.

$$\text{Eq. 15} \qquad G_{PI}(s) = K_P + \frac{K_I}{s} = K_I \frac{1 + \dfrac{s}{\omega_z}}{s}$$

The whole control loop is shown in Figure 4. Considering the transport delay caused by digital implementation, the performance of the analog design approach is very close to the direct digital approach.
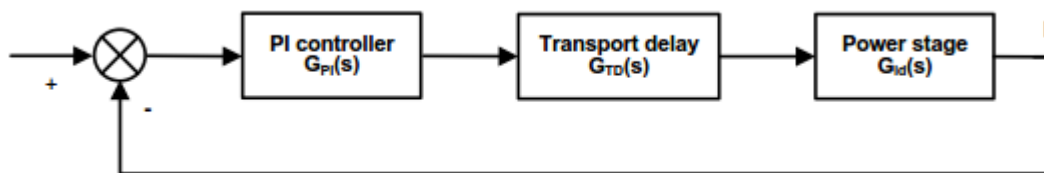
Figure 4. Current control loop

The first step in the current control loop design is to write a transfer function for the open control loop. It consists of the transfer function of the PI controller, the transfer function of the system, and the transport delay:

$$\textbf{Eq. 16} \qquad G_{Open}(s) = G_{PI}(s) \cdot G_{TD}(s) \cdot G_{id}(s) = \left(K_I \frac{1 + \dfrac{s}{\omega_z}}{s} \right) \cdot \left(\frac{1 - \dfrac{sT_D}{2}}{1 + \dfrac{sT_D}{2}} \right) \cdot \left(\frac{V_{OUT}}{sL} \right)$$

The performance of the control loop is defined by the cross-over frequency ω_c and the phase margin φ_{pm}. Because the cross-over frequency directly impacts the total harmonic distortion (THD) of the PFC, it must be as high as possible. On the other hand, the cross-over frequency must not be higher than 10-20 % of the control-loop sampling frequency. The phase margin impacts the overshoot during the step change at the input of the PI controller. A good compromise is the phase margin between 45-60°.

The parameters of the PI controller are calculated using the known transfer function of the open loop and the rules for a stable control loop. The position/frequency of the controller zero ω_z is calculated as:

$$\textbf{Eq. 17} \qquad \omega_z = \frac{\omega_c}{\tan(\varphi_{pm} + 2\arctan(\dfrac{T_D}{2}\omega_c))}$$

When ω_z is known, the integral gain K_I of the PI controller is obtained as:

$$\textbf{Eq. 18} \qquad K_I = \frac{L}{V_{OUT}} \cdot \frac{\omega_c^2}{\sqrt{1 + \dfrac{\omega_c^2}{\omega_z^2}}}$$

Finally, the proportional gain of the controller is calculated as:

$$\textbf{Eq. 19} \qquad K_P = \frac{K_I}{\omega_z}$$

The PI controller constants are calculated using real quantities. In a digital implementation, all quantities are scaled into the range which can be represented by the MCU. Scale the PI controller constants into the internal MCU representation according to Eq. 20 and Eq. 21. For more details, see the *GFLIB_CtrlPIpAW()* function in *GFLIB User's Guide* (document CM4GFLIBUG).

$$\textbf{\textit{Eq. 20}} \qquad G_{P\_scaled} = K_P \cdot \frac{e_{max}}{u_{max}}$$

$$\textbf{\textit{Eq. 21}} \qquad G_{I\_scaled} = K_I \cdot T_S \cdot \frac{e_{max}}{u_{max}}$$

3.2. Voltage-control loop design

3.2.1. Voltage-control loop transfer function

The outer voltage-control loop is derived in a similar way as the current-control loop. Figure 3 leads to these four equations:

$$\textbf{\textit{Eq. 22}} \qquad \frac{V_{OUT}}{|v_{in}|} = \frac{1}{1-d}$$

$$\textbf{\textit{Eq. 23}} \qquad 1-d = \frac{\overline{V_{IN}}|\sin(\omega t)|}{V_{OUT}}$$

$$\textbf{\textit{Eq. 24}} \qquad i_L = \overline{I_L}|\sin(\omega t)|$$

$$\textbf{\textit{Eq. 25}} \qquad i_D = (1-d) \cdot i_L$$

where $\overline{V}_{IN}$ and $\overline{I}_L$ are amplitudes of the input voltage and the inductor current. After the rearranging and mathematical manipulation, the output current i_D is expressed as:

$$\textbf{\textit{Eq. 26}} \qquad i_D = \frac{\overline{V}_{IN}\overline{I}_L}{2V_{OUT}} - \frac{\overline{V}_{IN}\overline{I}_L}{2V_{OUT}}\cos(2\omega t)$$

The first term corresponds to the DC part and the second term to the AC part of i_D. Applying averaging and small-signal perturbation results in:

$$\textbf{\textit{Eq. 27}} \qquad \hat{i}_D = \frac{1}{2}\frac{\overline{V}_{iN}\hat{i}_L}{V_{OUT}} - \frac{\hat{v}_{OUT}I_D}{V_{OUT}}$$

The diode current $\hat{i}_D$ is expressed according to the type of load as:

$$\textbf{Eq. 28} \qquad \hat{i}_D = \hat{v}_{OUT}Cs - \frac{\hat{v}_{OUT}I_D}{V_{OUT}}$$

for constant output power, or

$$\textbf{Eq. 29} \qquad \hat{i}_D = \hat{v}_{OUT}Cs + \frac{\hat{v}_{OUT}I_D}{V_{OUT}}$$

for resistive load. For further calculation, consider the constant output power load. After substituting Eq. 28 into Eq. 27, Eq. 27 can be rewritten as:

$$\textbf{Eq. 30} \qquad G_{vi}(s) = \frac{\hat{v}_{OUT}}{\hat{i}_L} = \frac{1}{2}\frac{\overline{V}_{IN}}{V_{OUT}Cs}$$

which is the final transfer function of the outer voltage-control loop.

3.2.2. Voltage loop controller design

The voltage controller design procedure is very similar to the current controller design. The processing delay in the system is not considered, because the voltage loop is oversampled when compared to the required bandwidth of the control loop. The processing delay is therefore very small and can be neglected. The voltage-control loop block diagram is shown in this figure:
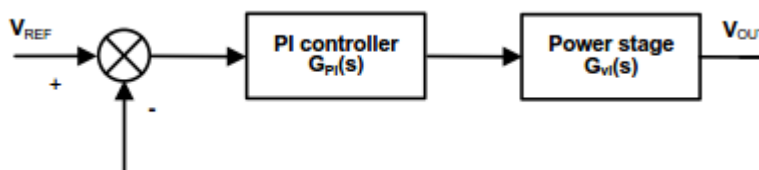

Figure 5. Voltage loop block diagram

Then open-loop transfer function for Figure 5 can be written as:

$$\textbf{Eq. 31} \qquad G_{Open}(s) = G_{PI}(s) \cdot G_{vi}(s) = \left(K_I \frac{1 + \dfrac{s}{\omega_z}}{s} \right) \cdot \left(\frac{1}{2}\frac{\overline{V}_{IN}}{CsV_{OUT}} \right)$$

The transfer function of the voltage open loop is expressed in Eq. 31. The performance of the control loop is again defined by the control loop bandwidth ω_c and phase margin φ_{pm}. One of the requirements for the voltage-control loop is to attenuate the voltage ripple at $2\omega_s$. Therefore, the bandwidth of the control loop must be very small, usually set from 0.1 to 0.2 of $2\omega_s$. The phase margin is set close to 90°, because the voltage overshoot of the DC-bus voltage is not desired.

When ω_c and φ_{pm} are defined, the PI controller constants are calculated as:

$$\text{Eq. 32} \qquad \omega_z = \frac{\omega_c}{\tan(\varphi_{pm} - \frac{\pi}{2} + \arctan(\omega_c C \frac{R}{2}))}$$

$$\text{Eq. 33} \qquad K_I = \frac{4V_{OUT}}{R\bar{V}_{IN}} \frac{\omega_c \sqrt{1+(\omega_c C \frac{R}{2})^2}}{\sqrt{1+(\frac{\omega_c}{\omega_z})^2}}$$

Finally, the proportional gain of the controller is calculated as:

$$\text{Eq. 34} \qquad K_P = \frac{K_I}{\omega_z}$$

The PI controller constants must be again scaled into the internal digital representation (see Eq. 20 and Eq. 21.)

3.3. Voltage feed-forward block design

The purpose of the voltage feed-forward block is to compensate for the variation of input voltage in the voltage-control loop. The feed-forward block is described by Eq. 35, where A is the voltage controller output (required current amplitude), B is the input voltage, and C is the RMS value of the input voltage.

$$\text{Eq. 35} \qquad x = \frac{AB}{C^2}$$

The RMS value of the input voltage is obtained by filtering the input voltage using Butterworth second-order filter (n=2) from the FSLESL library. The transfer function for the second-order filter is expressed as:

$$\text{Eq. 36} \qquad H(s) = \frac{\omega_c^2}{s^2 + s\sqrt{2}\omega_c + \omega_c^2}$$

The filter stop frequency ω_{STOP} is set to $2\omega_s$, where ω_s is the main frequency in rad/s. The filter attenuation G_S is chosen from the required THD, for example 1.5 %. The cut-off frequency is then calculated as:

$$\text{Eq. 37} \qquad \omega_c = \frac{\omega_{STOP}}{\sqrt[n^2]{10^{-G_s/10} - 1}}$$

The filter transfer function is transformed into the digital domain using bilinear transformation.
The general form of a second-order filter in the digital domain is expressed as:

$$\text{Eq. 38} \qquad H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

For the second-order Butterworth filter, all filter coefficients (a_1, a_2, b_0, b_1, and b_2) are expressed as:

$$\text{Eq. 39} \qquad b_0 = \frac{\omega_c^2}{\frac{4}{T^2} + \frac{2\sqrt{2}}{T}\omega_c + \omega_c^2}$$

$$\text{Eq. 40} \qquad b_1 = \frac{\omega_c^2}{\frac{4}{T^2} + \frac{2\sqrt{2}}{T}\omega_c + \omega_c^2}$$

$$\text{Eq. 41} \qquad b_2 = \frac{\omega_c^2}{\frac{4}{T^2} + \frac{2\sqrt{2}}{T}\omega_c + \omega_c^2}$$

$$\text{Eq. 42} \qquad a_1 = \frac{\omega_c^2}{\frac{4}{T^2} + \frac{2\sqrt{2}}{T}\omega_c + \omega_c^2}$$

$$\text{Eq. 43} \qquad a_2 = \frac{\omega_c^2}{\frac{4}{T^2} + \frac{2\sqrt{2}}{T}\omega_c + \omega_c^2}$$

Because the filter provides an average value of filter's output, the filtered value must be multiplied by $\frac{\pi}{2\sqrt{2}}$ to get the RMS value of the input voltage. For more details about filter constants' calculation, see *GDFLIB User's Guide* (document CM4GDFLIBUG).

4. Conclusion

This application note provides guidance on designing a stable PFC control system based on the boost converter topology. This document is accompanied by another application note that describes the implementation of interleaved PFC for a specific hardware platform (see Section 5, "References").

5. References

- *GFLIB User's Guide* (document CM4GFLIBUG)
- *GDFLIB User's Guide* (document CM4GDFLIBUG)
- *AN PFC implementation* (document ANxxxx)

6. Revision History

This table summarizes the changes done to this document since the initial release:

Table 1.   Revision history

Revision number	Date	Substantive changes
0	02/2016	Initial release.

Document Number: AN5257
Rev. 0
02/2016