**NXP Semiconductors**
Application Note

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# SPI topics: watchdog, serial output and parity check

for the dual SOIC 24 V high-side switch family

## 1 Introduction

This application note describes SPI robustness with respect to the Watchdog & parity check and the SPI Serial Output data of the following devices:

- MC06XS4200
- MC10XS4200
- MC20XS4200
- MC22XS4200
- MC50XS4200

These intelligent high-side switches are designed for use in 24 V systems such as trucks, busses, and special engines. They are applicable to other industrial and 12 V applications as well. The low $R_{DS(on)}$ channels can be used to control incandescent lamps, LEDs, solenoids, or DC motors. Control, device configuration, and diagnostics are performed through a 16-bit SPI interface, allowing easy integration into existing applications. For complete feature descriptions, refer to the individual data sheets for the devices.

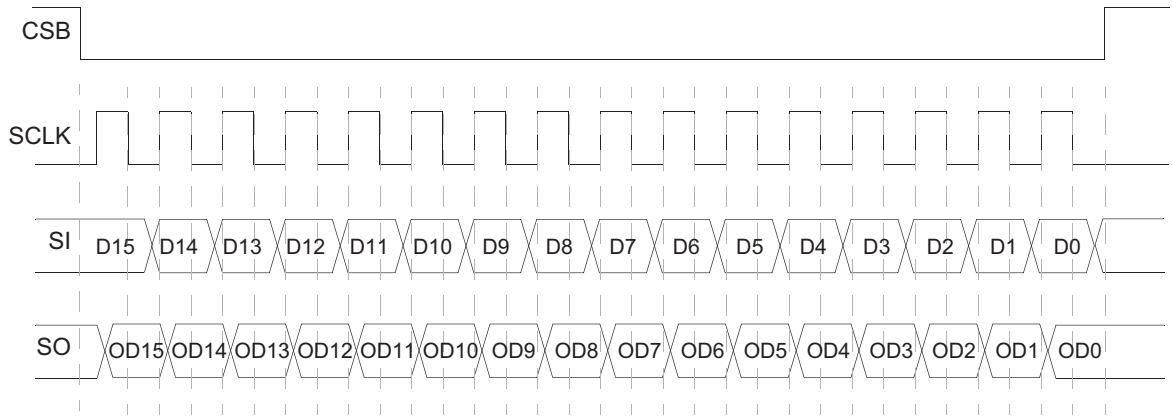
Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

**Contents**

# 2 SPI

## 2.1 Serial output register

The SPI interface offers full duplex, synchronous data transfers over four I/O lines: Serial Input (SI), Serial Output (SO), Serial Clock (SCLK), and Chip Select (CSB).The SI / SO pins of the device follow a first-in first-out (D15 to D0) protocol. Transfer of input and output words starts with the most significant bit (MSB).




Notes 1. RSTB must be in a logic [1] state during data transfer.
2. Data enter the SI pin starting with D15 (MSB) and ending with bit D0.
3. Data are available on the SO pin starting with bit OD15 (MSB) and ending with bit 0 (OD0).

**Figure 1. 16-bit SPI interface timing diagram**

**Table 1. SI message bit assignment**

| Bit n | SI register bit | Bit functional description |
|---|---|---|
| MSB<br>.<br>.<br>.<br>LSB | D15 | Watchdog in (WDIN): Its state must be alternated at least once within the timeout period |
| | D14 | Parity (P) check. P-bit must be set to 0 for an even number of 1-bits and to 1 for an odd number. |
| | D13 | Selection between SI registers from bank 0 (0 = channel 0) and bank 1 |
| | D12:D10 | Register address bits |
| | D9:D0 | Used to configure the device and the protective functions and to address the SO registers |

The SO output value depends on the register previously selected by the STATR register: The first sixteen SO register bits are set to the address previously accessed by SI word (bit D13, D2…D0 of the STATR_s input register).

Figure 2 shows an SPI sequence under various circumstances, illustrating the SI frames and the corresponding contents of the SO register.

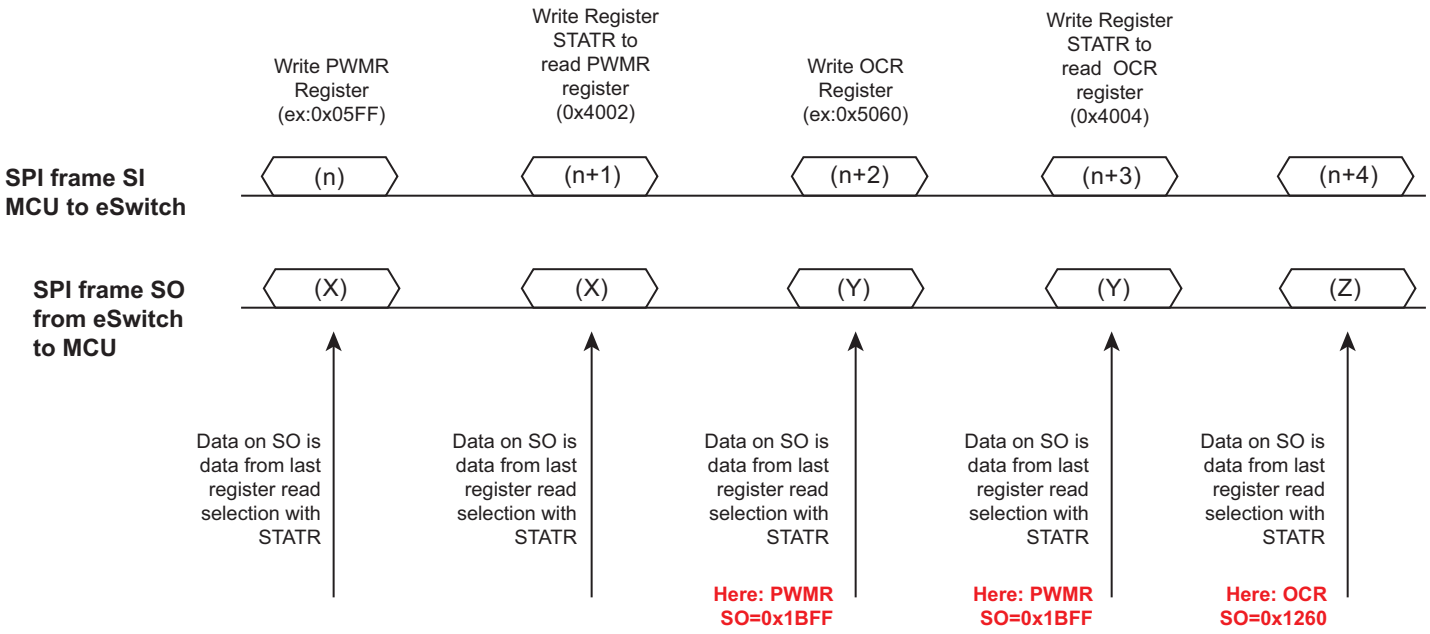



**Figure 2. SO message versus SI write commands**

## 2.2 Control of written SI data

To determine in real time if the SPI communication occurred without errors, extend the frame to 32 bits. Send two identical 16-bit words consecutively on SI, with the CSB pin released for the duration of the 32 bits. The SO output will then report the STATR selected register and the second word from SI.

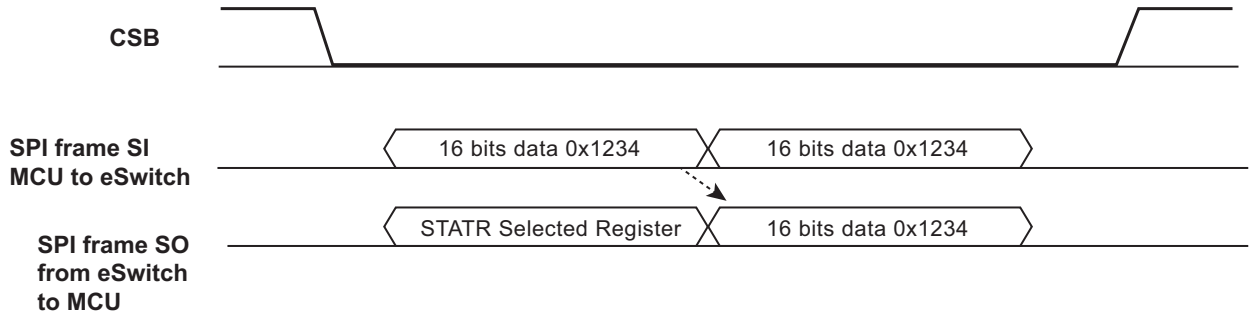



**Figure 3. 32-bit SPI interface**

# 3 SPI robustness monitoring feature

The device monitors the SPI communication robustness through the Watchdog bit and parity check. Parity check (P) must be set so that the total number of 1-bits in the SPI word is even. The Watchdog feature monitors whether the communication has been lost. The device monitors the state of the first bit (WDIN) of the SPI frame.

## 3.1 Watchdog

When the state of the WDIN bit remains unchanged within a data stream of duration $t_{WDTO}$ = 310 ms typ., the device assumes SPI communication has been lost and enters Fail-safe mode. The FSOB pin then goes low. This behavior can be disabled by setting the bit WD_DIS = 1 (register GCR, bit D4)

The Watchdog timer starts at the rising edge of RSTB. The SPI frames must be sent with the WDIN bit alternating at least once within the 310 ms timeframe.

When the RSTB is not under control (for example, if the device happens to enter Fail-safe Mode at start up,) a sequence must be run to exit from the aforementioned mode:

1. Send a SPI frame with WDIS bit =1 (D15), The register and contents do not matter.
2. Send a second SPI frame with WDIS bit=0 within the 310 ms timeframe.

Figure 4 describe the Watchdog timing:

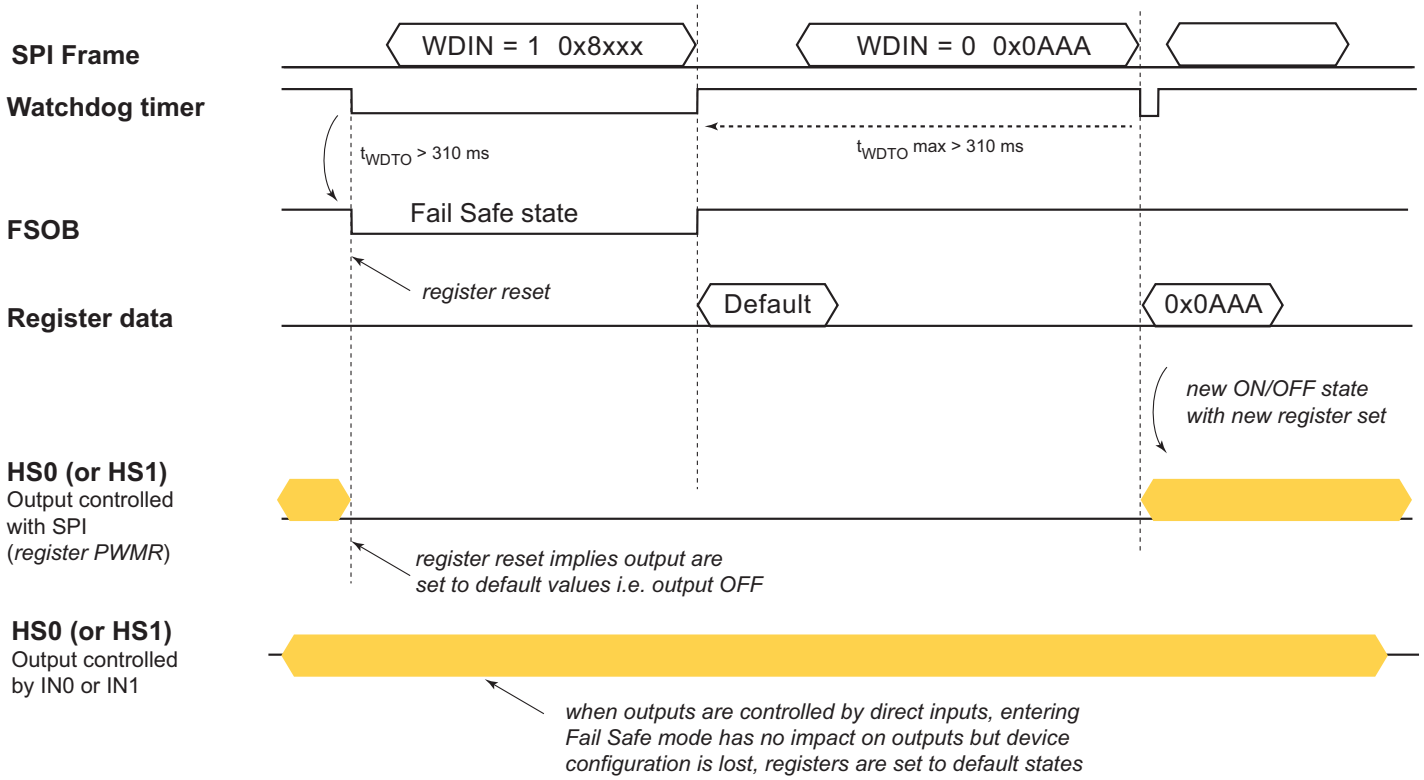



**Figure 4. Watchdog timing diagram**

When the device enters Fail-safe mode, the output states differ depending on the control method used:

- If the ON/OFF state is controlled by registers (PWMR register), the registers are reset to default values and the outputs are switched OFF.
- If the ON/OFF state is controlled by direct inputs IN0 & IN1, the outputs remain controlled by IN0 & IN1 and are not switched OFF. The register are reset to default values.

## 3.2 Parity check

Parity check (P) must be set with an even number of 1-bits in the SPI word (P = 0 for an even number of 1-bits and P = 1 for an odd number.) The parity bit is Bit14 of the SPI frame. If the MCU happens to erroneously set a communication fault or Parity bit, the device reports the parity error at the next SPI frame even if the SPI frame indicates no parity error.

Figure 5 show several scenarios of an SPI sequence. The drawing illustrates the parity errors on the SI frames and the corresponding contents on SO. The SO output bits follow the same rule described in Figure 4. In this example, the PWMR register is selected with STATR for SO read and all register writings apply to the PWMR register.

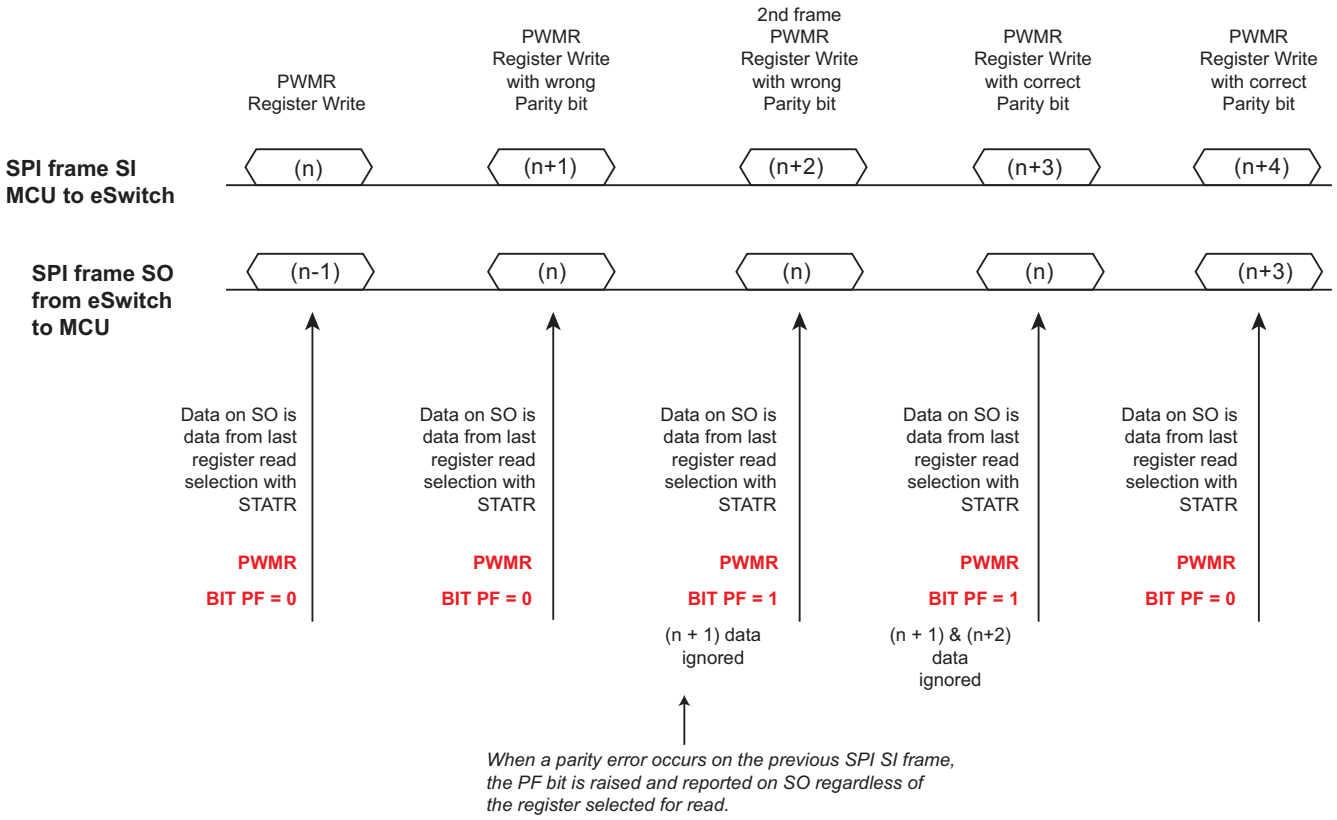



**Figure 5. Parity check**

# 4 SPI unused address 011

As shown in Figure 6, the address 011, bit D12-D10 of the Serial Input register addresses is not used. Register writes to this address are ignored and the SO data reports the content of the previous read register selected. If the STATR register selects the 011 address as the selected register, the read and write is ignored and the result of the previous register selection is used.

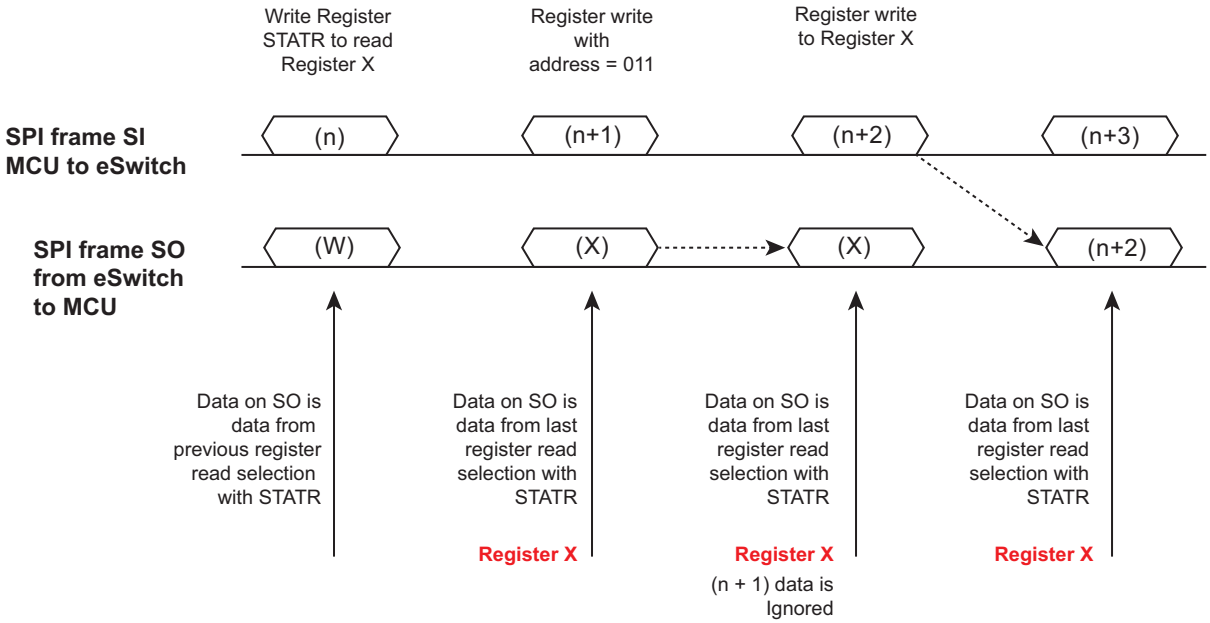



**Figure 6. Addressing address 011**

# 5 Revision history

| Revision | Date | Description |
|---|---|---|
| 1.0 | 5/2015 | • Initial release |
| | 7/2016 | • Updated to NXP document form and style |

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