Freescale Semiconductor
Application Note

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Transitioning from FXAS21000C to FXAS21002C

Hardware and Software Considerations

Contents

1 Introduction

This application note describes the hardware and software differences between FXAS21000C and FXAS21002C and provides information on transitioning from FXAS21000C to FXAS21002C. It also presents a recommended application schematic that can accommodate either device via zero-ohm jumper population changes. To enable easy software migration, minor register map and digital feature differences between the two parts are highlighted.

The key content is divided into two major sections. Section 4 explains the hardware considerations in transitioning from FXAS21000C to FXAS21002C, and Section 5 details the software considerations.

2 Key Benefits of using FXAS21002C

Improved battery life in portable applications by reducing overall power consumption.

- Reduced current consumption in Active mode from 5.8 mA to 2.6 mA.
- Reduced Standby to Active mode transition time from 200 ms to 60 ms, which reduces system power consumption.

Enhanced user experience through performance improvements

- Reduced noise from 55 mdps√Hz to 25 mdps√Hz
- Increased maximum full-scale range (FSR) from 1600 dps to 2000 dps. Allows higher rotational rates, especially for sports and gaming applications.
- Increased digital output (ADC) resolution from 14 bit to 16 bit. Allows higher precision in angular rate measurements.
- Improved angular velocity resolution from 200 mdps/LSB in ±1600 dps FSR mode to 62.5 mdps/LSB in ±2000 dps FSR mode. Allows higher precision in angular rate measurements.
- Increased maximum output data rate (ODR) from 200 Hz to 800 Hz.

Key feature enhancements from FXAS21000C to FXAS21002C

- Programmable digital low-pass filter: Used for further limiting the digital output data bandwidth and noise.
- Power mode transition control via external pin: Available for accelerometer-based power management (motion interrupt).
- I^2C interface mode: I^2C Fast Mode Plus, allowing SCL frequency up to 1 MHz.
- Enhanced auto-increment read address pointer behavior to facilitate faster read out of the FIFO data in a burst-read operation.

3 Upgrade Guide

Switching from FXAS21000C to FXAS21002C is extremely convenient. Systems designed with FXAS21000C can easily be upgraded to FXAS21002C without making any major changes in the pin layout or driver code. Here are a few minor changes that need to be made in the hardware and software:

- Changes to be made in the software
  - Change value of WHO_AM _I register.
  - Configure **CTRL_REG3** (new register in FXAS21002C) for additional functionalities, including external power CTRL using the INT2 pin.
  - Reconfigure **CTRL_REG1[**DR**]** field for setting the desired ODR and **CTRL_REG0[**BW**]** for setting the LPF cutoff frequency correctly.

- Changes to be made in the hardware
  - When implementing SPI Interface, connect pin 8 to V_{DDIO}.
  - For external power control, by configuring **CTRL_REG3**[EXTCTRLEN], pin 2 (INT2) can be used as an input.

All the above mentioned changes in the hardware and software are described in detail in the following hardware and software consideration sections, respectively.

4 Hardware Considerations

FXAS21000C and FXAS21002C are highly similar in their pin layout and digital interface (I2c and SPI) circuits. The exceptions are described in this section.

4.1 Pinout Adjustments

The pinouts of FXAS21000C and FXAS21002C are slightly different. These differences in the pin layout and the corresponding functionality can be seen in Table 1. The most significant difference is pin 8. On the FXAS21000C, pin 8 is not used. On the FXAS21002C, pin 8 is used to select the digital communications mode, either I^2C or SPI. To select I^2C mode, connect pin 8 to GND. To select SPI mode, connect pin 8 to V_{DDIO}.

More functionality has been added to pin 2 of the FXAS21002C. In addition to being an interrupt output, pin 2 can also serve as an input to provide power state control.

Table 1. Pin changes

Pin	FXAS21000C		FXAS21002C	
	Name	Function	Name	Function
2	INT2	Interrupt Output 2	INT2/PWR_CTRL	Interrupt Output 2 / Power state transition control input
8	Reserved	Reserved - Must be tied to ground	I^2C_B/SPI	Digital interface selection pin. This pin must be tied either high or low to select SPI or I^2C interface mode, respectively.

4.2 I^2C and SPI Connection Changes

The FXAS21000C and FXAS21002C devices have I^2C and SPI interfaces available. The differences between the devices, for each interface, are described in this section. **Note:** No changes need to be made in the hardware for I^2C communication when switching from FXAS21000C to FXAS21002C.

When using the SPI interface option, the recommended circuit for the FXAS21000C will not function properly with the FXAS21002C part. In order to implement SPI mode on the FXAS21002C, pin 8 must be connected to V_{DDIO} keeping the rest of the circuit similar to FXAS21000C. Figure 1 and Figure 2 illustrate the SPI connection layout for both sensors. Figure 1 is identical with Figure 2, except for the pin 8 connectivity.

We recommend the circuit design in Figure 2, which is compatible with either part.

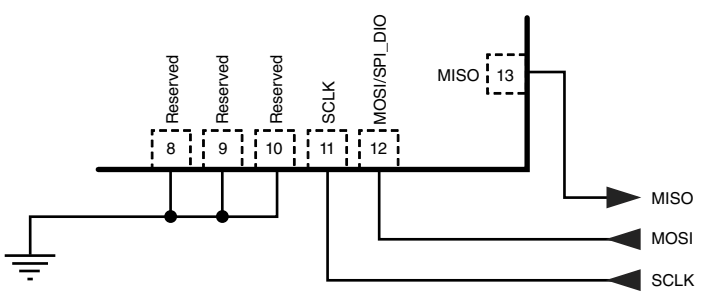

Figure 1. SPI connection for FXAS21000C only

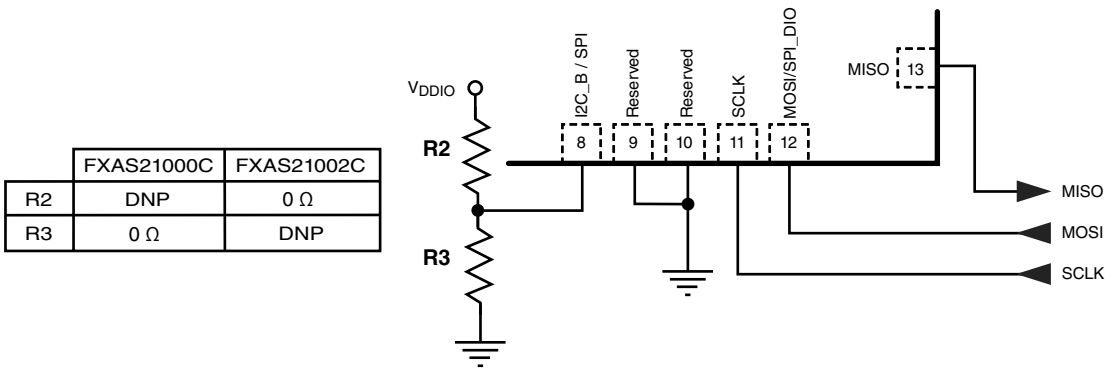

Figure 2. FXAS21000C and FXAS21002C SPI connection with resistor selection network

5 Software Considerations

FXAS21002C and FXAS21000C have similar register map definitions and are largely software compatible; the exceptions are described in this section.

5.1 FSR and sensitivity differences

FXAS21000C and FXAS21002C have differences in FSR and ADC resolution, both of which affect the conversion from ADC LSBs to angular rate in degrees per second (dps). In both devices, the FSR is selected using the **CTRL_REG0**[FS] field.

Table 2. Full-scale range and sensitivity

CTRL_REG0[FS]	FSR (dps)		Sensitivity (mdps/LSB)	
	FXAS21000C	FXAS21002C	FXAS21000C	FXAS21002C
0b00	±1600	±2000	200	62.5
0b01	±800	±1000	100	31.25
0b10	±400	±500	50	15.63
0b11	±200	±250	25	7.82

FXAS21000C has 14 bits of ADC resolution and FXAS21002C has 16 bits of ADC resolution. FSR selections and angular rate sensitivities are shown in Table 2.

The register configuration for FSR settings does not need to be changed when switching from FXAS21000C to FXAS21002C. This is because for the same register configuration, the closest matching (higher) FSR and sensitivity will be obtained from the FXAS21002C as shown in Table 3. **Note:** In software, interpretation of output will require slight adjustment to account for the increased precision.

5.2 Register differences

There are some differences in the registers between FXAS21000C and FXAS21002C.

Table 3. Register differences

Name	FXAS21000C	FXAS21002C
OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB	Format: 14-bit, left justified, 2's complement	Format: 16-bit, 2's complement
CTRL_REG3	Does not exist	Address: 0x15
WHO_AM_I	Value: 0xD1	Value: 0xD6

Note: 14 bit output for FXAS21000 is obtained by removing the last two bits of LSB data for each axis (right shifting two bits).

From the perspective of device driver software, when switching from FXAS21000C to FXAS21002C the following register changes need to be made:

- Change the WHO_AM_I value as shown in Table 3 for the driver to identify the device correctly.
- Configure the new register CTRL_REG3 (0x15) in FXAS21002C for additional functionalities.
- Change **CTRL_REG1**[DR] to set the ODR as desired and change **CTRL_REG0**[BW] to set the LPF cutoff as desired.

5.3 ODR selections

The output data rate (ODR) for both FXAS21000C and FXAS21002C is selected using the 3-bit **CTRL_REG1**[DR] field as shown in Table 4.

Table 4. Output data rate

Decimal number	CTRL_REG1[DR]	ODR (Hz)	
		FXAS21000C	FXAS21002C
0	0b000	200	800
1	0b001	100	400
2	0b010	50	200
3	0b011	25	100
4	0b100	12.5	50
5	0b101	6.25	25
6	0b110	3.125	12.5
7	0b111	1.5625	12.5

As shown in Table 4, for the same **CTRL_REG1**[DR] field, the ODR of FXAS21002C is four times that of FXAS21000C. This register should be reconfigured accordingly because, on switching from FXAS21000C to FXAS21002C, the same register configuration would lead to significant change (four times) in the ODR.

In order to maintain the same ODR as configured for FXAS21000C, starting from 200 Hz, the simplest way to reconfigure the registers is by adding the decimal equivalent *2* to the current **CTRL_REG1**[DR] field value. For example, suppose the system is using an FXAS21000C sensor and is configured for an ODR of 100 Hz, the **CTRL_REG1**[DR] field in that case would be configured to 0b001 (whose decimal equivalent is 1). Now, on switching to the sensor FXAS21002C, decimal

number 2 needs to be added to the **CTRL_REG1[**DR**]** field. Therefore, the field now reads 1 + 2 = 3 (0b011). The field 0b011 corresponds to the ODR of 100 Hz for FXAS21002C. This way, registers can be configured to get the same ODR for FXAS21002C.

This method can cover ODRs from 200 Hz to 12.5 Hz ODR (corresponding to decimal numbers 2 to 6) for FXAS21002C. In order to achieve an ODR of 800 Hz and 400 Hz, registers can be configured for FXAS21002C, corresponding to decimal numbers 0 and 1 respectively, unlike in FXAS21000C. **Note:** FXAS21002C has a minimum 12.5 Hz ODR.

5.4 Zero-rate offset feature

FXAS21000C has a built-in hardware feature to zero the angular rate offset by setting the ZR_COND bit in **CTRL_REG0** when FXAS21000C is stationary. Zero-rate offset removal is typically best handled in host software by methods such as bias estimation and tracking in sensor fusion algorithms. As such, this feature has not been included in FXAS21002C.

5.5 Digital low-pass filter (LPF)

FXAS21002C features a second-order digital LPF function that may be used to further limit the output signal bandwidth beyond the ODR/2 Nyquist limiting that is performed by the anti-aliasing filter ahead of the ADC. The LPF is not available on FXAS21000C. The LPF feature cutoff frequency is a function of the selected ODR and the BW1 and BW0 control bits in **CTRL_REG0**.

In FXAS21000C, bits 7 and 6 in **CTRL_REG0** are not implemented—writes to these bits have no effect and reads always return 0:

Table 5. FXAS21000C CTRL_REG0 implementation

Bit	7	6	5	4	3	2	1	0
Read	0	0	SPIW	SEL[1:0]		HPF_EN	FS[1:0]	
Write								
Reset	0	0	0	0b00		0	0b00	

In FXAS21000C, output signal bandwidth is always equal to ODR/2. For example, ODR of 200 Hz leads to bandwidth of 100 Hz.

In FXAS21002C, bits 7 and 6 in **CTRL_REG0** are used to set the LPF cutoff frequency and are called BW1 and BW0, respectively. See Table 6.

Table 6. FXAS21002C CTRL_REG0 implementation

Bit	7	6	5	4	3	2	1	0
Read	BW1	BW0	SPIW	SEL[1:0]		HPF_EN	FS[1:0]	
Write								
Reset	0	0	0	0b00		0	0b00	

In FXAS21002C, setting up BW1 and BW0 will allow the output signal bandwidth to go below ODR/2, unlike in FXAS21000C. For example, an ODR of 800 Hz will lead to a bandwidth less than 400 Hz, ranging from 256 Hz to 64 Hz, depending on the BW1 and BW0 values.

The LPF cutoff frequency, therefore, is a function of the ODR selection made in **CTRL_REG1**, and the BW1 and BW0 settings. This is illustrated in Table 7.

Table 7. FXAS21002C LPF cutoff frequency

BW	ODR = 800 Hz	ODR = 400 Hz	ODR = 200 Hz	ODR = 100 Hz	ODR = 50 Hz	ODR = 25 Hz	ODR = 12.5 Hz
0b00	256	128	64	32	16	8	4
0b01	128	64	32	16	8	4	—
0b1x	64	32	16	8	4	—	—

When switching the sensor hardware to FXAS21002C, the BW1 and BW0, which were unimplemented in FXAS21000C, now give an output signal bandwidth, as shown in Table 7, corresponding to the configured ODR.

For example, when an ODR of 200 Hz in FXAS21000C with BW[1:0] equals 0b00, the output signal bandwidth equals 200/2, or 100 Hz. On FXAS21002C, the same configuration of BW[1:0] for ODR of 200 gives an output signal bandwidth of 64 Hz. This can be further scaled down by a factor of two until the bandwidth equals 16 Hz simply by incrementing BW[1:0] by 1. Therefore, when BW[1:0] is equal to 0b01, the output bandwidth is 64/2, which equals 32 Hz. For 0b10,the output bandwidth equals 16.

5.6 FIFO watermark event flag behavior

FXAS21000C and FXAS21002C clear the watermark interrupt event flag under different conditions.

For FXAS21000C, the watermark event flag (**F_WMKF**) is cleared by reading the **F_STATUS** register. Reading **F_STATUS** also clears the **SRC_FIFO** bit in the **INT_SOURCE_FLAG (0x0B)** register.

For FXAS21002C, the watermark event flag (**F_WMKF**) is cleared by reading enough samples from the FIFO for the sample count to go below the watermark level set in **F_SETUP**[F_WMRK].

5.7 Additional control register (CTRL_REG3) at 0x15

FXAS21002C implements an additional control register named **CTRL_REG3** at address 0x15. FXAS21000C does not include this register; the user space register map ends at address 0x14. As this is a new register in FXAS21002C, **CTRL_REG3** needs to be configured to utilize new features on this sensor.

Table 8. CTRL_REG3 register

Bit	7	6	5	4	3	2	1	0
Read	—	—	—	—	WRAPTOONE	EXTCTRLEN	—	FSR_DOUBLE
Write								
Reset	—	—	—	—	0	0	—	0

WRAPTOONE controls the behavior of the auto-increment read address pointer. When WRAPTOONE = 0, the auto-increment pointer rolls over to address 0x00 (**STATUS**) after the Z-axis LSB register is read. When WRAPTOONE = 1, the auto-increment pointer wraps around to address 0x01 (X-axis MSB) in order to facilitate the faster read out of the FIFO data in a burst-read operation (**STATUS** register only needs to be read once per FIFO burst-read operation).

EXTCTRLEN allows the device operating mode to be controlled using the INT2 pin (the pin becomes a high impedance input when this bit is set high). The input is level sensitive, and allows the host to transition the device operating mode from Standby to Active or from Ready to Active (and vice-versa) depending on the state of the Ready bit at the time

EXTCTRLEN is set. This feature can be useful in applications where the accelerometer motion detection function is used to power manage the gyro (for example, by placing it in a lower power state when the platform is stationary within certain pre-determined conditions). When EXTCTRLEN is 0, INT2 pin is used as an interrupt output (default). **Note:** When EXTCTRLEN = 1, the ACTIVE bit in **CTRL_REG1** is directly controlled by the logic state of the INT2 pin, and this bit becomes read only using the I^2C or SPI register interfaces.

FSR_DOUBLE allows the full-scale range selections of FXAS21002C to be increased by a factor of 2, from ±250/500/1000/2000°/s to ±500/1000/2000/4000°/s. This feature is provided to enable a higher dynamic range for sports applications such as golf club or tennis racket swings and other applications that require an increased dynamic range. While the full-scale range is doubled in this mode, the noise and nonlinearity of the output signal are also increased. When **FSR_DOUBLE** = 1, the sensitivity will be increased as shown in Table 9.

Table 9. Enabling a higher dynamic range

FSR Selection	Sensitivity (mdps/LSB) FSR_DOUBLE = 0	Sensitivity (mdps/LSB) FSR_DOUBLE = 1
CTRL_REG0[FS] = 00	62.50	125
CTRL_REG0[FS] = 01	31.25	62.5
CTRL_REG0[FS] = 10	15.63	31.25
CTRL_REG0[FS] = 11	7.81	15.63

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