Freescale Semiconductor
Application Note

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Dead-Time Compensation Method for Vector-Controlled VSI Drives Based on Qorivva Family

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Contents

1 Introduction

One of the main problems in pulse width modulated voltage-source inverter (PWM-VSI) drives is the nonlinear voltage gain caused by non-ideal characteristics of the power inverter. The most important nonlinearity is caused by the necessary blanking time between top and bottom switch to avoid inverter leg shout-through of the DC bus circuit. The type of the switch and pre-driver characteristics determine amount of the necessary blank time. The error caused by this phenomena can be significant in various cases and can cause the drive regulation issues and system instabilities.

This application note shows one of the methods to minimize or eliminate impact of the inserted blanking time so-called dead-time.

2 Dead-time phenomena

2.1 Inverter model

A typical cascade control structure for PMSM motor is shown in Figure 1. The motor control algorithm outputs are six PWM signals for VSI inverter top and bottom switches (MOSFET, IGBT, etc.), which define their on and off times respectively.

The on and off time define a value of the applied voltage by the converter itself. A VSI converter for modeling purposes and investigation of control behavior can be considered as a black box with a certain gain and phase delay. The gain Kr can be specified as shown in Equation 1 on page 2 . The inverter is sampled data system. The sampling interval gives you an indication about converter delay and is linked with the PWM period. A delay is specified as a half of the sampling period (PWM period). The transfer function in continuous time domain is shown in Equation 2 on page 2.

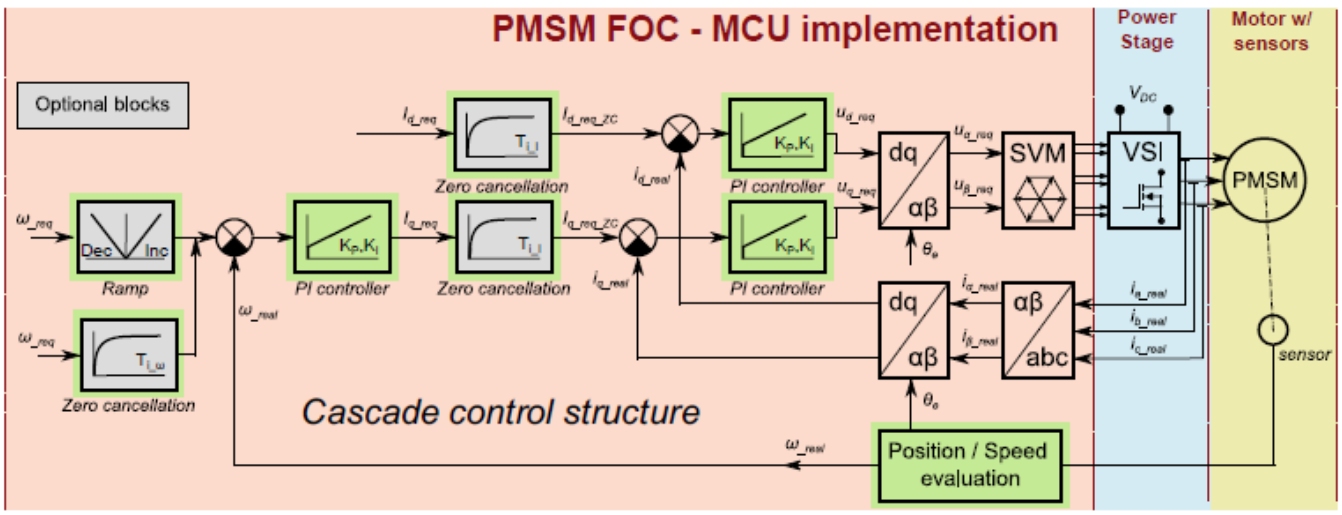


Figure 1. PMSM cascade structure

$$K_r = \frac{\frac{2}{\pi} * V_{dc}}{V_{cm}}$$

Equation 1

$$G(s) = \frac{K_r}{1 + sT}$$

Equation 2

2.2 Dead-time interpretation

To perform correct status change of the power switches in the inverter leg, a PWM generator should insert small amount of time between required switching edges for top and bottom switch. This time is called dead-time. It can vary from 0 to 5 microsecond, depends on the type of the switch, supply voltage, and gate driver capability etc. As was mentioned before the system has to insert some amount of blank time between top and bottom switches. This delay insert a load dependent (magnitude and phase) error in the generated output voltage.

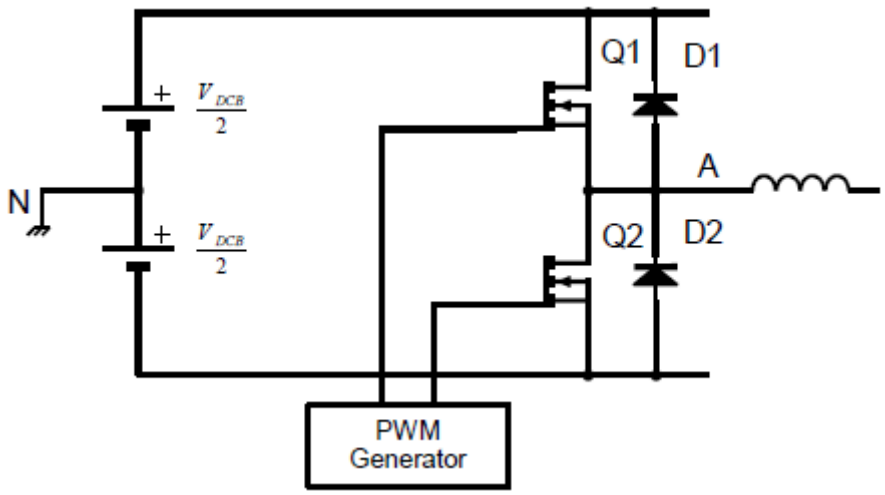


Figure 2. Simplified inverter one phase circuit

Since the blank time is inserted in each period, the error voltage introduces a serious waveform distortion. It increases with switching frequency introducing harmonic component that, if not compensated, may cause instabilities as well as additional losses in controlled machine. Another source of output voltage distortion may be a finite voltage drop across the switches. To examine an effect of the dead-time on the inverter output voltage, see what happen in one inverter leg per one pwm period. The basic configuration shown in Figure 2 consist of high and low side switches Q1 and Q2, and their reverse recovery diodes D1 and D2, connected between positive and negative rails of power supply. The driving signals are created in the PWM generation module. The output is connected to motor phase winding and current flowing from inverter has positive sign.

The volt-second algorithm developed is based on the well-known average voltage method. The basic principle is to compensate a average phase voltage loss or gain in each switching period. Figure 3 shows load voltage waveform for converter with MOSFET switches. These waveforms suppose that the load current at dead-time event is continuously flowing through switching devices or body diodes.

Let us suppose that PWM module counter counts from $-T_S/2$ to $T_S/2$, where T_S is PWM switching period. At the time T1 resp. T2 a PWM module wants to generate rising resp. falling edge of the PWMA signal. At this event the system inserts a dead-time, in which turn-on transistor passes into the off state and at the end of this interval second transistor in the inverter leg passes into the on state. This interval is added twice in one PWM period (rising and falling edge). The load volt-second balance (average voltage applied on the load) per one PWM period is changed. As is shown in Figure 3 a voltage curve depends on the polarity of the load current. The change of the phase average voltage is equal to error caused by the dead-time phenomena and can be calculated as is shown below.

A volt-second balance (average voltage) per one PWM period can be derived from Equation 3 on page 3.

$$\overline{V_{an}} = \frac{1}{Ts}\int_{0}^{Ts} v_{an}(t)d(t)$$

Equation 3.

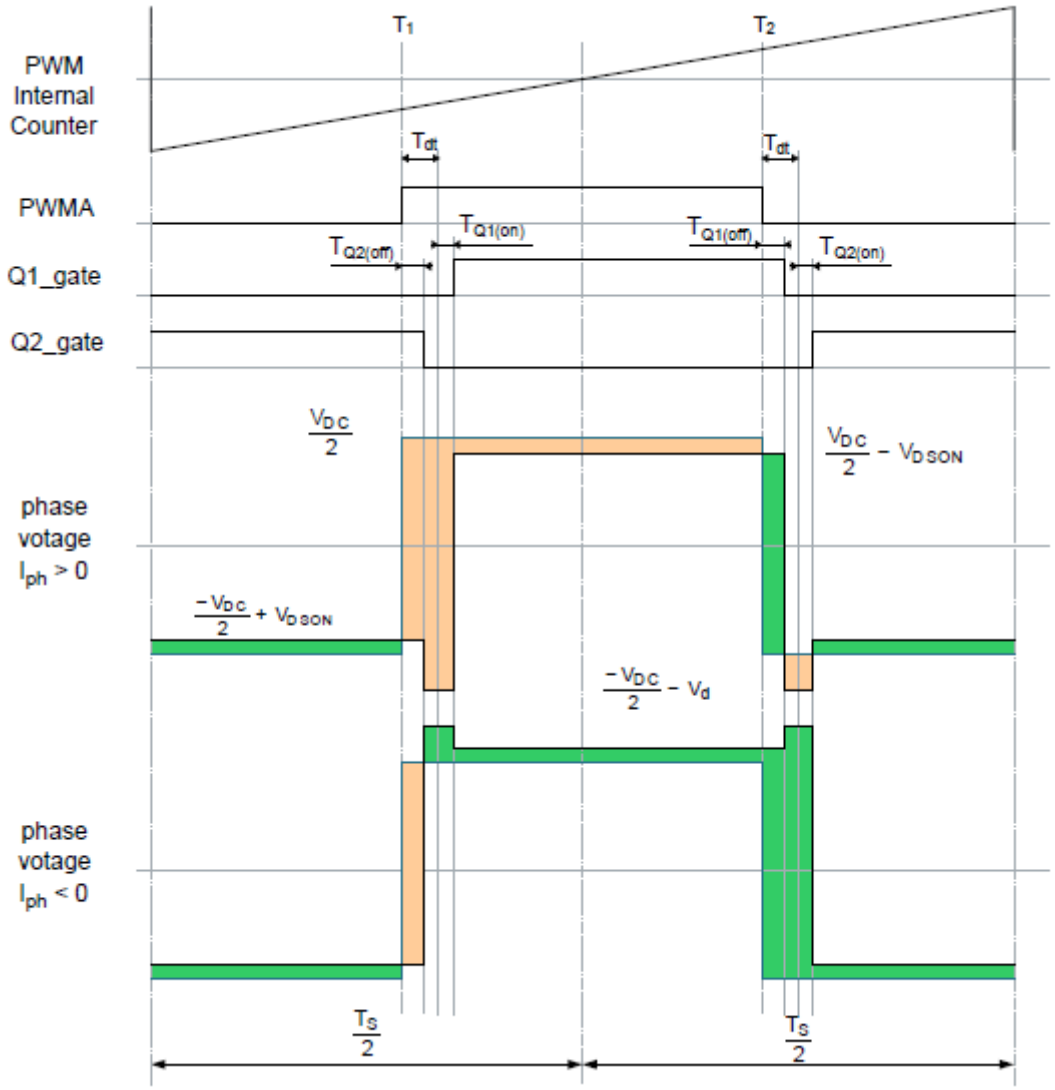


Figure 3. Phase voltage per one PWM period

For the positive load current the average phase voltage can be calculated as:

$$\overline{V_{ANP}} = \frac{1}{T_s}\int_0^{T_s} v_{anp}(t)d(t)$$

$$= (-\frac{V_{dc}}{2} + V_{DSQ2(on)}) * (\frac{((\frac{T_S}{2} - (T_1 - T_{Q2(off)})) + (\frac{T_S}{2} - (T_2 + T_{DT} + T_{Q2(on)})))}{T_S})$$

$$+ (-\frac{V_{DC}}{2} - V_D) * ((T_1 - T_{Q2(off)} - (T_1 - T_{DT} - T_{Q1(on)})) + (T_2 + T_{DT} + T_{Q2(on)} - (T_2 + T_{Q1(off)})))$$

$$+ (\frac{V_{DC}}{2} - V_{DSQ1(on)}) * (\frac{((T_1 - T_{DT} - T_{Q1(on)}) + (T_2 + T_{Q1(off)}))}{T_S})$$

$$= (-\frac{V_{DC}}{2} + V_{DSQ2(on)}) * (\frac{(T_S - (T_1 + T_2) - (T_{DT} + T_{Q2(on)} - T_{Q2(off)}))}{T_S})$$

$$+ (-\frac{V_{DC}}{2} - V_D) * (\frac{((T_{Q1(on)} + T_{DT} - T_{Q2(off)}) + (T_{DT} + T_{Q2(on)} - T_{Q1(off)}))}{T_S})$$

$$+ ((\frac{V_{DC}}{2} - V_{DSQ1(on)}) * (\frac{((T_1 + T_2) - T_{DT} - T_{Q1(on)} + T_{Q1(off)})}{T_S}))$$

Equation 4.

Let us suppose that the power inverter is equipped by the same transistors with the same dynamic parameters.

$$T_{Q1(on)} = T_{Q2(on)} = T_{Q(on)}$$
$$T_{Q1(off)} = T_{Q2(off)} = T_{Q(off)}$$
$$V_{DSQ1(on)} = V_{DSQ2(on)} = V_{DS(on)}$$

Equation 5.

$$T_1 + T_2 = T_{ON} ... required on - time for phase from SVM module$$
$$\frac{T_{ON}}{T_S} = DC ... required phase duty - cycle from SVM module$$

Equation 6.

Substituting Equation 5 on page 5 and Equation 6 on page 5 into Equation 4 on page 4, an average phase voltage for positive current load is acquired as follows:

$$\bar{V}_{ANP(real)} = \left(\frac{-V_{DC}}{2} + V_{DC(on)}\right) * \left(1 - DC - \frac{T_{DT} + T_{Q(on)} - T_{Q(off)}}{T_S}\right) - \left(\frac{V_{DC}}{2} + V_D\right) * \frac{2*(T_{DT} + (T_{Q(on)} - T_{Q(off)}))}{T_S} + \left(\frac{V_{DC}}{2} - V_{DS(on)}\right) * \left(DC - \frac{T_{DT} + (T_{Q(on)} - T_{Q(off)})}{T_S}\right)$$

Equation 7.

The same approach can be used for calculation of an average phase voltage per one PWM period for negative load current as shown in Equation 8 on page 5.

$$\bar{V}_{ANN(real)} = \left(\frac{-V_{DC}}{2} + V_{DC(on)}\right) \times \left(1 - DC - \frac{T_{DT} + T_{Q(on)} - T_{Q(off)}}{T_S}\right) + \left(\frac{V_{DC}}{2} + V_D\right) \frac{2 \times T_{DT} + 2\,\text{times}(T_{Q(on)} - T_{Q(off)})}{T_S} + \left(\frac{V_{DC}}{2} - V_{DS(on)}\right) \times \left(DC - \frac{T_{DT} + T_{Q(on)} - T_{Q(off)}}{T_S}\right)$$

Equation 8.

The required phase voltage can be calculated as:

$$\bar{V}_{ANP(ideal)} = -\frac{V_{DC}}{T_S} * (1 - DC) + \frac{V_{DC}}{T_S} * DC$$

Equation 9.

The error volt-second balance for MOSFET VSI inverter in a one phase can be calculated as difference of the ideal and real balance.

$$\bar{V}_{AN(err)} = \pm\left[V_{DS(on)} * \left(1 - 2 * \frac{T_{ON}}{T_S}\right) + (V_{DC} + 2 * V_D) * (T_{DT} + T_{D(on)} - T_{Q(off)})\right]$$

Equation 10.

Figure 4 shows a calculated ideal and real average phase voltages per one electrical period. The sign of the error caused by dead-time depends on the current polarity.

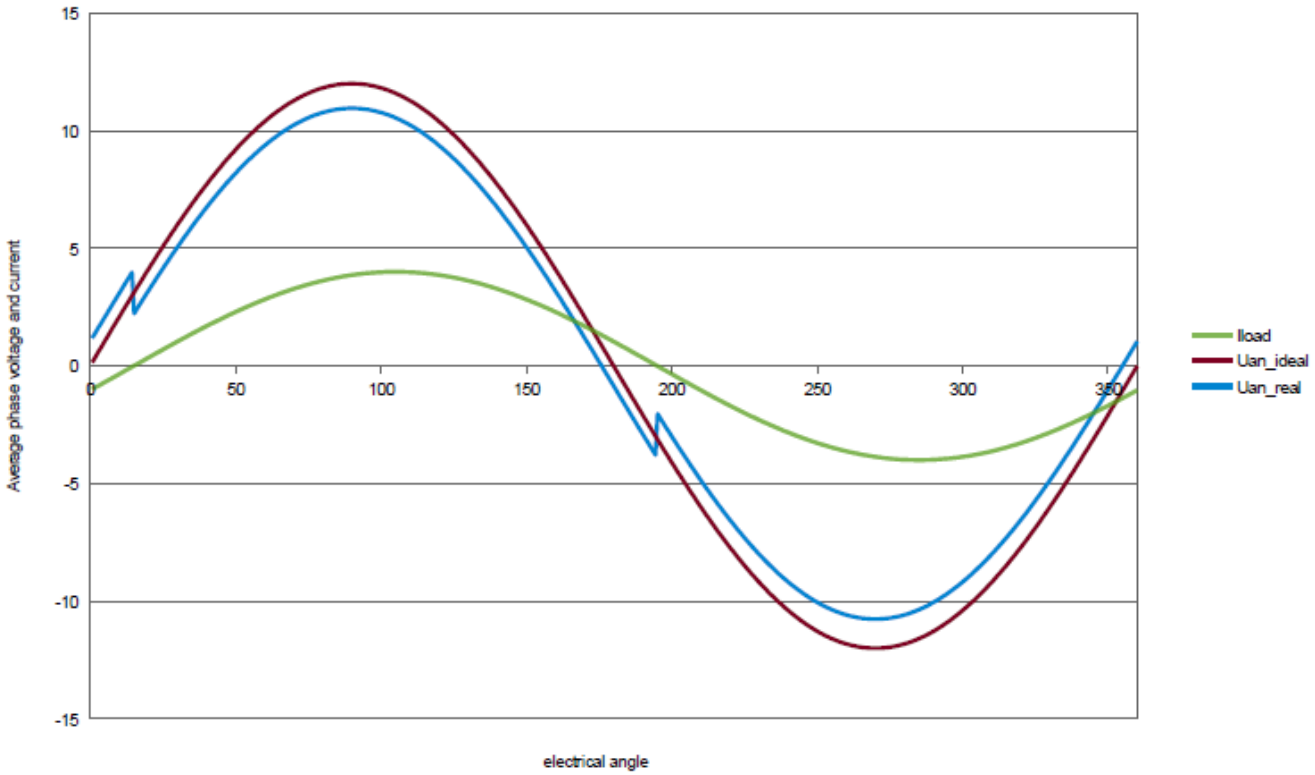


Figure 4. Estimated average phase voltage per one electrical revolution (ideal and with dead-time impact)

2.3 Error voltage transformation

The dead-time compensator function which is shown below could be obtained by analyzing the three phase error voltage caused by dead-time phenomena.

Let us suppose that the error voltage caused by dead-time insertion can be represented in the 3-phase ordinate system as a three vectors aligned with ABC phases and their summation results in the dead-time error voltage vector. The 3-phase inverter has a six active vectors, for each of them we can find out a resulting dead-time error voltage vector as is shown in Figure 5. Based on this we can reconstruct a phase error voltage per one electrical revolution, Figure 6. We can with advantage use a well known transformations from abc -> αβ (Figure 6), and since we know a electrical rotor position Θ_e we can also use transformation from αβ -> DQ ordinates (Figure 6). It results in the very simple compensation functions for D and Q part of the required voltage. Equations Equation 11 on page 6 to Equation 15 on page 7 quantify a compensator voltage value for D and Q part.

$$u_D = \frac{4}{3} \times U_{err} \times \cos(\frac{\pi}{3} \times k - \theta_e)$$

Equation 11.

$$u_Q = \frac{4}{3} \times U_{err} \times \sin(\frac{\pi}{3} \times k - \theta_e)$$

Equation 12.

$$U_{err} = \frac{t_{err}}{T_S} \times U_{DCBUS}$$

Equation 13.

$$t_{err} = t_{DT} + t_{Q(on)} - t_{Q(off)}$$

Equation 14.

$$k = 0 - 5 .. sectornumber \text{ from } SVM module$$

Equation 15.

, where ...

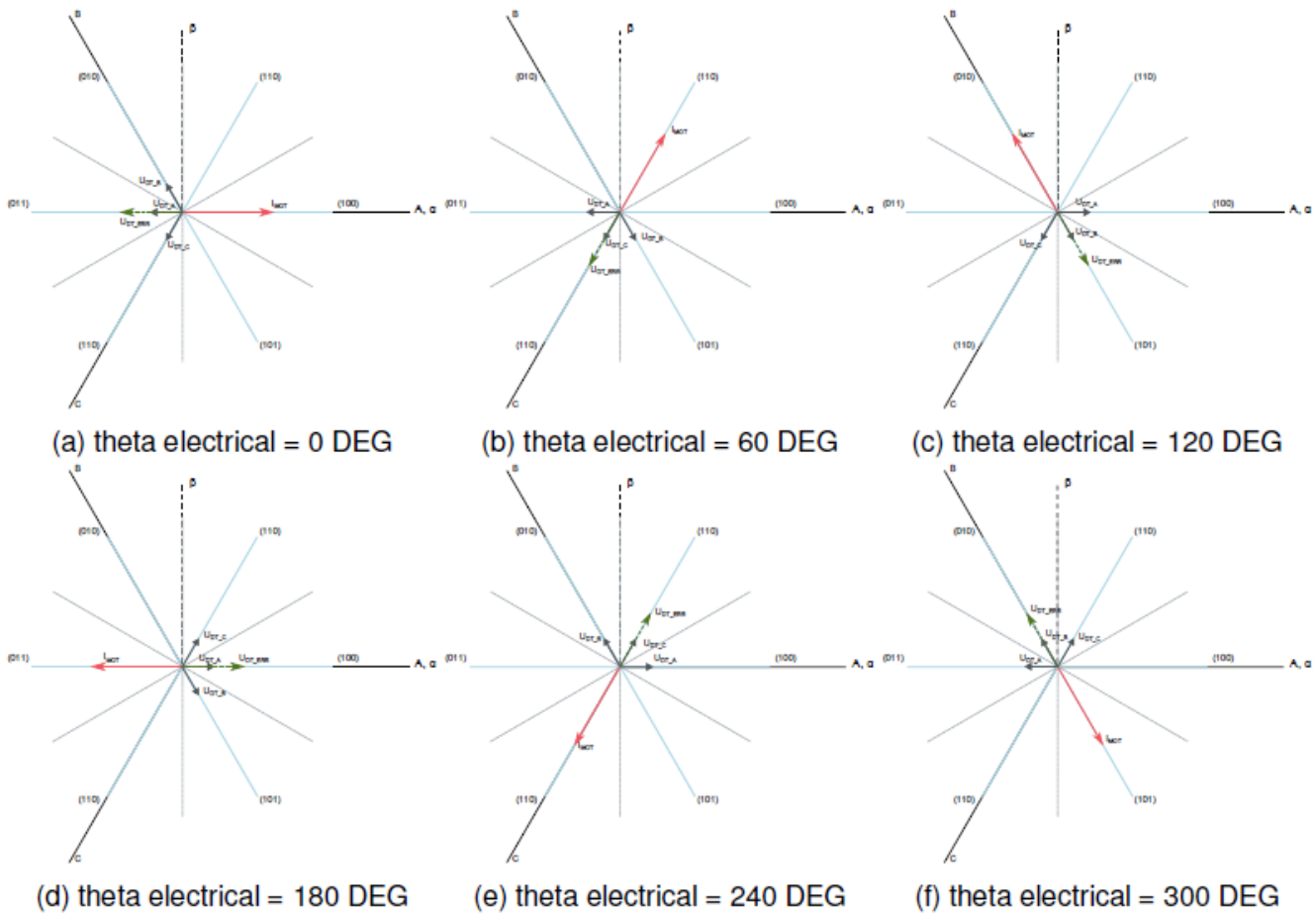
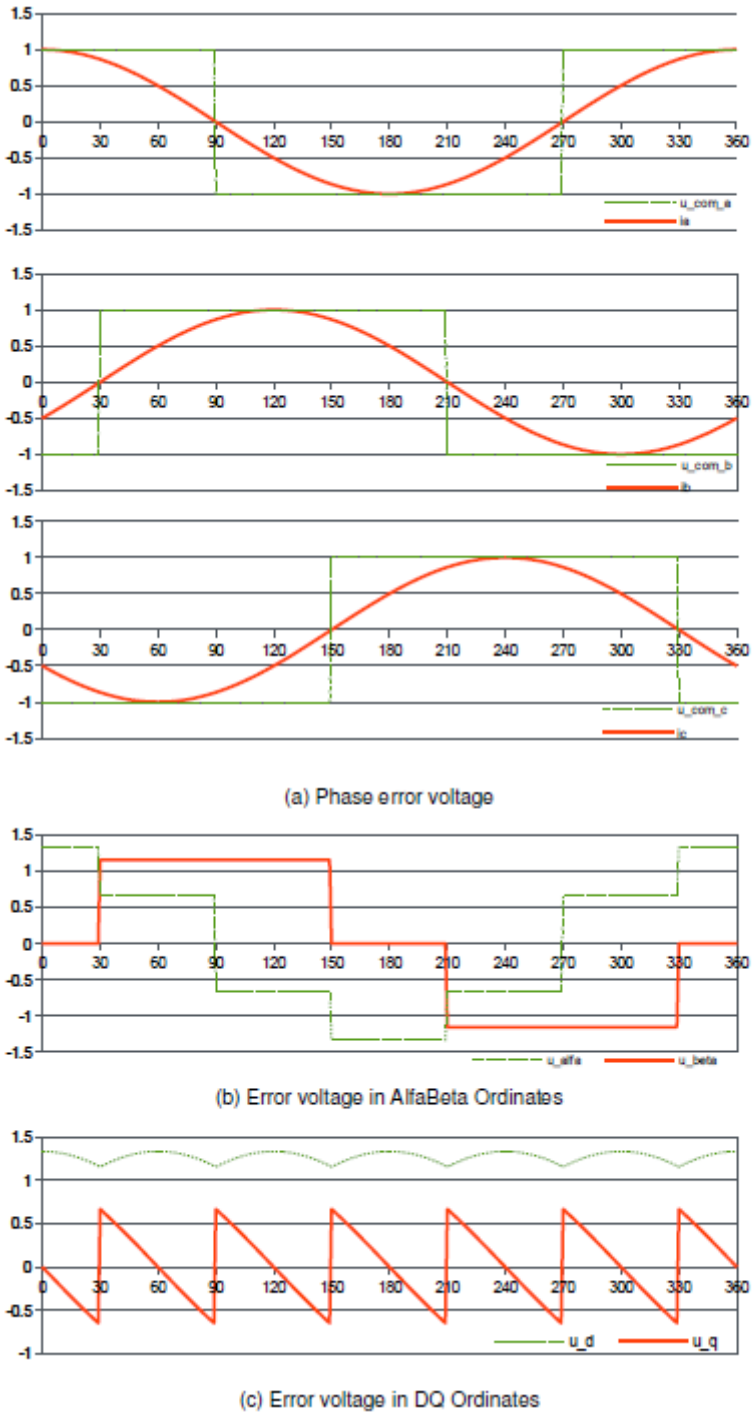


Figure 5. Error voltage vector interpretation



(a) Phase error voltage

(b) Error voltage in AlfaBeta Ordinates

(c) Error voltage in DQ Ordinates

Figure 6. Error voltage caused by dead-time effect per one electrical revolution

Since we know an error voltage value in DQ ordinates, we can use it to compensate dead-time effect as is shown in Figure 7.

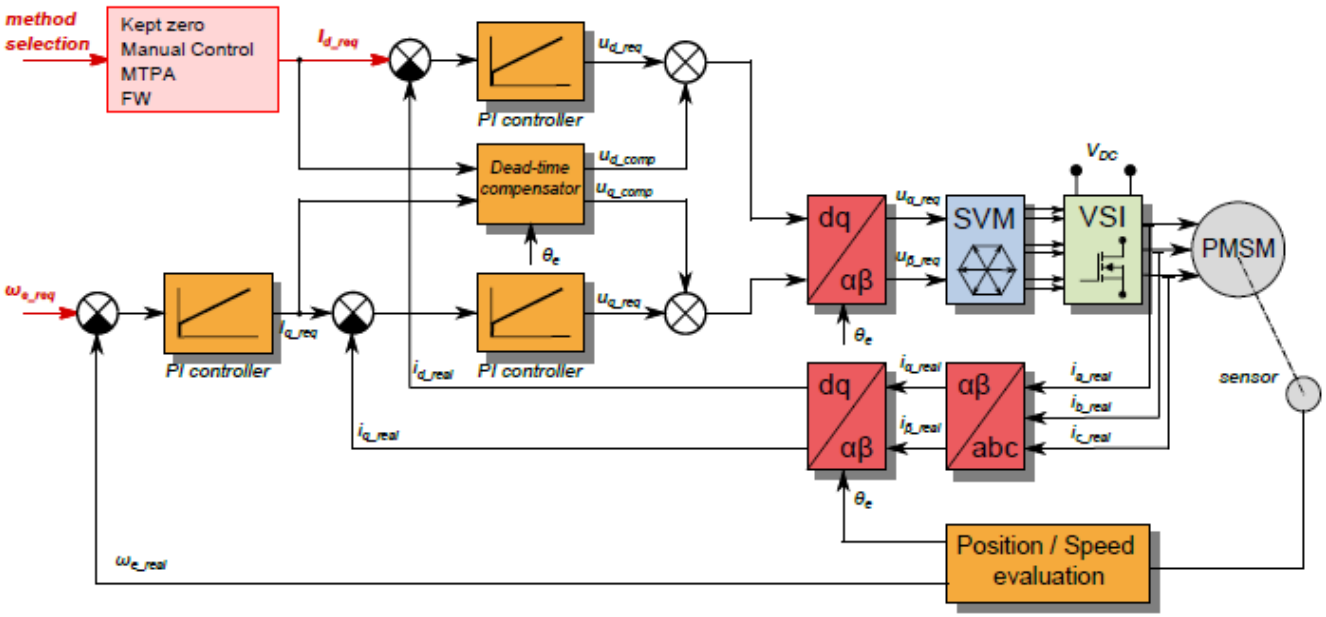
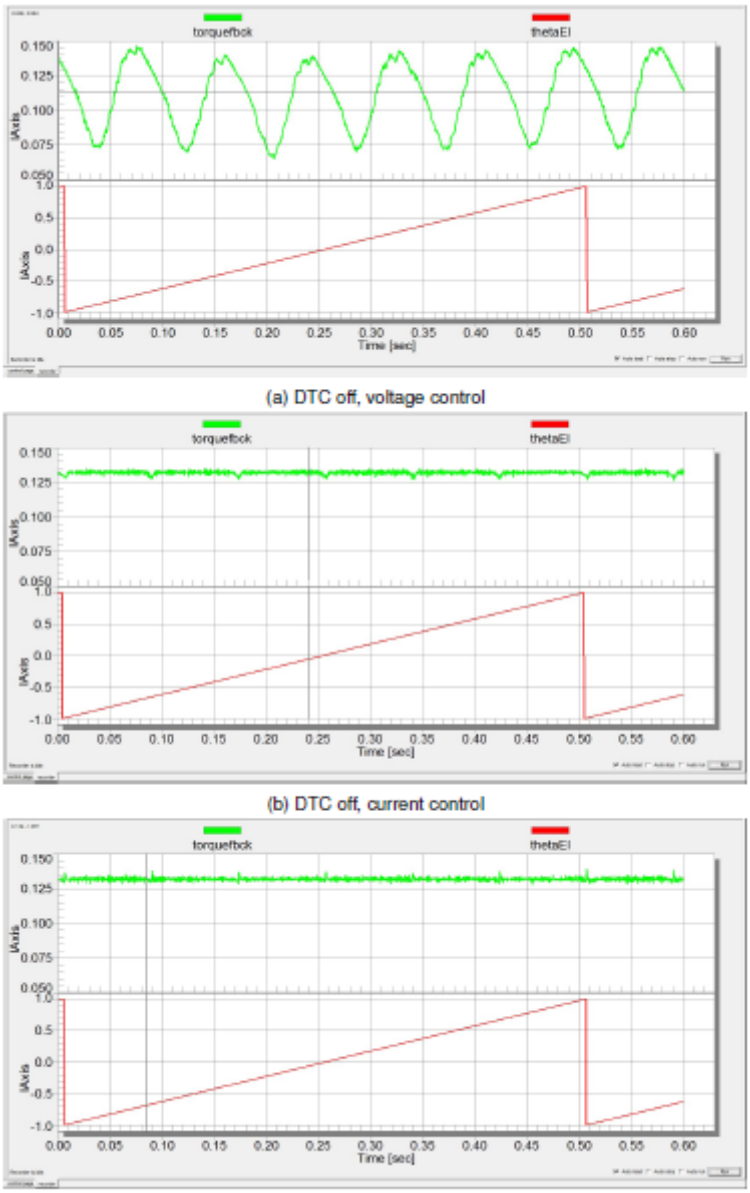


Figure 7. FOC structure with dead-time compensation algorithm

3 Conclusion

The proposed algorithm has been implemented on the MPC5604P device and tested with using the motor control connected to 3-phase inductances and/or PMSM motor. The impact of the dead-time has been investigated for different electrical motor frequencies. Figure 8, Figure 9, and Figure 10 show the impact of dead-time on the produced motor torque at different operational conditions. It can be seen that, on the low electrical frequencies (low speed) the current regulator is able to compensate a portion of the dead-time effect. The compensation could be used with advantage in sensor based field oriented control algorithms.

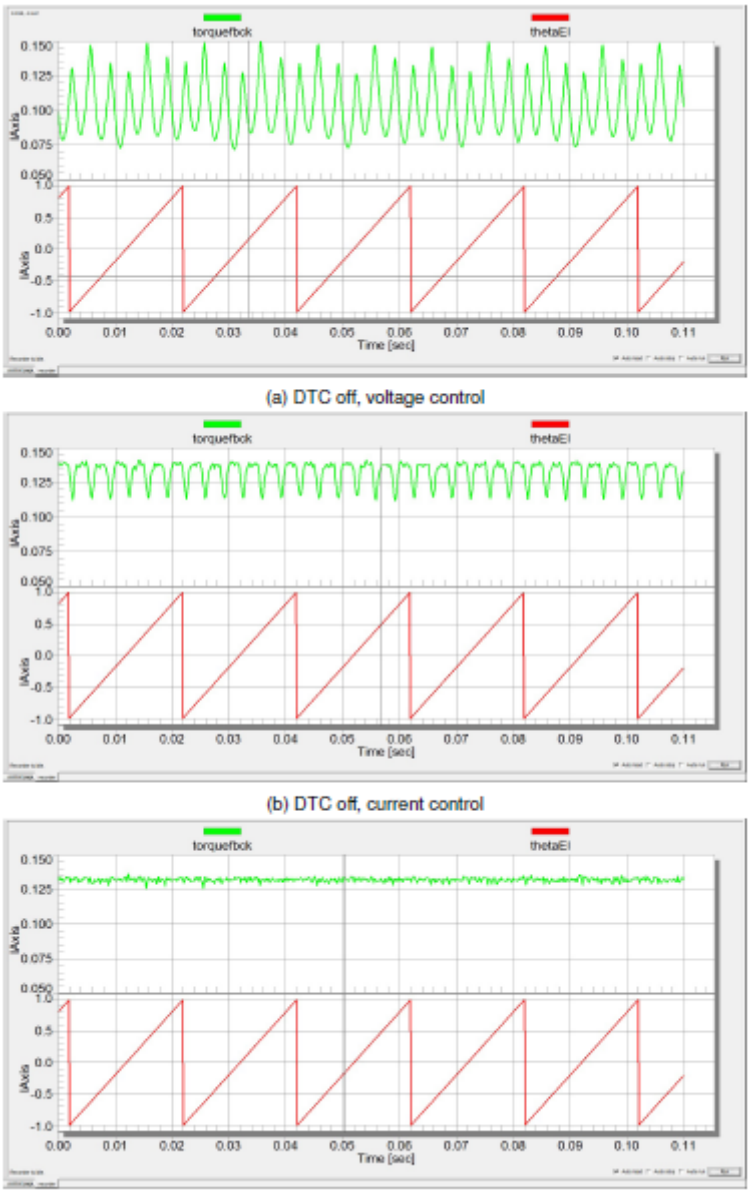


(a) DTC off, voltage control

(b) DTC off, current control

(c) DTC on, current control

Figure 8. Calculated motor torque at electrical frequency 2 Hz

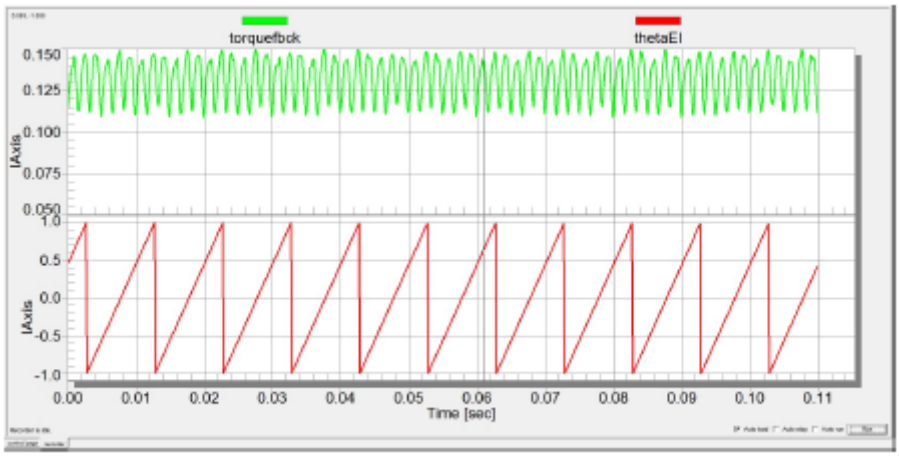


(a) DTC off, voltage control

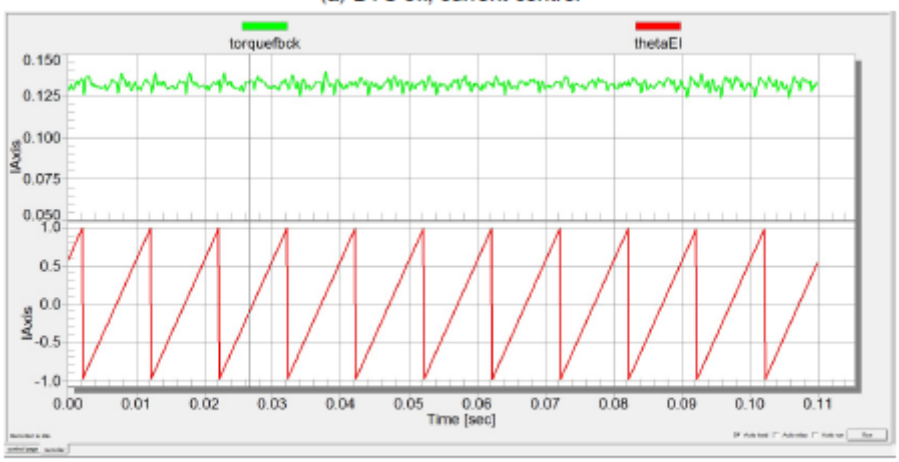
(b) DTC off, current control

(c) DTC on, current control

Figure 9. Calculated motor torque at electrical frequency 50 Hz



(a) DTC off, current control



(b) DTC on, current control

Figure 10. Calculated motor torque at electrical frequency 100 Hz

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