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A Minimum Evaluation System for the MC68331 and MC68332

By Ray Cornyn
Field Applications Group
Motorola Ltd., Aylesbury

INTRODUCTION

The MC68331 and MC68332 are members of Motorola's 68300 family of integrated 32-bit microprocessors. They are based on the 68000-compatible, CPU32 microprocessor core and include highly functional peripheral modules on the same silicon device.

This application note describes the design of a minimum evaluation system based on the MC68331 or MC68332. The system is intended as a low cost method of microprocessor evaluation and also as a starting point for engineers wishing to implement a development interface for their own designs. Due to the similarity in their pin-outs, both the MC68331 and MC68332 can be supported by the same evaluation board.

The system takes advantage of Background Debug Mode (BDM) which is a new development feature implemented on CPU32- based microprocessors. This mode supports the common features of a low level debugger such as register/memory modification, code download, software breakpoints and single line assembly/disassembly. This is accomplished without the need for either specific hardware or an external software monitor.

Each circuit consists of a 68331 or 68332 processor, two 32K x 8 static rams and a 32 KHz Crystal. The circuit is designed to support byte addressable 16-bit memory. Communication with BDM from a host computer is through a ten pin dual in line header.

CPU32

CPU32 is a user code compatible member of Motorola's 68000 family of microprocessors. It is a fully static design, implemented in HCMOS and is used as a microprocessor core for members of the 68300 family.

Although remaining code compatible with the original 68000, CPU32 has been enhanced to give significantly higher performance than the 68000 in most applications. Additions to the 68000 architecture have included support for two cycle memory access with dynamic bus sizing, upgraded microcode to reduce instruction cycle time and virtual memory support similar to the 68020. In addition to the performance enhancements to CPU32, the new core also includes a development interface called Background Debug Mode.

BACKGROUND DEBUG MODE

Background Debug Mode (BDM) is an additional mode of operation implemented on CPU32. It allows the user to communicate with an on-chip debug monitor through three specific interface pins DSI, DSO, and DSCLK/$\overline{\text{BKPT}}$. The protocol used is a 17-bit full duplex serial synchronous transfer with a clock rate of up to one half of the system clock. BDM is enabled by the user during reset by asserting the $\overline{\text{BKPT}}$ signal. With BDM enabled, software will be run as normal until any one of the following actions occurs. At this point control of the microprocessor is given to the debugger.

1. Double Bus Fault

This occurs when CPU32 responds to an initial bus error and while attempting to access the stack area to service this error, receives a second bus error. This normally indicates a serious system fault. With BDM enabled the CPU will switch to the debugger at this point. With BDM disabled this is a catastrophic failure mode causing the device to halt.

2. BGND Instruction

This is a new instruction added to CPU32. With BDM enabled this causes a switch to the debugger. With BDM disabled BGND is an illegal instruction causing an exception. BGND is normally used as a software breakpoint in BDM.

3. Hardware Breakpoint

Asserting the $\overline{\text{BKPT}}$ pin with BDM enabled forces the processor to switch to the debugger at the next instruction boundary. Without BDM enabled the processor will take the hardware breakpoint exception. (Vector offset $30).

When not in BDM the DSI pin becomes $\overline{\text{IFETCH}}$, the DSO pin becomes $\overline{\text{IPIPE}}$ and DSCLK becomes $\overline{\text{BKPT}}$. The functions of $\overline{\text{IFETCH}}$ and $\overline{\text{IPIPE}}$ are to offer information on the state of the internal pipeline. This data can be used by other development tools such as logic analysers and real time trace buffers when CPU32 is operating in normal running mode.

Debugger Commands

Once active the debugger supports the following commands:

Command	Mnemonic
Read Address or Data register	RAREG/RDREG
Write Address or Data Register	WAREG/WDREG
Read System Register	RSREG
Write System Register	WSREG
Read Memory Location	READ
Write Memory Location	WRITE
Dump Memory Block	DUMP
Fill Memory Block	FILL
Resume Execution	GO
Call User Code	CALL
Reset Peripherals	RST
No Operation	NOP

A full explanation of the bit patterns for each command can be found in the CPU32 users manual (CPU32 UM/AD). Although it is possible for the user to implement their own command interface for BDM., there are many ready made support packages available from both Motorola and third party companies which implement this for the user. See the section on BDM support products for details.

CIRCUIT OPERATION

The evaluation system makes use of the on-chip memory interface logic which is part of the MC68331 and MC68332 Systems Integration Modules. Each device has twelve programmable chip selects which can be programmed for memory block size, base address, port size, read or write and for wait state generation. Of the twelve chip selects $\overline{CSBOOT}$ is active immediately after reset, the others remain inactive until initialised by the microprocessor.

MEMORY INTERFACE

The circuit uses three chip selects to access the two memories. $\overline{CSBOOT}$ is used as the output enable on both upper and lower bytes. $\overline{CS0}$ and $\overline{CS1}$ are used as lower and upper write enables respectively. The circuit is designed to make the most effective use of the memory access time available by keeping both memory devices permanently enabled. $\overline{CSBOOT}$ is then used as the decoded output enable for both memories taking advantage of the reduced output enable access time of static RAM. With the memories permanently enabled a global asynchronous R/$\overline{W}$ signal can not be used. The additional chip selects are therefore used as decoded upper and lower write enables to the individual RAMs.

With this configuration two cycle memory access can be used with 35 ns static RAM.

NOTE: The evaluation system requires $\overline{CSBOOT}$,$\overline{CS0}$ and $\overline{CS1}$ to be initialised for correct memory operation.

CIRCUIT DETAILS

A block diagram for the evaluation system is shown in Figure 1 with a full schematic in Figure 2. Power requirements for the circuit are 5 Volts ± 10% and approximately 400 mA (see Figure 3).

BDM CONNECTIONS

In addition to DSI,DSO and DSCLK pins required for Background debug mode communications. The interface connector includes Vss, Vdd ,$\overline{RESET}$, $\overline{BERR}$ and Freeze. These signal are used by the host computer to monitor device operation and also to support additional debugging features. Freeze has the specific function of indicating to the host systems that the debugger is ready to communicate.

BDM SUPPORT PRODUCTS

Background Debug Mode as implemented on CPU32 requires a host computer system to interface with the processor during debug. Motorola and a range of third party companies have developed software and hardware support packages to allow BDM to be used with host computers such as the IBM PC. The evaluation system described in this application note is designed to be compatible with any of these BDM support products. A full list of BDM support products is given in Appendix A.

For development and test of the evaluation system, ICD32 from P+E Inc was used as the host debugger. This package is available both from Motorola and also from P+E Inc directly. It is a low cost development environment for the IBM PC consisting of an editor, assembler and source code debugger. The package also contains the hardware interface to allow direct communication through the printer port of a PC to the BDM port of the 68331 or 68332.

To simplify repetitive tasks such as processor initialisation. ICD32 supports a macro command file structure. This allows a series of ICD32 commands to be combined in a standard text file and then run as a single command by ICD32. If the macro file is called startup.icd, ICD32 will run this as an initialisation routine on power up.

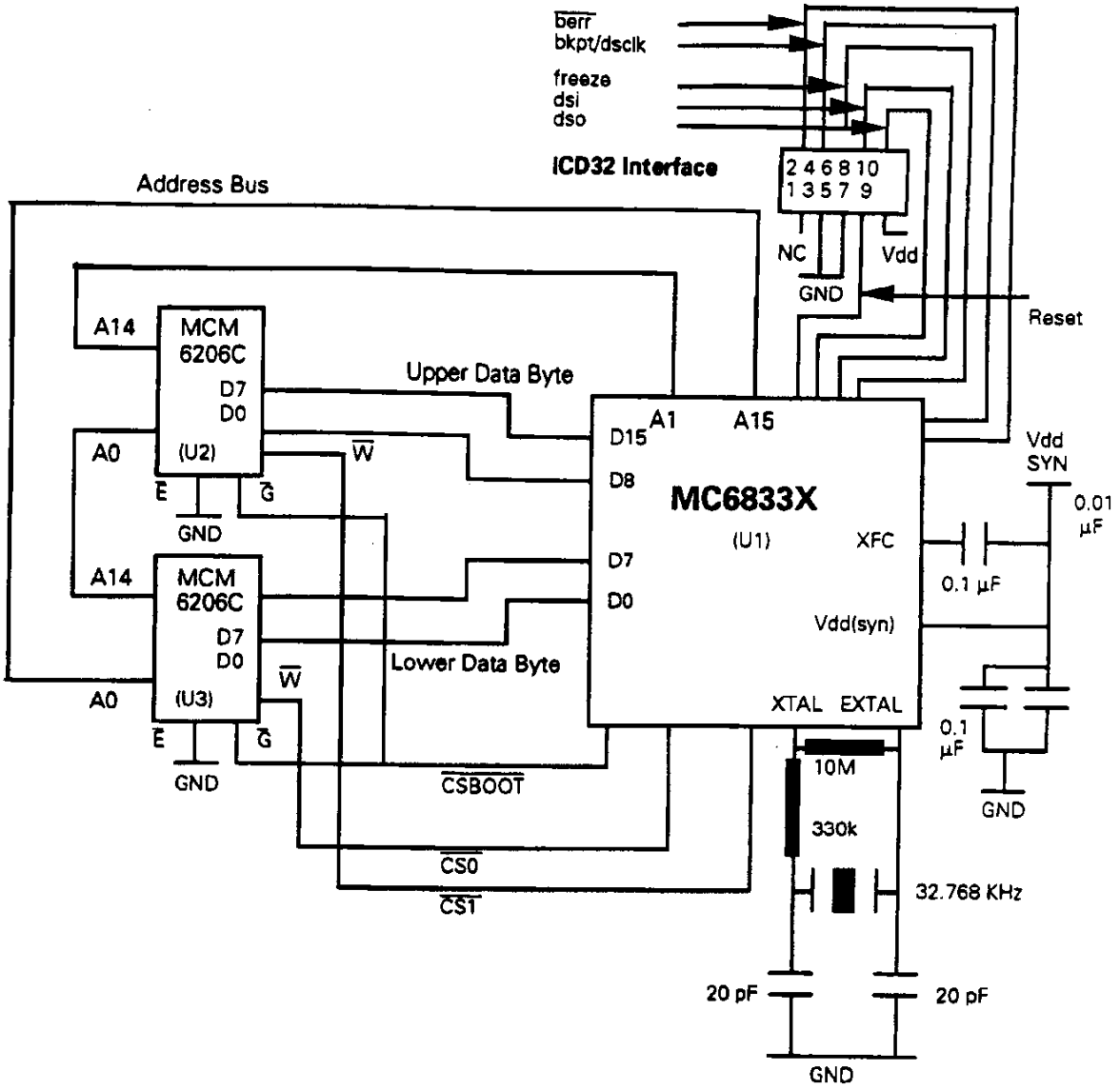


Figure 1. 6833X Minimum System to Support ICD32

A suggested startup routine for ICD32 is given in Appendix B. This Initialises the chip select registers to support the two cycle access to the RAM with a base address of $0000. It also sets the clock synthesiser for 16 MHz operation, disables the watchdog timer and sets the cpu registers. The stack pointer is set to $8000 and the program counter to $3000. A command is also shown to enable the onboard RAM of the 68332.

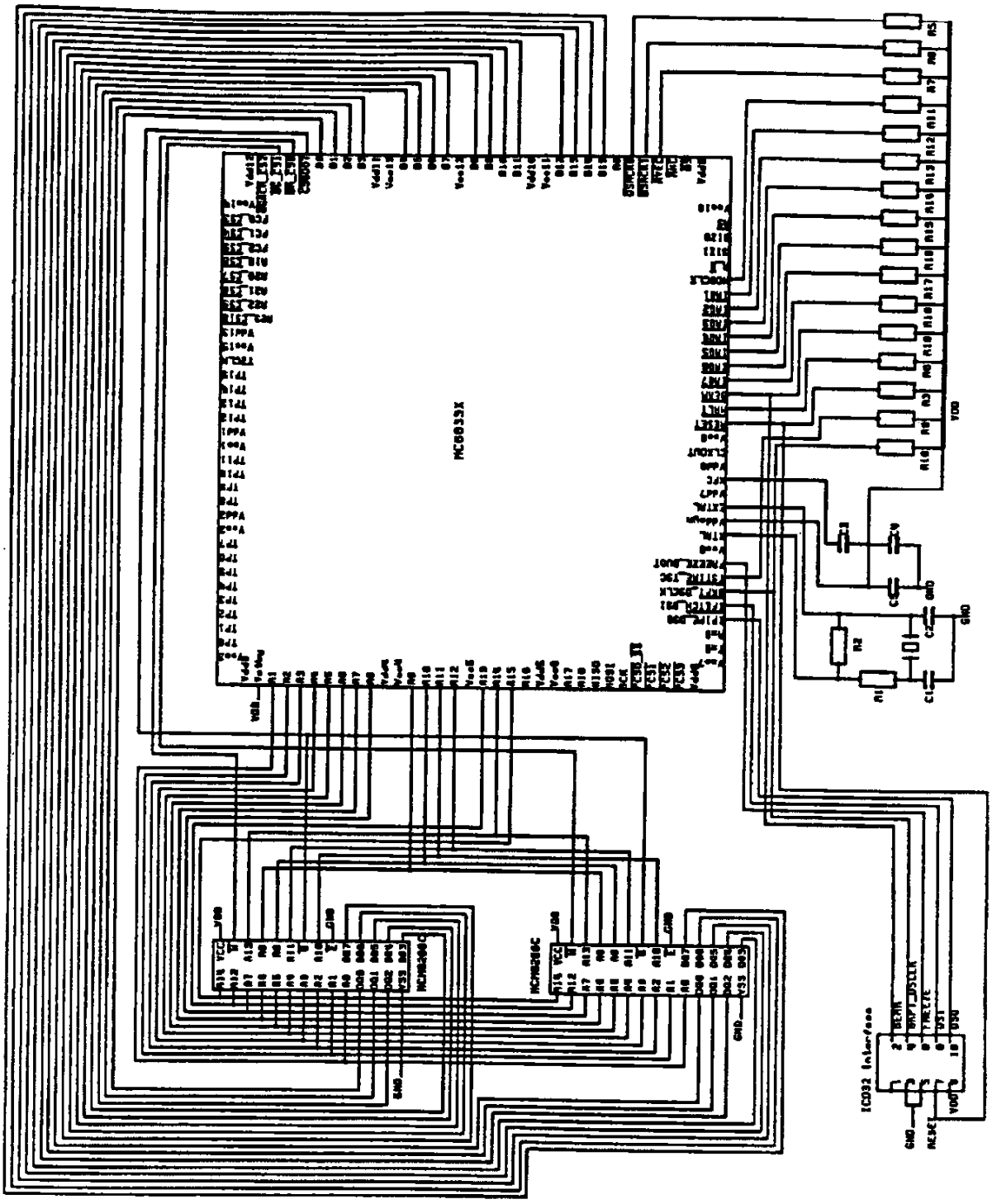
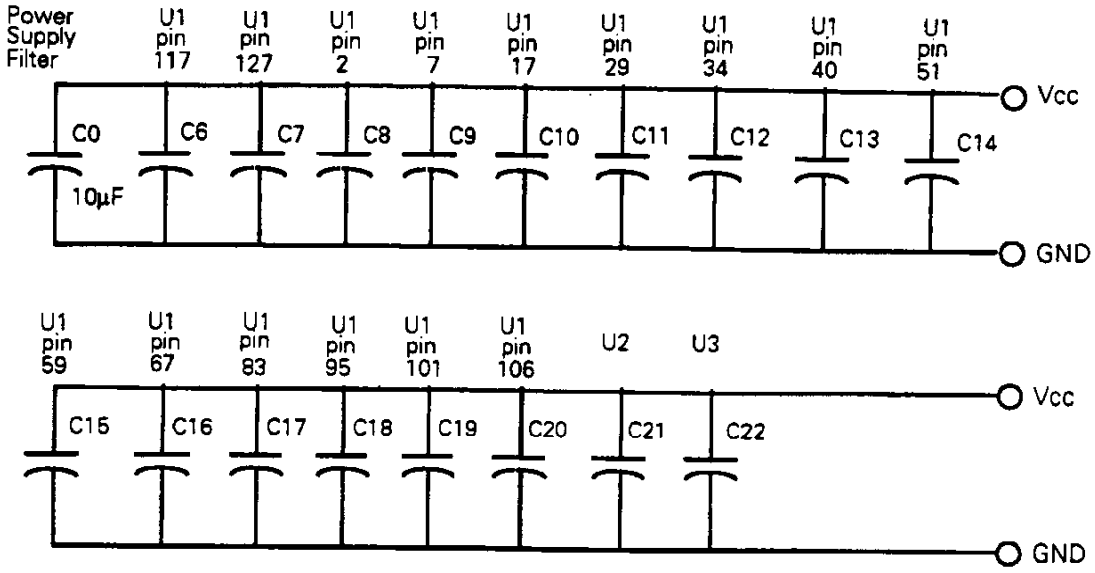


Figure 2. Circuit schematic

Decouple capacitors for ICs as labeled.

All capacitors from C6 to C22 are 0.1µF @ 50V.



Pull-up resistors are 1/8 watt, 5%.

R5-R19 — 5k	R3 (RESET) — R880

External clock circuit element

R1,R2 are 1/8 watt & 5%, caps are 50V.

R1	R2	C1,C2	C3,C4	C5
330k	10M	20pF	0.1µF	0.01µF

Figure 3. Power connections for MC68331/MC68332

Operating Notes:

1. When using *BD32* if there is no startup code in the evaluation RAM , (as is likely from power up), it is possible to enter a state where BD32 cannot get access to the processor. This is normally due to the processor picking up random reset vectors and jumping to non decoded memory where it does not receive an access termination signal such as $\overline{\text{DSACK}}$ or $\overline{\text{BERR}}$. The processor will then stall indefinitely at this address waiting for this signal. To force the part into BDM, manually assert $\overline{\text{BERR}}$.

   (Other support products have control of $\overline{\text{BERR}}$ and do not require this assistance.)

2. The watch-dog timers of the 68331 and 68332 are automatically enabled on reset of the processors. Although the watchdog is disabled whilst in background mode it becomes active when the users code is running. If the watchdog register is not polled in the user code, watchdog resets will occur. Disabling the watch-dog from BDM for the early stages of debugging can be helpful.

3. It is important that the pull-up resistor value used on the $\overline{\text{RESET}}$ pin is not increased from the 880 Ohms shown in the circuit diagram. The $\overline{\text{RESET}}$ pin is both an input and output and the pin is sampled after an internal reset such as the watch-dog or $\overline{\text{RESET}}$ instruction has occured. If the resistor is a high value and there is any appreciable capacitive loading on the pin, it is possible for the processor to recognise an additional external $\overline{\text{RESET}}$ due to the delay in the pin going high.

APPENDIX A — PRODUCTS SUPPORTING BDM

1. M68ICD32 — Assembly level full screen debugger
   Available from your Motorola Semiconductors Sales Office or Distributor
   or P+E Microcomputer Systems Inc.
   (PC only)

2. BD32 — Assembly level line Debugger
   Freeware Debugger
   Available from your Motorola Semiconductors Sales Office or Distributor
   (PC only)

3. EST 300 — Assembly level debugger with built in simulator and performance analysis options.
   Can be used to support C source level debug with Xray from Microtech or
   XDB from Intermetrics.
   Supplied by Embedded Support Tools Inc., Massachusetts.
   (PC, SUN, Apollo)

4. CADS — ADA source code debugger.
   Supplied by A.D.A. Ltd , Maidenhead, England.

APPENDIX B — SUGGESTED STARTUP MACRO FOR ICD32

```
Startup.icd
d0 0
d1 0
d2 0
d3 0
d4 0
d5 0
d6 0
d7 0

a0 0
a1 0
a2 0
a3 0
a4 0
a5 0
a6 0
a7 8000                          Sets stack pointer.
PC 3000                          Sets program counter.
CODE 3000                        Initialises code window
WATCHDOG                         Disables watchdog timer.

mm.w     fffa48   0003           [
mm.w     fffa4a   6bb0
mm.w     fffa4c   0003           Initialisation of Chip Selects.
mm.w     fffa4e   33b0
mm.w     fffa50   0003
mm.w     fffa52   53b0           ]
mm.w     fffa04   7f00           Set frequency to 16MHz.
mm.w     fffb04   1000           Enable on-chip RAM (* 332 Only).
```