Freescale Semiconductor
Application Note

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Features of Voltage Regulators in the MMPF0100

1 Introduction

The PF0100 is a Freescale's Power Management IC (PMIC) that targets application processors using the ARM(TM) Cortex-A9 core. It integrates a total of 14 regulators. While the PF0100 is an optimum choice because its flexibility allows it to be used in a wide variety of other systems.

In this application note, we will take an in-depth look at the different voltage regulators, both switching and linear, in the PF0100. This will enable the reader to develop a deeper understanding of the PMIC and help choose an optimal way to use the part in their system.

Freescale analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic together on a single cost-effective die.

2 Overview

The PF0100 integrates six buck regulators, six general purpose LDO regulators, a DDR reference, and an always-ON RTC supply. Figure 1 shows a high-level block diagram of the PMIC.The PF0100 works from an input voltage of 2.8 V to 4.5 V.

Contents

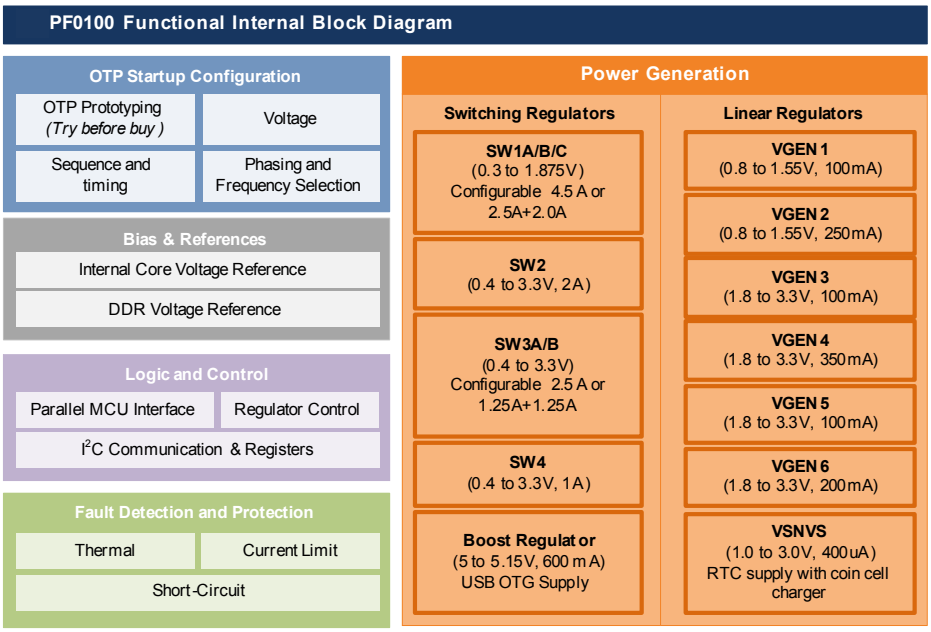

Figure 1. PF0100 Block Diagram

A key feature of PF0100 is its One-time-programmable (OTP) memory. OTP allows key startup parameters such as output voltage, startup sequence, startup slew rate, and regulator configuration to be programmed into the part. This enables the PF0100 to lend itself as the PMIC of choice for a variety of applications.

3 Buck Regulators in the PF0100

A buck regulator is a step-down DC to DC converter. It uses two switches to create a pulse width modulated signal with a magnitude equal to the input voltage. This signal is filtered by an LC filter to create a DC output voltage. The DC output voltage is duty cycle times the amplitude of the pulses (input voltage in this case). Figure 2 shows an overview of a buck regulator converting an input voltage of 3.3 V to an output voltage of 1.1 V. The PWM controller adjusts the duty cycle of the pulses to keep output voltage within regulation.

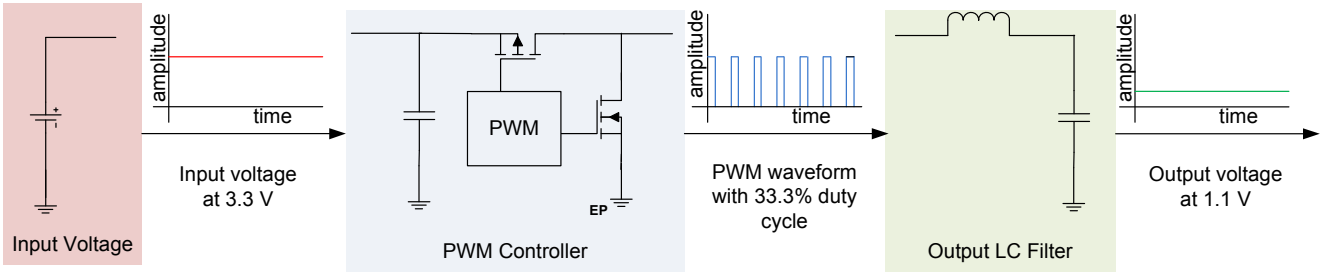

Figure 2. Overview of a Buck Regulator

There are six such individual buck regulators in the PF0100. Table 1 gives a breakdown of the current and voltage capability of the regulators. Output voltage and sequence of these regulators can be set and controlled individually.

Table 1. Six Independent Buck Regulators in the PF0100

Regulator Name	Output Voltage Range	DC Load Current Capability
SW1AB	0.3 to 1.875 V	2.5 A
SW1C	0.3 to 1.875 V	2.0 A
SW2	0.4 to 3.3 V	2.0 A
SW3A	0.4 to 3.3 V	1.25 A
SW3B	0.4 to 3.3 V	1.25 A
SW4	0.4 to 3.3 V	1.0 A

Flexibility of the PF0100 allows certain regulators listed in Table 1 to be combined to give a single regulator of higher output current. Table 2 gives breakdown of a configuration that gives a total of four regulators. SW1AB and SW1C are combined to give a single 4.5 A regulator, namely, the SW1ABC. Similarly SW3A and SW3B, each rated at 1.25 A, are combined to give a single 2.5 A regulator, the SW3AB.

Table 2. Four Independent Buck Regulators in the PF0100

Regulator Name	Output Voltage Range	DC Load Current Capability
SW1ABC	0.3 to 1.875 V	4.5 A
SW2	0.4 to 3.3 V	2.0 A
SW3AB	0.4 to 3.3 V	2.5 A
SW4	0.4 to 3.3 V	1.0 A

SW1AB and SW1C can be combined independent of SW3A and SW3B and vice versa. Hence it is possible to achieve a total of five independent regulators as well. Table 3 and Table 4 give a breakdown of those configurations.

Table 3. Five Independent Buck Regulators in the PF0100 - Option 1

Regulator Name	Output Voltage Range	DC Load Current Capability
SW1ABC	0.3 to 1.875 V	4.5 A
SW2	0.4 to 3.3 V	2.0 A
SW3A	0.4 to 3.3 V	1.25 A
SW3B	0.4 to 3.3 V	1.25 A
SW4	0.4 to 3.3 V	1.0 A

Table 4. Five Independent Buck Regulators in the PF0100 - Option 2

Regulator Name	Output Voltage Range	DC Load Current Capability
SW1AB	0.3 to 1.875 V	2.5 A
SW1C	0.3 to 1.875 V	2.0 A
SW2	0.4 to 3.3 V	2.0 A
SW3AB	0.4 to 3.3 V	2.5 A
SW4	0.4 to 3.3 V	1.0 A

To see circuit connections for the different configurations, refer to the MMPF0100 datasheet.

4 PF0100 Buck Regulator Features

4.1 Phase Interleaving

As shown in Figure 2, a buck converter uses two MOSFETs to convert the input voltage to a pulse width modulated waveform, which is filtered by the output LC filter. This type of operation results in high input harmonic distortion for two reasons:

1. High di/dt through the top MOSFET as it turns on
2. When the top MOSFET is fully turned on, the inductor current rises (governed by V_{IN}-V_{OUT} and the inductor value) thus discharging the input capacitor

The DC inductor current is equal to the load current. During each switching period, inductor current transitions from the bottom MOSFET to the top MOSFET when the former turns off and the latter turns on. Due to the fast turn on of the top MOSFET, inductor current transitions to the top MOSFET in very short time resulting in high dI/dt through it. This high dI/dt is buffered by the input capacitor which discharges as a result. Additionally, after the top MOSFET fully turns on, the inductor is charged from the input as its current rises and it stores energy to provide to the output. The net effect is seen as noise and ripple on the input supply.

In a multi-regulator PMIC such as the PF0100, the input noise can be significant if the top MOSFET of all the regulators turn on simultaneously. A large number of input capacitors would be required to filter the noise thus created. To prevent this, the PF0100 automatically interleaves switching of the different regulators.

Figure 3 shows the default phase node waveforms of SW1AB, SW2, SW3AB, and SW4. It is seen that the waveforms are phase-shifted, thus reducing the overall amplitude of input noise and ripple.

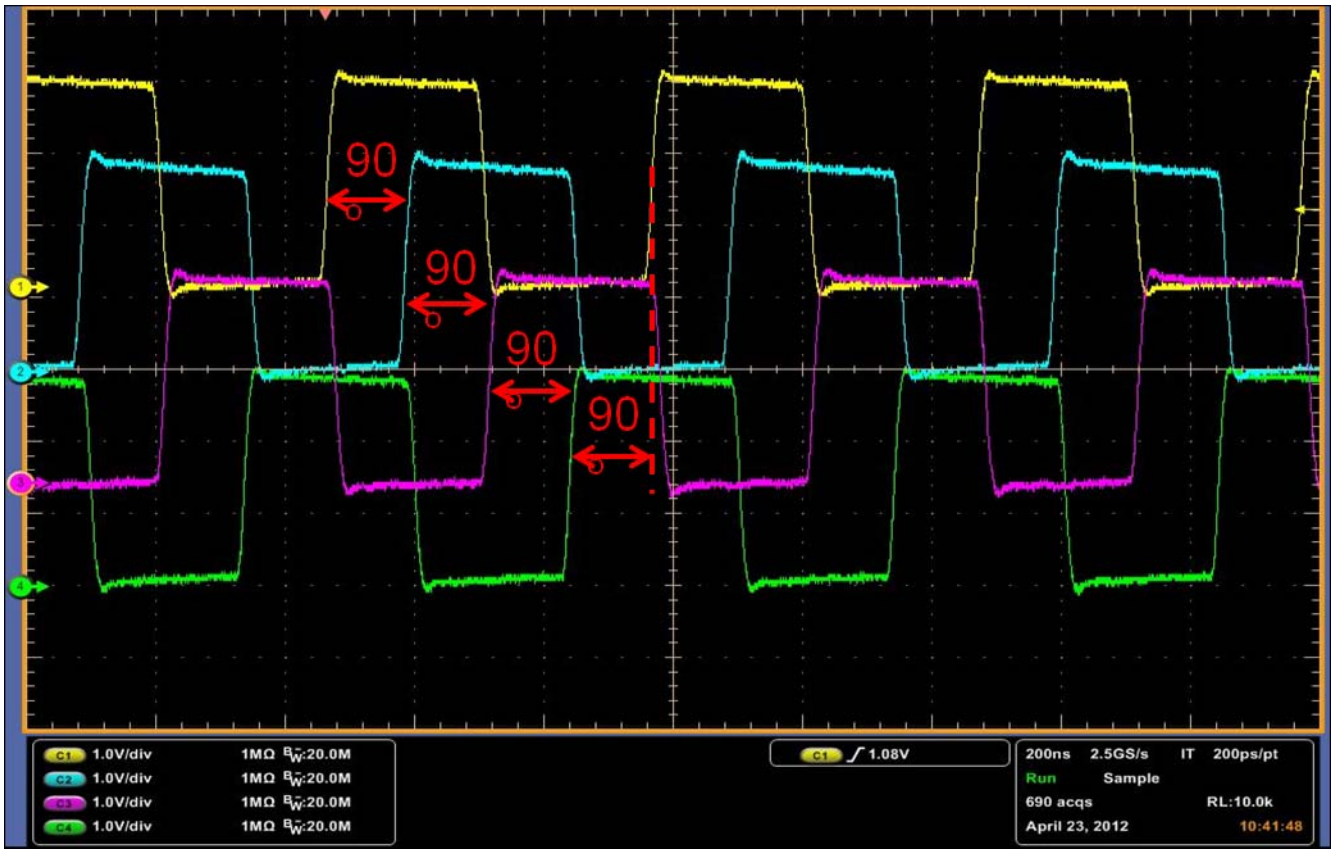

Figure 3. Interleaving of Buck Regulators

Phase-shifting between the regulators is also controllable with I^2C by writing to the SWxPHASE[1:0] bits. This is useful when load currents are not equally distributed in the regulators. Software can change the SWxPHASE[1:0] setting during different modes of operation of the system to get to optimal phasing for each.

4.2 Switching Modes

There are four major losses associated with the MOSFETs in a buck converter:

1. Conduction losses due to the $R_{DS(ON)}$ of the MOSFETs
2. Switching losses that occur as inductor current transitions from the bottom MOSFET to the top MOSFET
3. Gate drive losses required to turn-on and turn-off the MOSFETs
4. Body diode losses due to inductor current flowing through the bottom MOSFET's body diode

Conduction, switching, and body diode losses are significant during heavy load operation. Gate drive and body diode losses are significant during light load operation. The PF0100 employs different modes of switching to maximize efficiency across the entire load range.

4.2.1 Pulse Width Modulation (PWM)

The traditional mode of switching in a buck regulator is Pulse Width Modulation (PWM). In PWM mode, there are continuous pulses generated by the MOSFETs irrespective of the load current. While it is the preferred mode of switching at higher load currents, its efficiency at light loads is poor. This is mainly due to quiescent current required to provide the gate drive for the continually switching MOSFETs. At light load currents, the ratio of power supplied to the load to the power required to drive the gates is low. While PWM has the drawback of low efficiency at low load currents, it is advantageous in providing the fastest transient response as well as limiting the switching noise to a certain spectrum.

4.2.2 Pulse Frequency Modulation (PFM)

To avoid the high losses associated with light load operation in PWM mode, Pulse Frequency Modulation (PFM) is used. In the PFM mode, switching frequency is approximately proportional to the load current. This way, at light load conditions, the gate drive losses are reduced and efficiency is increased. Further, the PF0100 uses a circuit to calculate inductor current flow and turns off the bottom MOSFET if the inductor current goes negative. This prevents discharge of the output capacitor due to negative inductor current. These two features help provide efficiency as high as 90% at load currents as low as 100 µA. Figure 4 shows a block diagram of the PFM operation in the PF0100 as well as associated waveforms.

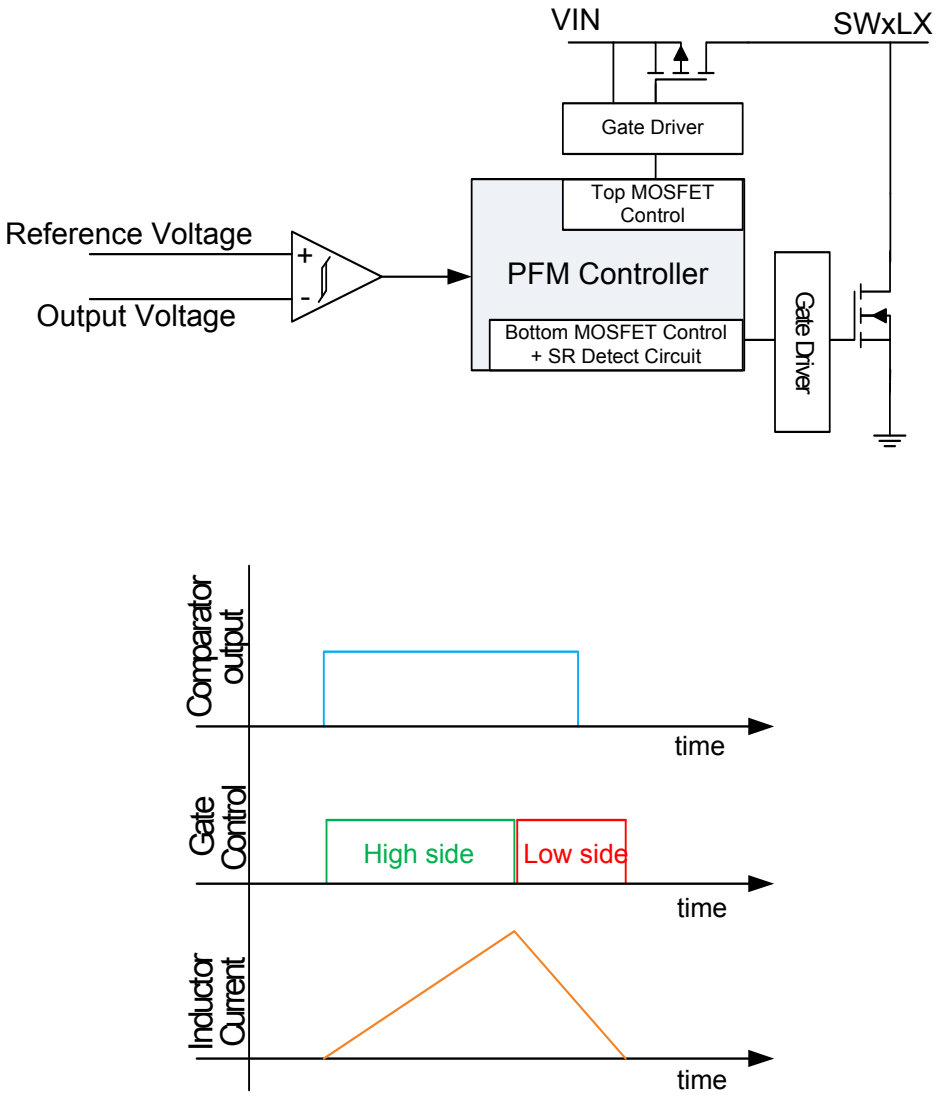

Figure 4. PFM Operation Block Diagram and Associated Waveforms

A hysteretic comparator compares the output voltage to an internal reference voltage. When the output voltage falls below the reference voltage, the top MOSFET is turned on for a fixed on-time to charge the output capacitor. After the top MOSFET turns off, the bottom MOSFET is turned on to provide a path for the inductor current. An internal circuit predicts zero crossing of the inductor current and turns off the bottom MOSFET, thus preventing inductor current from going negative and discharging the output capacitor.

A drawback of PFM mode is that at high load currents, the frequency of switching can become very high, thus leading to lower efficiency. It is recommended to use the PFM mode of operation for load currents lower than 100 mA. For higher load currents, PWM or APS mode of switching is recommended.

4.2.3 Auto Pulse Skip Mode (APS)

APS is the default mode of switching in the PF0100. All the regulators come up in APS mode after a turn-on event. The mode of operation can then be changed in software. It is also possible to set the switching mode to either PFM or PWM and then turn on the regulators.

APS mode offers a good compromise between PFM and PWM operation. At light load currents it offers higher efficiency than PWM mode, but in most cases, lower efficiency than PFM mode. At higher load currents, switching automatically transitions to PWM mode.

In the APS mode, the top MOSFET is turned on for a fixed on time whenever output voltage falls below the reference voltage. A circuit monitors the inductor current and whenever it detects negative inductor current, the bottom MOSFET is turned off thus preventing discharge of the output capacitor. This is also advantageous in avoiding turn-on switching losses the next time the top MOSFET turns on. If the output voltage goes above the reference voltage and remains so during the next clock cycle, the switching pulses are *skipped,* thus preventing switching and gate drive losses. When the circuit does not detect zero-crossing of the inductor in consecutive cycles, switching automatically transitions to PWM. Load transient response in the APS mode is comparable to that in the PWM mode.

4.3 Current Limit Protection

An inherent advantage of a buck regulator is that in the event of an overload or short-circuit on the output, the top MOSFET can be turned off, thus limiting the current available to the load.

In the PF0100, current through the top MOSFET is monitored every switching cycle. Whenever the top MOSFET current goes above a set threshold, the gate pulse is terminated thus limiting the inductor current from going to dangerous levels.

By default the current limit threshold is set to two times the rated current of the regulator. It can be changed to 1.5 times by setting the SWxILIM bit associated with individual regulators.

If the current limit comparator is tripped continually for 8.0 ms, the SWxFAULTI interrupt bit associated with the regulator is set. If the interrupt is unmasked, the INTB pin is pulled low. There is also a programmable ‘Power Good’ mode wherein the RESETBMCU pin is pulled low in the event of a current limit fault.

4.4 Power Stage Control

Generally, the buck regulator inductor is chosen to be able to withstand currents at least up to the current limit of the regulator. In the PF0100, the power MOSFETs are composed of smaller MOSFET stages connected in parallel. For applications not requiring the rated load current of a particular regulator, the size of the MOSFET effectively switching can be reduced by disconnecting a percentage of the MOSFET stages.

Reducing the power stages also reduces the current limit proportionally thus allowing use of smaller inductors. For example, SW2 is rated for 2.0 A and has a default inductor current limit of 4.0 A. By setting the SW2_PWRSTG[2:0] bits to 011, 25% of the MOSFETs are disconnected thus reducing the current rating of the regulator to 1.5 A and reducing the inductor current limit to 3.0 A.

Reducing the power stages also reduces the gate drive losses associated with the switching MOSFETs. Efficiency at light loads can be increased if software automatically reduces the effective power stages for low power modes, such as Sleep and Standby, of the system.

4.5 Dynamic Voltage Scaling (DVS)

In traditional buck regulators, output voltage is set by using a resistor divider to generate a voltage, which is compared to a fixed reference voltage. When the ratio of the resistor divider changes, the output voltage changes to keep the divided voltage equal to the reference voltage. This approach is disadvantageous for two reasons:

1. current is consumed by the resistor divider which can become significant during light load operation

2. loop gain of the regulator is different for different output voltages, thus affecting stability of the regulator

Often additional load capacitors and capacitors in parallel to these resistors are added to maintain stability.

The PF0100 uses a different approach to set the output voltage: the reference is varied directly for different output voltage settings. This avoids the use of lossy resistors and loop gain of the regulator does not change with output voltage, thus requiring no additional components. External component selection is very simple in the PF0100.

Figure 5 shows a high level comparison of the two approaches. Often, the resistor divider and compensation capacitors in parallel to them significantly increase the overall component count when using discrete regulators.

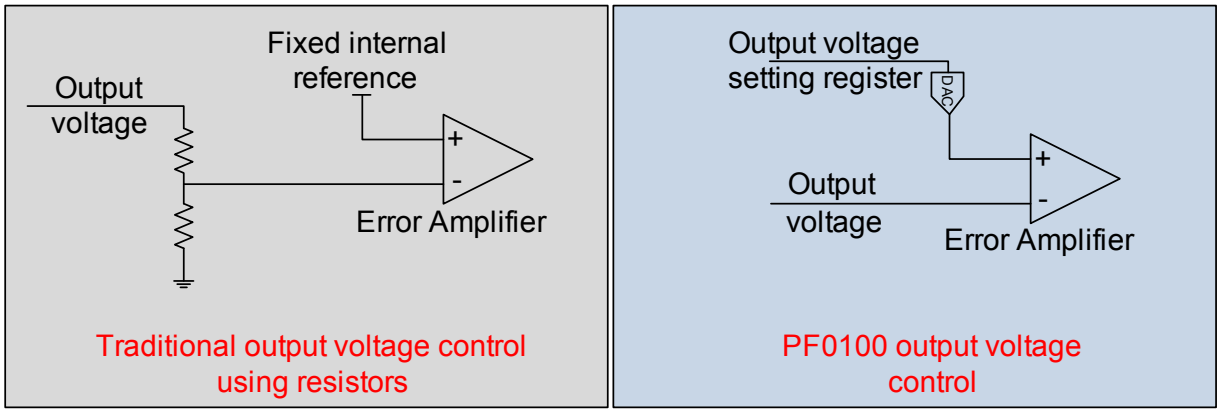

Figure 5. Output Voltage Control - Traditional Versus PF0100

One obvious advantage when using a digital to analog converter (DAC) to control the reference voltage is that transition of output voltage from one level to another can be precisely controlled without any external components.

Systems use lower core voltages when entering low power modes, such as Sleep and Standby to reduce overall power consumption. When using discrete regulators, an additional MOSFET in series with a resistor is required to change the effective resistor divider ratio. Not only are additional components required, but the slew rate of the output voltage cannot be controlled and is often limited by the inductor current limit.

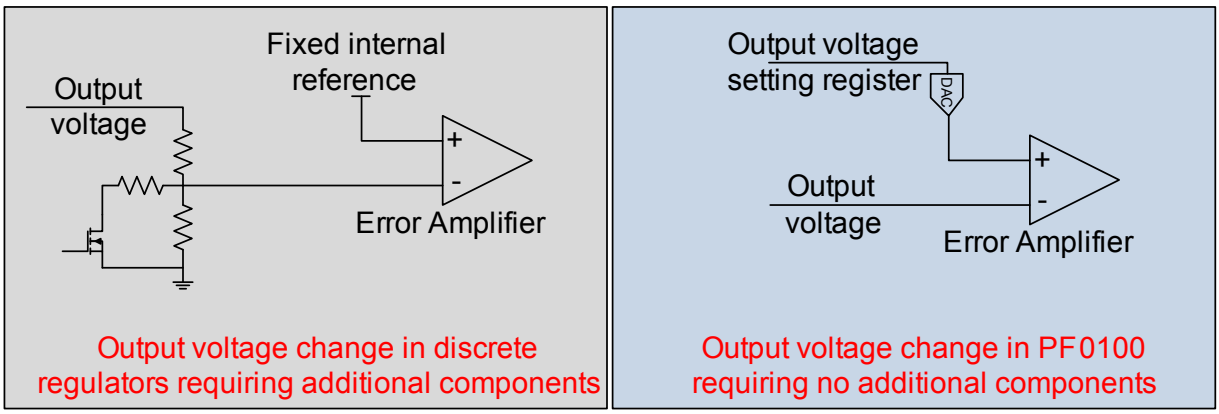

Figure 6. Output Voltage Transition - Discrete Versus PF0100

In the PF0100, to change output voltage from level to another, the output voltage register associated with each regulator has to be changed. Internal circuitry steps the DAC output from the old level to the new level in controlled steps. The rate of change of output voltage can be precisely controlled by using the SWxDVSSPEED[1:0] bits. Figure 6 shows a comparison of the two approaches. Figure 7 shows an example of how the PF0100 responds to a voltage change request.

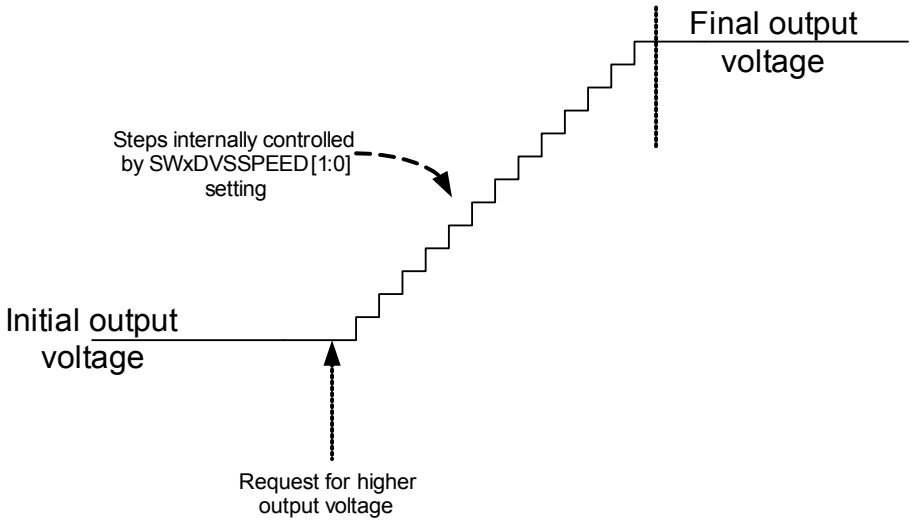

Figure 7. PF0100 Output Voltage Change Response

4.6 Switching Frequency Margining

Certain applications have strict EMC requirements. Standards place limits on electromagnetic emissions at certain frequencies. To support applications having this requirement, PF0100 allows software to margin the switching frequency to allow systems to move away from sensitive bands. Switching frequency of the PF0100 is derived from a master 16 MHz clock which is divided down to achieve 1.0 MHz, 2.0 MHz (default), or 4.0 MHz. Software can margin the 16 MHz clock thus changing the chosen switching frequency proportionally. The 16 MHz clock can be changed to between 12 MHz and 20 MHz in steps of 250 kHz.

4.7 VTT Tracking Mode

The SW4 regulator can be used in a VTT tracking mode for DDR memory termination. In this mode, the SW4 output voltage automatically tracks half of SW3A output voltage (which would be used to provide VCC for the DDR). In this mode SW4 works only in the PWM mode to enable it to source or sink load current. By default SW4 is in a standard regulator mode. It can be set to VTT tracking mode via OTP.

4.8 Turn-off Pull-down Resistor

All the buck regulators have an internal 500 ohm resistor in series with a switch at the SWxFB pins. When a regulator is enabled (ON), its associated switch is open thus the resistor is disconnected. When the regulator is turned OFF, the switch closes thus connecting the resistor across the output capacitors. This helps in discharging the output capacitors quickly during a turn-off event and prevents intermediate voltages at the load when off.

5 Linear Regulators in PF0100

5.1 VGEN1 – VGEN6 LDO Regulators

There are six general purpose LDO regulators in the PF0100. Table 5 gives a breakdown of the voltage and current ratings of each.

Table 5. General Purpose LDO Regulators in the PF0100

LDO Regulator	Maximum Input Voltage	Output Voltage Range	Maximum Load Current
VGEN1	3.4 V	0.8 to 1.55 V in 50 mV steps	100 mA
VGEN2		0.8 to 1.55 V in 50 mV steps	250 mA
VGEN3	3.6 V	1.8 to 3.3 V in 100 mV steps	100 mA
VGEN4		1.8 to 3.3 V in 100 mV steps	350 mA
VGEN5	4.5 V	1.8 to 3.3 V in 100 mV steps	100 mA
VGEN6		1.8 to 3.3 V in 100 mV steps	200 mA

These regulators are straightforward to work with. Their output voltage can be set via OTP and changed via I^2C. Slew rate of startup and subsequent output voltage changes are internally controlled.

All the regulators have in-built current limit protection. When load current tries to go above the current limit protection threshold (typically approximately 1.6 times the rated current), the regulators enter a constant current mode, thus limiting the amount of current available to the load. Corresponding interrupt bits are set to notify the processor. Additionally, when the REGSCPEN bit is set and a regulator enters current limit protection, it is disabled.

5.2 VREFDDR Voltage Reference

VREFDDR is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then utilizes a voltage follower to drive the load. Figure 8 shows a block diagram of VREFDDR.

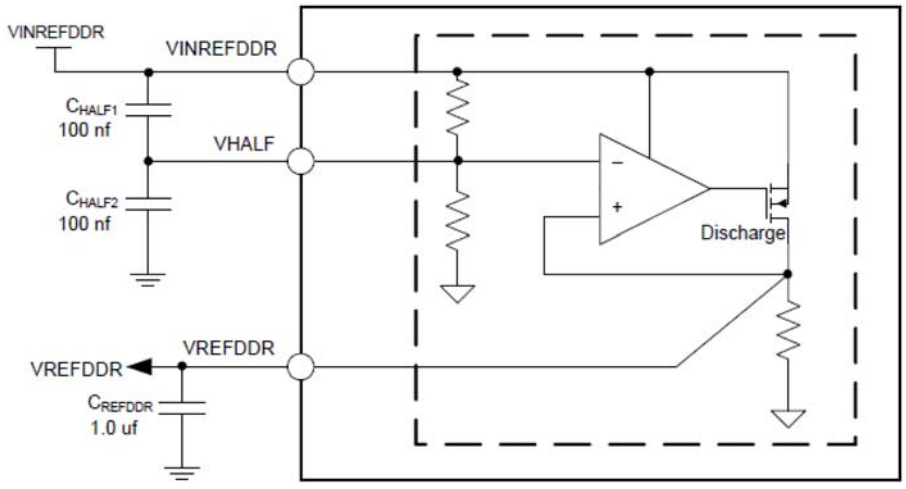

Figure 8. VREFDDR Block Diagram

5.3 VSNVS Switch/LDO

VSNVS is an always-on LDO regulator that can either be powered by VIN or by a coin cell. Its output voltage can be set to 1.0 V, 1.1 V, 1.2 V, 1.3 V, 1.5 V, 1.8 V, or 3.0 V via OTP. When set to 3.0 V, the regulator acts as a switch when powered only by a coin cell. For other output settings, the regulator acts as an LDO when powered only by a coin cell.

VSNVS is generally used to power the Real Time Clock (RTC) block in a processor. It can also be used to power a standalone RTC. Figure 9 shows the block diagram of VSNVS.

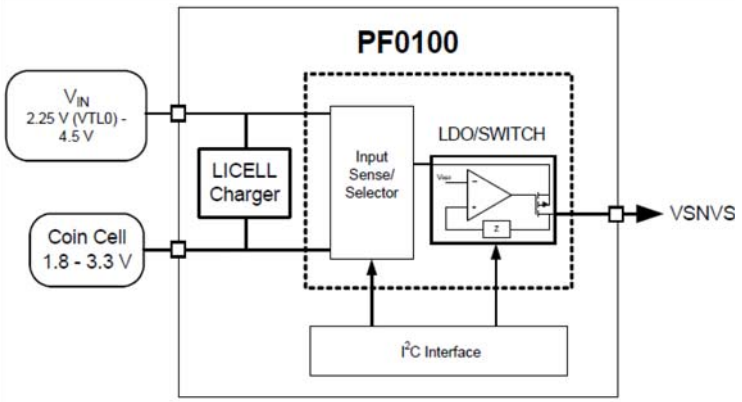

Figure 9. VSNVS Block Diagram

6 Conclusion

The PF0100 offers 14 high performance voltage regulators in a single package. All the regulators are internally compensated. Startup, slew rate control and DVS are internally controlled thus providing a power management solution requiring minimal external components. Its flexibility and configurability make it suitable to power a wide variety of systems.

7 References

Following are URLs where you can obtain information on related Freescale products and application solutions:

Document Number and Description		URL
MMPF0100	Data Sheet	www.freescale.com/files/analog/doc/data_sheet/MMPF0100.pdf
Freescale.com Support Pages		**URL**
MMPF0100 Product Summary Page		http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MMPF0100
Power Management Home Page		http://www.freescale.com/PMIC
Analog Home Page		http://www.freescale.com/analog

8 Revision History

Revision	Date	Description
1.0	5/2013	• Initial release
	2/2014	• Removed an object covering text content.

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