Freescale Semiconductor
Application Note

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Differences Between P4080 Rev. 2 and P4080 Rev. 3

About this document

This document describes the differences between P4080 QorIQ integrated multicore communication processor silicon revision 2 and revision 3. Rev. 3 features many improvements and fixes to many Rev. 2 errata. See *P4080 Chip Errata* (P4080CE) for the most up-to-date information on these errata.

The P4080 reference manual (P4080RM) describes the functionality of both Rev. 2 and Rev. 3 of the chip.

Some P4080 development systems that were shipped to alpha customers and third party tool developers were originally populated with Rev. 1 parts. Most of these have been upgraded to Rev. 2 parts.

NOTE

P4080 Rev. 1 is not documented in this application note.

Contents

1 Memory map

There are no significant differences between the memory maps of Rev. 2 and Rev. 3. However, the memory maps of specific IP modules may differ as noted in their respective sections of this document.

2 Signals

Table 1. Signal differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
SerDes register—BnTTLCRn0	Reset value for lanes configured as SGMII, SRIO, XAUI, and Aurora (all non-PCI Express protocols) is: 00**01**_**1000**_0000_0000_ 0**0**00_0000_0000_0000b	for lanes configured as SGMII, SRIO, XAUI, and Aurora (all non-PCI Express protocols) is: 00**00**_**0011**_0000_0000_ 0**1**00_0000_0000_0000b

3 Reset, clocking, and initialization

There are no significant differences.

4 Pre-boot loader

There are no significant differences.

5 Secure boot and Trust Architecture

There are no significant differences.

6 e500mc core

Table 2. e500mc differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Processor version register (PVR)	8023_0020h	8023_0031h
System version register (SVR)	• P4080 with security: 8208_0020h • P4080 no security: 8200_0020h • P4040 with security: 8209_0020h • P4040 no security: 8201_0020h	• P4080 with security: 8208_0030h • P4080 no security: 8200_0030h • P4040 with security: 8209_0030h • P4040 no security: 8201_0030h

Table 2. e500mc differences (continued)

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Performance monitor—Event counts when using the PMLCax[EVENT] field and the corresponding counter, PMCx, is not frozen.	The following event counts are inaccurate: • Event 16—The number of branches in the BTB mispredicted due to direction prediction are not counted correctly. • Event 73—The snoop hit event only counts snoop hits in the cast out buffers, the line fill buffers, and the L1 Data cache. It does not count snoop hits in the L1 cast away and Backside-L2. • Event 126—The L2 castout event only counts castouts from the DLFB. It does not count cast outs from the Backside L2 as expected.	The event counts are now accurate.
Performance monitor—Performance monitor counter set up to count during user mode (PMLCax[FCS]=1, MSR[PR]=1)	The following events (PMLCal[EVENT]) are not counted: • Event 86—Interrupts taken • Event 87—External input interrupts taken • Event 88—Critical input interrupts taken • Event 89—System call and trap interrupts	The events are now counted properly.
Local Control A Registers (PMLCa0–PMLCa3/UPMLCa0–UPMLCa3) allow freezing the PM counters in guest state (FCGS1) and in hypervisor state (FCGS0). See the *e500mc Core Reference Manual* for more information.	The FCGS0/FCGS1 fields are not implemented on the core used on P4080 Rev 2.	The FCGS0/FCGS1 fields are implemented on the core used on P4080 Rev 2.
Extended External Debug Control Register 0 forced halt (EEDCR0[forced_halt]). See the *e500mc Core Reference Manual* for more information.	This field is not implemented on the core used on P4080 Rev 2.	This field is implemented on the core used on P4080 Rev 3.

Table 2. e500mc differences (continued)

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
External debug mode (EDM)—instuction address compare (IAC) and data address compare (DAC) watchpoint events . See the *e500mc Core Reference Manual* for more information.	On the core used on P4080 Rev 2, IACs and DACs that cause halts in EDM mode will not trigger watchpoints.	On the core used on P4080 Rev 3, IACs and DACs that cause halts in EDM mode will trigger watchpoints.
e500mc core performance monitor events: • Com:68 BIU master global requests • Com:69 BIU master data-side requests • Com:70 BIU number of stash requests received • Com:71 BIU number of stash accepts • Com:74 Snoop pushes • Com:75 Snoop sharing See the *e500mc Core Reference Manual* for more information.	Not supported on the core used on P4080 Rev 2.	Supported on the core used on P4080 Rev 3.

7 CoreNet platform cache (CPC)

There are no significant differences.

8 CoreNet coherency fabric (CCF)

Table 3. CCF Differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Procedure to ensure resources exist for upstream transactions (workaround for erratum GEN A-004849). **Note:** Special conditions are required to perform these writes correctly. See application note *Reconfiguring the CoreNet Coherency Fabric for A-004849* (AN4571) for details.	Last step is to write 0000_001**2**h to DCSR at offset 0B_0108h.	Last step is to write 0000_001**C**h to DCSR at offset 0B_0108h.

9 Peripheral access management unit (PAMU)

There are no significant differences.

10 DDR memory controllers

There are no significant differences.

11 I2C modules

There are no significant differences.

12 Enhanced local bus controller (eLBC)

There are no significant differences.

13 Enhanced serial peripheral interface (eSPI)

There are no significant differences.

14 Enhanced secure digital host controller (eSDHC)

Table 4. eSDHC differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Host Capabilities Register (HOSTCAPBLT)	Reset value is 07F3_0000h, falsely indicating that the chip supports 1.8 V, 3.0 V, suspend/resume, and advanced DMA capabilities, when, in fact, it does not support these capabilities.	Reset value is 0163_0000h, correctly indicating that the chip does not support 1.8 V, 3.0 V, suspend/resume, and advanced DMA capabilities.

15 Universal serial bus interface (USB)

Table 5. USB differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Programmable burst size (USBx_BURSTSIZE[TXPBURST, RXPBURST])	TXPBURST and RXPBURST are effectively write-only fields. The actual value written in the register is used correctly for the burst length, but the fields always return 10h when read.	TXPBURST and RXPBURST are R/W fields. When read, they return the true value that was last written.

Table 5. USB differences (continued)

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Queue head transfer overlay	In host mode, the NAK counter is decremented after receiving a NYET to an OUT Token. Thus, the NAK counter may be lower than expected.	In host mode, the NAK counter is not decremented after receiving a NYET to an OUT Token. Thus, the NAK counter more accurately reflects the actual count.
Isochronous endpoint operation model	When the USB controller is in device mode and the host sends two consecutive ISO OUT transactions (for example: OUT - DATA0 - OUT - DATA1) with a short inter-packet delay between DATA0 and the second OUT (less than 200 ns), the device sees the DATA1 packet as a short-packet even if it is correctly formed. In this case, the device terminates the transfer, generating an IOC interrupt (USBSTS[UI]). Note however, that DATA0 is correctly received.	The device correctly handles consecutive ISO OUT transactions.

16 DUART

There are no significant differences.

17 PCI Express interface controller

Table 6. PCI Express dfferences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
End-to-end CRC (ECRC) error checking support	End-to-end CRC (ECRC) errors on packets may not be detected even if ECRC checking is enabled. Therefore, ECRC checking should be disabled by clearing the ECRC checking enable bit (Advanced_Error_Capabilities_and_Control_Register[ECRCCE] = 0). This does not affect the ability of the device to properly detect and respond to link-level CRC (LCRC) errors.	End-to-end CRC (ECRC) errors on packets are detected properly. Therefore, ECRC checking may be enabled (Advanced_Error_Capabilities_and_Control_Register[ECRCCE] = 1) if desired.

18 Serial RapidIO interface

There are no significant differences.

19 DMA controllers

There are no significant differences.

20 Multicore programmable interrupt controller (MPIC)

Table 7. MPIC differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Multicasting external interrupts	Edge-triggered external interrupts can only be sent to a single destination.	Edge-triggered external interrupts can be sent to multiple destinations (multicast).
IP Block Revision Register 1 (BRR1)	0040_0401h	0040_0402h
Feature Reporting Register—FRR[NIRQ]	Reset value is 000_1111_1011b (0FBh). This is an inflated value in relation to the actualy number of interrupts.	Reset value is 000_1100_0011b (0C3h). This is a more realistic value for the number of interrupts.
Interrupt summary registers (IRQSIESR*n*)	The IRQSIESR bit for internal interrupt n is **not** masked by IIVPR*n*[MSK] if IILR*n*[TGT] =I RQ_OUT_B or *sien*.	The IRQSIESR bit for internal interrupt n is masked by IIVPR*n*[MSK] if IILR*n*[TGT] = IRQ_OUT_B or *sien*.

21 Interrupt assignments

There are no significant differences.

22 General purpose I/O

There are no significant differences.

23 Device configuration and pin control

Table 8. Device config and pin control differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
Processor version register (PVR)	8023_0020h	8023_0031h
System version register (SVR)	P4080 with security: 8208_0020h P4080 no security: 8200_0020h P4040 with security: 8209_0020h P4040 no security: 8201_0020h	P4080 with security: 8208_0030h P4080 no security: 8200_0030h P4040 with security: 8209_0030h P4040 no security: 8201_0030h

24 Run control and power management (RCPM)

There are no significant differences.

25 Debug and performance monitoring

There are no significant differences.

26 Datapath processing subsystem

26.1 Data Path Accelleration Architecture (DPAA)

There are no significant differences between the DPAA overview summary of Rev. 2 and Rev. 3. However, specific DPAA modules may differ as noted in their respective sections of this document.

26.2 Queue Manager (QMan)

Table 9. QMan differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
QMan IP Revision Register 1 (QMAN_IP_REV_1)	0A01_0101h	0A01_0102h

26.3 Buffer Manager (BMan)

There are no significant differences.

26.4 Frame Manager (FMan)

There are no significant differences.

26.5 Data path three-speed Ethernet controller (dTSEC)

Table 10. dTSEC differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
1588 time-stamping in SGMII 10/100 mode	Not supported	Supported

26.6 10-Gigabit Ethernet media access controller

Table 11 describes differences in the 10GEC block.

Table 11. 10GEC Differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
10-gigabit Ethernet MAC Controller ID register (EC10G_ID)	0001_032Ch	0001_0330h

26.7 IEEE Std 1588™ timer module

There are no significant differences.

26.8 Security Engine (SEC)

Table 12. SEC differences

Feature/Function	P4080 Rev. 2	P4080 Rev. 3
SEC Version ID Register (SECVID)	0A10_0200h	0A10_0300h
INCL_SEQ_OUT field in the Job Ring Configuration Register	Not present	Added INCL_SEQ_OUT field in the Job Ring Configuration Register. If this bit is set to 1, entries in the Job Ring's Output Ring will include a 32-bit word indicating the number of bytes written out via SEQ STORE and SEQ FIFO STORE commands in this job.
PKHA CHA	Original version of the PKHA CHA	Changed to single-digit version of the PKHA CHA. Functionality is the same as the original PKHA.
swap_bytes function	Not present	swap_bytes function added to MATH command
MATH command	Original list of sources and destinations for the MATH command	Additional sources and destinations added to the MATH command
MATH command	DPOVRD register cannot be read or written using the MATH command	DPOVRD register can be read and written using the MATH command
MACsec Decapsulation PDB, FCS option	Not present	FCS option added to MACsec Decapsulation PDB
MOVE_LEN command	Not present	New MOVE_LEN command added
MOVE command	Original list of destinations for the MOVE command	Additional destinations added to the MOVE command
Job Ring debugging registers	Original arrangement of the Job Ring debugging registers	Job Ring debugging registers redefined
DECO debuggng registers	Original arrangement of the DECO debuggng registers	DECO debuggng registers redefined
JUMP command, subroutine call and subroutine return	Original four versions of the JUMP command	Added subroutine call and subroutine return versions of the JUMP command
Shared Descriptor Header, read input frame (RIF) option	Shared Descriptor Header does not have an RIF field	Added RIF (Read Input Frame) option to the Shared Descriptor Header

26.9 Pattern Matching Engine (PME)

There are no significant differences.

27 Revision History

This table provides a revision history for this application note.

Table 13. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	08/2014	Section 2, “Signals:” • SerDes register—BnTTLCRn0[FLT_SEL]: Removed row describing differences in recommended settings. The recommended setting for BnTTLCRn0[FLT_SEL] is the same (01_1011b) for all protocols on both Rev 2 and Rev 3. • SerDes register—BnTTLCRn0[PM_DIS]: Removed row describing differences in recommended settings. The recommended setting for BnTTLCRn0[PM_DIS] is the same (0b) for all protocols on both Rev 2 and Rev 3. • SerDes register—BnTTLCRn0[bit 0]: First, the bit number was incorrect. It should have been bit 31, not bit 0. Second, the row describing differences in recommended settings was removed. The recommended setting for BnTTLCRn0[bit 31] is the same (1b) for all protocols on both Rev 2 and Rev 3.
0	06/2014	Initial public release.

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