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P3041 QorIQ Integrated Processor Design Checklist

About this document

This document provides recommendations for new designs based on the P3041. It may also be useful in debugging newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

Each section has a pin termination checklist or a system-level checklist, or sometimes both.

Before you begin

Ensure you are familiar with the following Freescale documents before proceeding:

- *P3041 QorIQ Integrated Processor Hardware Specifications* (P3041EC)
- *P3041 QorIQ Integrated Processor Reference Manual* (P3041RM)
- *P3041 Chip Errata* (P3041CE)
- *QorIQ Data Path Acceleration Architecture (DPAA) Reference Manual* (DPAARM)

Contents

1 Simplifying the first phase of design

This section outlines recommendations to simplify the first phase of design. Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

This figure shows the major functional units within the chip.

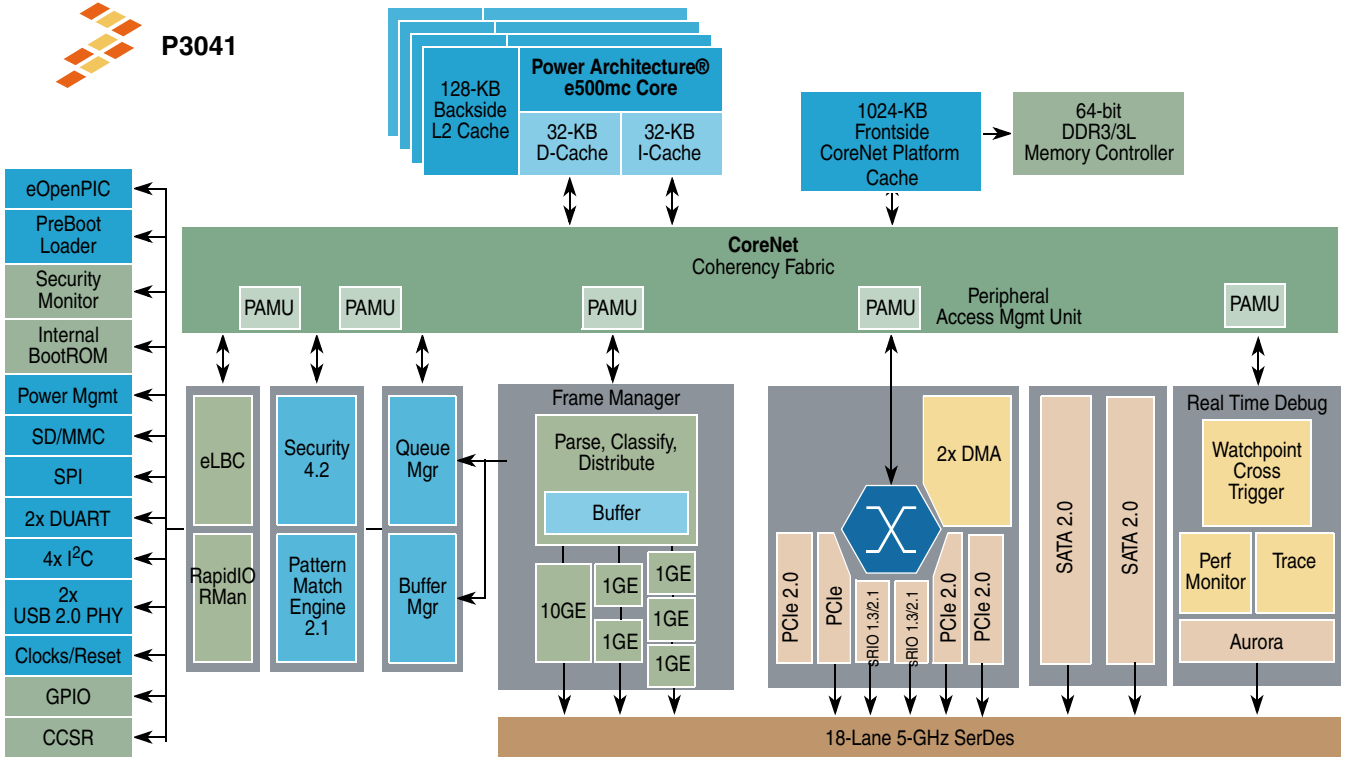


Figure 1. Chip Block Diagram

1.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
Related documentation		
P3041CE	*P3041 Chip Errata* **Note:** This document describes the latest fixes and work-arounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your Freescale representative
P3041EC	*P3041 QorIQ Integrated Processor Hardware Specifications*	Contact your Freescale representative
P3041FS	*P3041 Fact Sheet*	www.freescale.com
P3041RM	*P3041 QorIQ Integrated Processor Reference Manual*	www.freescale.com
P3041RMAD	*Errata to P3041 QorIQ Integrated Processor Reference Manual*	Contact your Freescale representative
DPAARM	*QorIQ Data Path Acceleration Architecture (DPAA) Reference Manual*	Contact your Freescale representative
P3041SECRM	*P3041 Security (SEC 4.2) Reference Manual*	Contact your Freescale representative
E500CORERM	*PowerPC e500 Core Complex Reference Manual*	www.freescale.com
AN4326	*Verification of the IEEE 1588 Interface*	www.freescale.com
AN4311	*SerDes Reference Clock Interfacing and HSSI measurements Recommendations*	www.freescale.com
AN4309	*PowerQUICC DDR3 SDRAM Controller Register Setting Considerations*	www.freescale.com
AN4290	*Configuring the Data Path Acceleration Architecture (DPAA)*	www.freescale.com
AN3939	*DDR Interleaving for PowerQUICC and QorIQ Processors*	www.freescale.com
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.freescale.com
AN3645	*SEC 2/3x Descriptor Programmer's Guide*	www.freescale.com
AN2919	*Determining the I2C Frequency Divider Ratio for SCL*	www.freescale.com

Table 1. Helpful tools and references (continued)

ID	Name	Location
Software tools		
I2CBOOTSEQ	Boot sequencer generator tool allows configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I2C EEPROM. The chip requires a particular data format for register changes as outlined in the P3041RM. The boot sequencer tool (I2CBOOTSEQ) is a C-code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the P3041RM. The file that is generated is an s-record file that can be used to program the EEPROM.	Contact your Freescale representative
LBCUPMIBCG	UPM Programming tool features a GUI for a user-friendly programming interface. It allows programming of all three of the chip's user-programmable machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator will print out the UPM RAM array that can be used in a C-program.	Contact your Freescale representative
NetComm Software	The NetComm device driver software package is available for download. It includes the following: • Device drivers for DPAA and other commonly used modules • Use cases to test the functionality of DPAA and other commonly used modules	www.freescale.com/netcommsw
QorIQ DPAA SDK	Mentor Embedded Linux Essentials for QorIQ Processors with Data Path Acceleration	www.freescale.com
Hardware tools		
P3041DS[1]	Development system, including schematics, bill of materials, board errata list, user's Guide, and configuration guide	Contact your Freescale representative
Models		
IBIS	To ensure first path success, Freescale strongly recommends using the IBIS models for board level simulations, especially for SerDes and DDR characteristics.	www.freescale.com
BSDL	Use the BSDL files in board verification.	www.freescale.com
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	www.freescale.com

Table 1. Helpful tools and references (continued)

ID	Name	Location
Available training		
—	Our third-party partners are part of an extensive alliance network. More information can be found at www.freescale.com/alliances.	www.freescale.com/alliances
—	Training materials from past Smart Network Developer's Forums and Freescale Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	www.freescale.com/alliances

[1] Design requirements in the device hardware specification and design checklist supersede the design/implementation of the DS system.

1.2 Product revisions

This table lists the processor version register (PVR) and system version register (SVR) values for the various chip silicon derivatives.

Table 2. Chip product revisions

Device number	Device revision	Core revision	Processor version register value	System version register value	With...
P3041E	1.0	V2.2	0x8023_0121	0x8219_0310	DPAA SEC 4.2
P3041				0x8211_0310	DPAA only
P3041E	1.1			0x8219_0311	DPAA SEC 4.2
P3041				0x8211_0311	DPAA only

2 Power design recommendations

2.1 Power pin recommendations

Table 3. Power and ground pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
AV_{DD}_CC1	—	Power supply for Core cluster PLL1 (1.0 V through a filter).	Tie to GND		
AV_{DD}_CC2	—	Power supply for Core cluster PLL2 (1.0 V through a filter).	Tie to GND		
AV_{DD}_DDR	—	Power supply for the DDR PLL (1.0 V through a filter).	Tie to GND		
AV_{DD}_PLAT	—	Power supply for the Platform PLL (1.0 V through a filter).	Tie to GND		
AV_{DD}_SRDS1	—	Power supply for the SerDes PLL1 (1.0 V through a filter).	Tie to GND		
AV_{DD}_SRDS2	—	Power supply for the SerDes PLL2 (1.0 V through a filter).	Tie to GND		
AV_{DD}_SRDS3	—	Power supply for the SerDes PLL3 (1.0 V through a filter).	Tie to GND		
SV_{DD}	—	Power supply for the SerDes core logic (1.0 V).	Tie to GND		
BV_{DD}	—	Power supply for the local bus and GPIO (1.8 V/2.5 V/3.3 V).	Tie to GND		
CV_{DD}	—	Power supply for eSPI and& eSDHC.	Tie to GND		
GV_{DD}	—	Power supply for the DDR (1.5 V/1.35V).	Tie to GND		
LV_{DD}	—	Power supply for the TSEC (2.5 V/3.3 V).	Tie to GND		
OV_{DD}	—	Power supply for the general I/O (3.3 V).	Tie to GND		
$V_{DD\_CA\_CB\_PL}$	—	Power supply for core 0-3 and platform (1.0 V).	Tie to GND		
V_{DD_LP}	—	Low power security monitor supply (1.0V)	Tie to GND		
SENSEVDD_CA_PL	—	For Rev 1.1 and Rev 2.0, the better solution is to use the SENSEVDD_CB and SENSEGND_CB pair. The SENSEVDD_CA_PL and SENSEGND_CA_PL pair can be left as unconnected.	Leave unconnected		
SENSEVDD_CB	—				
XV_{DD}	—	Power supply for the SerDes transceiver (1.5 V/1.8 V).	Tie to GND		
POVDD	—	Fuse programming override supply (1.5V).	Tie to GND		

Table 3. Power and ground pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
USB1_VDD_3P3	—	USB1 PHY PLL 3.3V Supply.	Tie to GND or leave unconnected		
USB2_VDD_3P3	—	USB2 PHY Transceiver 3.3V Supply.	Tie to GND or leave unconnected		
USB1_VDD_1P0	—	USB1 PHY PLL 1.0V Supply.	Tie to 1.0V		
USB2_VDD_1P0	—	USB2 PHY PLL 1.0V Supply	Tie to 1.0V		
SGND	—	SerDes core logic GND			
XGND	—	SerDes transceiver GND			
GND	—	Ground			
AGND_SRDS1	—	SerDes PLL 1 GND			
AGND_SRDS2	—	SerDes PLL 2 GND			
AGND_SRDS3	—	SerDes PLL 3 GND			
SENSEGND_CA_PL	—	Core group A and Platform GND sense			
SENSEGND_CB	—	Core group B GND sense			
USB1_AGND	—	USB1 PHY Transceiver GND			
USB2_AGND	—	USB2 PHY Transceiver GND			

2.2 Power system-level recommendations

Table 4. Power design system-level checklist

Item	Remarks (for customer use)	Completed
General		
1. Ensure that all power supplies have a voltage tolerance no greater than 5% from the nominal value.[1]		
2. Ensure the power supply is selected based on MAXIMUM power dissipation.[1]		
3. Ensure the thermal design is based on THERMAL power dissipation.[1]		

Table 4. Power design system-level checklist (continued)

Item	Remarks (for customer use)	Completed
4. Ensure the power-up sequence is within 75 ms.[1]		
5. Use large power planes to the extent possible.		
6. Ensure the PLL filter circuit is applied to $AV_{DD\_CA\_PL}$, AV_{DD_CB}, AV_{DD_DDR}.		
7. If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SRDS. Otherwise, a filter is not required.		
8. Ensure the PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.		
9. Ensure the decoupling capacitors of 0.1 µF are placed at each V_{DD}, AV_{DD}, B/C/G/L/X/S/OV_{DD} pin.		
Power supply decoupling		
10. Provide large power planes, because immediate charge requirements by the device are always serviced from the power planes first.		
11. Place at least one decoupling capacitor at each V_{DD}, AV_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} pins of the device.		
12. Ensure these decoupling capacitors receive their power from separate V_{DD}, AV_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND planes in the PCB, utilizing short traces to minimize inductance.		
13. Capacitors may be placed directly under the device using a standard escape pattern, and others may surround the part.		
14. Ensure these capacitors have a value of 0.01 or 0.1 µF. 15. Only use ceramic surface mount technology (SMT) capacitors to minimize lead inductance, preferably 0402 or 0603.		
16. Distribute several bulk storage capacitors around the PCB, feeding the V_{DD}, AV_{DD}, BV_{DD}, CV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes to enable quick recharging of the smaller chip capacitors.		
17. Ensure the bulk capacitors have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary.		
18. Ensure the bulk capacitors are connected to the power and ground planes through two vias to minimize inductance.		
19. Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply so as to be able to handle the chip dynamic load requirements.[2]		

Table 4. Power design system-level checklist (continued)

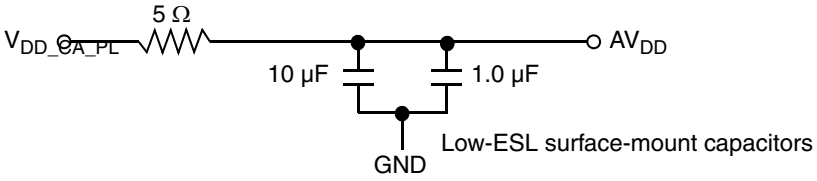
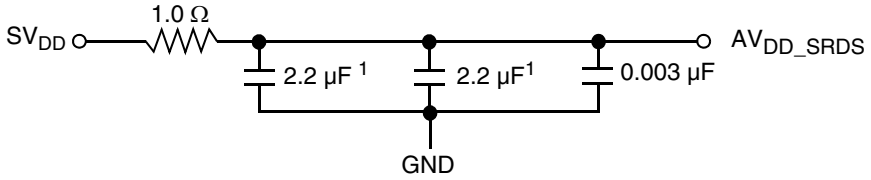
Item	Remarks (for customer use)	Completed
SerDes power supply decoupling		
20. Use only SMT capacitors to minimize inductance.		
21. Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.		
22. Ensure the board has at least one 10×10-nF SMT ceramic chip capacitor as close as possible for each supply ball of the chip. 23. Where the board has blind vias, ensure these capacitors are placed directly below the chip supply and ground connections. 24. Where the board does not have blind vias, ensure these capacitors are placed in a ring around the chip as close to the supply and ground connections as possible.		
25. **For all SerDes supplies:** Ensure there is a 1-µF ceramic chip capacitor on each side of the device.		
26. **For all SerDes supplies:** Ensure there is a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor between the device and any SerDes voltage regulator.		
PLL power supply filtering[3]		
27. Provide independent filter circuits per PLL power supply, as illustrated in this figure[4]. 		
28. Ensure it is built with surface mount capacitors with minimum effective series inductance (ESL). [5]		
29. Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.		
30. Ensure each of the PLLs is provided with power through independent power supply pins ($AV_{DD\_CA\_PLAT}$, AV_{DD_CB}, AV_{DD_DDR}, AV_{DD_SRDS}, respectively).		
31. Ensure the AV_{DD} level is always equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.		

Table 4. Power design system-level checklist (continued)

Item	Remarks (for customer use)	Completed
32. For maximum effectiveness, ensure the filter circuit is placed as close as possible to the AV_{DD_SRDS} ball to ensure it filters out as much noise as possible.		
33. Ensure the ground connection is near the AV_{DD_SRDS} ball. The 0.003-µF capacitor is closest to the ball, followed by the two 2.2-µF capacitors, and finally the 1.0-Ω resistor to the board supply plane.		
34. To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in this figure.  Caution: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk.		
35. Ensure the capacitors are connected from AV_{DD_SRDS} to the ground plane.		
36. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.		
37. Ensure AV_{DD_SRDS} is a filtered version of SVDD.		
38. Ensure that signals on the SerDes interface are fed from the XV_{DD} power plane.		

1 See the P3041EC for more details.
2 Suggested bulk capacitors are 100–330 µF (AVX TPS tantalum or Sanyo OSCON).
3 The PLL power supply filter circuit filters noise in the PLLs' resonant frequency range from 500 kHz–10 MHz.
4 A higher capacitance value for C2 can be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL <= 0.5 nH).
5 Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

3 Power-on reset recommendations

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{PORESET}}$. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted. When $\overline{\text{PORESET}}$ de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 5. Power-on reset system-level checklist

Item	Remarks (for customer use)	Completed
Timing		
1. Ensure $\overline{\text{PORESET}}$ is asserted for a minimum of 1ms. Ensure $\overline{\text{HRESET}}$ is asserted for a minimum of 32 SYSCLK cycles.		
2. Use a 4.7 kΩ pull-down resistor to pull the configuration pin to a valid logic-low level.		
3. **Optional:** An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when $\overline{\text{PORESET}}$ is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of $\overline{\text{PORESET}}$, hold their values for at least 2 SYSCLK cycles after the de-assertion of $\overline{\text{PORESET}}$, and then release the pins to high impedance afterward for normal device operation. **Note:** See the P3041EC for details about reset initialization timing specifications.		
I/O supply voltage encodings		
4. Ensure IO_VSEL[0:4] encodings are selected properly for each I/O supply. The external pull-up resistor on IO_VSEL[0:4] must be less than 1K. Warning: Incorrect voltage-select settings can lead to irreversible device damage. **Note:** See the P3041EC for details about I/O voltage selection.		

This table lists all the reset configuration pins. See the chip reference manual, section 4.6.3 for more information.

Table 6. Reset configuration pins

Reset configuration name	Function signal name	Configuration	Default value	Remarks (for customer use)	Completed
cfg_gpinput[0:15]	LAD[0:15]	This is for an application-specific purpose.	1111 1111 1111 1111		
cfg_xvdd_sel	LAD[26]	0: XVDD 1.8V 1: XVDD 1.5V	1		
cfg_elbc_ecc	LAD[23]	0: NAND flash ECM disable 1: NAND flash ECC enable	1		
cfg_dram_type	LAD[24]	0: DDR3 technology(1.5V) 1: DDR3L technology(1.35V)	1		
cfg_rcw_src[0]	LGPL0/LFCLE	Source of the reset configuration word	1		
cfg_rcw_src[1]	LGPL1/LFALE		1		
cfg_rcw_src[2]	LGPL2/LOE/LFRE		1		
cfg_rcw_src[3]	LGPL3/LFWP		1		
cfg_rcw_src[4]	LGPL5		1		
cfg_svr[0:1]	LAD[16:17]	LAD[16:17] = 2'b11;	11		

4 DDR recommendations

Table 7. DDR pin termination checklist

Signal name	I/O Type	Used	Not used	Remarks (for customer use)	Completed
MA[0:15]	O	Must be properly terminated to VTT.	May be left unconnected.		
MBA[0:2]	O	Must be properly terminated to VTT.	May be left unconnected.		
MCK[0:3] / $\overline{\text{MCK[0:3]}}$	O	Must be properly terminated.	May be left unconnected. However, the MCK pin should be disabled via DDRCLKDR register.		
MCKE[0:3]	O	Must be properly terminated to VTT.	May be left unconnected.		

Table 7. DDR pin termination checklist (continued)

Signal name	I/O Type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{MCS}}$[0:3]	O	Must be properly terminated to VTT.	May be left unconnected.		
MDIC[0:1]	I/O	These pins are used for automatic calibration of the DDR IOs. The calibration resistor value for DDR3 should be 20-Ω (full-strength mode) or 40.2-Ω (half-strength mode).	May be left unconnected.		
MDM[0:8]	O	—	May be left unconnected.		
MDQ[0:63]	I/O	—	May be left unconnected.		
MDQS[0:8] / $\overline{\text{MDQS}}$[0:8]	I/O	—	May be left unconnected.		
MECC[0:7]	I/O	—	May be left unconnected.		
$\overline{\text{MAPAR\_ERR}}$	I	This pin is an open drain output from registered DIMMs. Ensure that a 4.7K pull-up to GVDD is present on this pin.	This pin is should be pulled up whether used or not.		
MAPAR_OUT	O	If the controller supports the optional MAPAR_OUT and MAPAR_ERR signals, ensure that they are hooked up as follows: • MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM) • ERR_OUT (from the RDIMM) => MAPAR_ERR (at the controller)	May be left unconnected.		

Table 7. DDR pin termination checklist (continued)

Signal name	I/O Type	Used	Not used	Remarks (for customer use)	Completed
MODT[0:3]	O	Are the MODT signals connected correctly? In general, for Dual Ranked DIMMS, the following should all go to the same physical memory bank: • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) • MODT(2), MCS(2), MCKE(2) • MODT(3), MCS(3), MCKE(3) For Quad Ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But, in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one Quad Ranked DIMM. If DIMM (modules) is used then the termination is on the DIMM. If discrete design is used, MODT[0:3] must be terminated to VTT when used.	May be left unconnected.		
$\overline{\text{MRAS}}$	O	Must be properly terminated to VTT.	May be left unconnected.		
$\overline{\text{MCAS}}$	O	Must be properly terminated to VTT.	May be left unconnected.		
$\overline{\text{MWE}}$	O	Must be properly terminated to VTT.	May be left unconnected.		
MVREF	I	DDR Reference Voltage: 0.49 × GVDD to 0.51 × GVDD. MVREF can be generated using a divider from GVDD as MVREF. Another option is to use supplies that generate GVDD, VTT, and MVREF voltage. These methods help reduce differences between GVDD and MVREF. Generating MVREF from a separate regulator is not recommended as MVREF will not track GVDD as closely.	Must be connected to GND.		

5 SerDes recommendations

Table 8. SerDes pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
SD_TX[0:17]	O	—	Must be left unconnected.		
$\overline{\text{SD\_TX}}$[0:17]	O	—	Must be left unconnected.		
SD_RX[0:17]	I	—	Must be connected to GND.		
$\overline{\text{SD\_RX}}$[0:17]	I	—	Must be connected to GND.		
SD_REF_CLK1	I	—	Must be connected to GND.		
SD_REF_CLK2	I	—	Must be connected to GND.		
SD_REF_CLK3	I	—	Must be connected to GND.		
$\overline{\text{SD\_REF\_CLK1}}$	I	—	Must be connected to GND.		
$\overline{\text{SD\_REF\_CLK2}}$	I	—	Must be connected to GND.		
$\overline{\text{SD\_REF\_CLK3}}$	I	—	Must be connected to GND.		

6 eLBC recommendations

Table 9. eLBC pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
LAD[0:31]	I/O	These pins are reset configuration pin. They have a weak internal pull-up P-FET that is enabled only when the processor is in the reset state. LAD[16:17] cfg_svr[0:1]. LAD[23] cfg_elbc_ecc. LAD[24] cfg_dram_type. LAD[26] cfg_xvdd. **Note:** The following pins must NOT be pulled down during power-on reset: LAD[16:22], LAD[25]	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND. If the POR default is not used, still need to pull up if the POR default is acceptable.		
LA[27:31]	O	Pin LA[28:31] must NOT be pulled down during power-on reset.			
LDP[0:3]	I/O	—	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND.		
$\overline{\text{LCS}}$[0:7]	O	Recommend a weak pull-up resistor (2–10KΩ) be placed on this pin to BV_{DD} to ensure no random chip select assertion due to possible noise and etc.	May be left unconnected.		
$\overline{\text{LWE}}$[0:3]	O	—	May be left unconnected.		
LBCTL	O				
LALE	O				
LGPL0/LFCLE	O	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled	If the POR default is acceptable, May be left unconnected.		
LGPL1/LFALE	O				
LGPL2/LOE/LFRE	O				
LGPL3/LFWP	O				
LGPL4/LGTA/ LUPWAIT/LPBSE	I/O	For systems which boot from Local Bus (GPCM)-controlled NOR flash or (FCM)-controlled NAND flash, a pull up on LGPL4 is required.			

Table 9. eLBC pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
LGPL[5]	O	This pin is a reset configuration pin. It has a weak internal pull-up P-FET that is enabled only when the processor is in the reset state.	If the POR default is acceptable, May be left unconnected.		
LCLK[0:1]	O	—	May be left unconnected.		

7 DMA recommendations

Table 10. DMA pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{DMA1\_DREQ0}}$ / $\overline{\text{GPIO[18]}}$	I	RCW[DMA1] bit to select between DMA1 or GPIO function.	Tie high through a 2–10 kΩ to OVDD.		
$\overline{\text{DMA1\_DACK0}}$ / GPIO[19]	O	RCW[DMA1] bit to select between DMA1 or GPIO function.	Tie high through a 2–10 kΩ to OVDD.		
$\overline{\text{DMA1\_DDONE0}}$	O	—	If RCW field DMA1 = 0b1 (RCW bit 384), the DMA1 external interface is not enabled and the DMA1_DDONE0 pin should be left as a no connect.		
$\overline{\text{DMA2\_DREQ0}}$ / GPIO[20]/LB_MDVAL	I	RCW[DMA2] bit to select between DMA2 or debug or GPIO function.	Tie high through a 2–10 kΩ to OVDD.		
$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT[7]}}$/ LB_MSRCID[0]	O	RCW[DMA2] bit to select between DMA2 or debug or GPIO function.	Tie high through a 2–10 kΩ to OVDD.		
$\overline{\text{DMA2\_DDONE0}}$	O	RCW[DMA2] bit to select between DMA2 or debug or GPIO function.	If RCW field DMA2 = 0b1 (RCW bit 386, 387), the DMA2 external interface is not enabled and the DMA2_DDONE0 pin should be left as a no connect.		

8 PIC recommendations

Table 11. PIC pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
IRQ[0:2}	I	Ensure pin is driven in the non asserted state, or use pull up.	Tie low through a 2–10 kΩ to GND.		
IRQ0[3:11]/GPIO[21:29]	I	Ensure pin is driven in the non asserted state, or use pull up. Configure RCW to select IRQ function.	Tie low through a 2–10 kΩ to GND.		
$\overline{\text{IRQ\_OUT}}$/EVT9	O	Pull up through a 2–10 kΩ resistor to OV_{DD}.	May be left unconnected.		

9 IEEE 1588 recommendations

Table 12. IEEE 1588 pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
TSEC_1588_CLK_IN	I	External high precision timer reference clock input.	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
TSEC_1588_TRIG_IN[1:2]	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
TSEC_1588_ALARM_OUT1	O	—	May be left unconnected.		
TSEC_1588_ALARM_OUT2	O	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.	May be left unconnected.		
TSEC_1588_CLK_OUT	O	—	May be left unconnected.		

Table 12. IEEE 1588 pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
TSEC_1588_PULSE_OUT[1:2]	O	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.	May be left unconnected.		
EC_XTRNL_RX_STMP1	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
EC_XTRNL_TX_STMP1	I				
EC_XTRNL_RX_STMP2	I				
EC_XTRNL_TX_STMP2	I				

10 Ethernet management recommendations

Table 13. Ethernet management pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
EMI1_MDC	O	—	May be left unconnected.		
EMI1_MDIO	I/O	Pull up through a 2–10 kΩ resistor to LV_{DD}.	Tie low through a 2–10 kΩ resistor to GND.		
EMI2_MDC	I/O	Should be pulled up to 1.2 V through a 180 Ω ± 1% resistor for EMI2_MDC.	May be left unconnected.		
EMI2_MDIO	I/O	Should be pulled up to 1.2 V through a 330 Ω ± 1% resistor for EMI2_MDIO.	Tie low through a 2–10 kΩ resistor to GND.		

11 TSEC recommendations

Table 14. TSEC pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
EC1_GTX_CLK125	O	This pin functions as EC1_GTX_CLK125 for RGMII mode.	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
TSEC1_TXD[0:3]	O	—	May be left unconnected.		
TSEC1_TX_EN	O	This pin requires an external 1 kΩ pull-down resistor to prevent the PHY from seeing a valid Transmit Enable before it is actively driven (during reset).	May be left unconnected.		
TSEC1_GTX_CLK	O	—	May be left unconnected.		
TSEC1_RXD[0:3]	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
TSEC1_RX_DV	I	—	Tie low through a 2–10 kΩ resistor to GND.		
TSEC1_RX_CLK	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
EC2_GTX_CLK125	O	This pin functions as EC2_GTX_CLK125 for RGMII mode.	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		
TSEC2_TXD[0:3]	O	—	May be left unconnected.		
TSEC2_TX_EN	O	This pin requires an external 1 kΩ pull-down resistor to prevent the PHY from seeing a valid Transmit Enable before it is actively driven (during reset).	May be left unconnected.		
TSEC2_GTX_CLK	O	—	May be left unconnected.		
TSEC2_RXD[0:3]	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		

Table 14. TSEC pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
TSEC2_RX_DV	I	—	Tie low through a 2–10 kΩ resistor to GND.		
TSEC2_RX_CLK	I	—	Tie low to the inactive state through a 2–10 kΩ resistor to GND.		

12 UART recommendations

Table 15. UART pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
UART1_SOUT/GPIO8	O	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW (Reset Configuration Word).	May be left unconnected.		
UART2_SOUT/GPIO9	O				
UART1_SIN/GPIO10	I	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW (Reset Configuration Word).	Tie low through a 2–10 kΩ resistor to GND.		
UART2_SIN/GPIO11	I				
$\overline{\text{UART1\_RTS}}$/ UART3_SOUT/GPIO12	O	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW (Reset Configuration Word).	May be left unconnected.		
$\overline{\text{UART2\_RTS}}$/ UART4_SOUT/GPIO13	O				
$\overline{\text{UART1\_CTS}}$/ UART3_SIN/GPIO14	I	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW (Reset Configuration Word).	Tie high through a 2–10 kΩ resistor to OVDD.		
$\overline{\text{UART2\_CTS}}$/ UART4_SIN/GPIO15	I				

13 I²C recommendations

Table 16. I²C pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
IIC1_SDA	I/O	Tie these open-drain signals high through a nominal 1 kΩ resistor to OV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	Tie high through a 2–10 kΩ resistor to OV_{DD}.		
IIC1_SCL	I/O				
IIC2_SDA	I/O				
IIC2_SCL	I/O				
IIC3_SCL/ $\overline{\text{SDHC\_CD}}$/GPIO16	I/O	These signals are multiplexed with other functionalities.If configured for I2C function, tie these open-drain signals high through a nominal 1 kΩ resistor to OV_{DD}. Optimum pull-up value depends on the capacitive loading of external devices and required operating speed.	Tie high through a 2–10 kΩ resistor to OV_{DD}.		
IIC3_SDA/ SDHC_WP/GPIO17	I/O				
IIC4_SCL/$\overline{\text{EVT5}}$	I/O				
IIC4_SDA/$\overline{\text{EVT6}}$	I/O				

14 eSDHC recommendations

Table 17. eSDHC pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
SDHC_CMD	I/O	Pull up high through a 2–10 kΩ resistor to CV_{DD}.	Pull up high through a 2–10 kΩ resistor to CV_{DD}.		
SDHC_DAT[0:3]	I/O	Pull up high through a 2–10 kΩ resistor to CV_{DD}.	Tie high through a 2–10 kΩ resistor to CV_{DD}.		
SDHC_DAT[4:7]/ SPI_CS[0:3]	O	Pull up high through a 2–10 kΩ resistor to CV_{DD}. SDHC_DAT[4:7] require CVDD = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.	Tie high through a 2–10 kΩ resistor to CV_{DD}.		

Table 17. eSDHC pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
SDHC_WP/ IIC3_SCL/GPIO16	I	If RCW field I2C = 0b100 or 0b101 (RCW bits 355–357), the SDHC_WP and $\overline{\text{SDHC\_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC\_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC\_CD}}$ = 0 (card detected). If RCW field I2C != 0b100 or 0b101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and $\overline{\text{SDHC\_CD}}$ are internally driven such that SDHC_WP = write enabled and $\overline{\text{SDHC\_CD}}$ = card detected and the selected I2C3 or GPIO external pin functionality may be used.	It can be configured as a GPIO output pin and leave unconnected.		
SDHC_CD/ IIC3_SDA/GPIO17	I	If RCW field I2C = 0b100 or 0b101 (RCW bits 355–357), the SDHC_WP and $\overline{\text{SDHC\_CD}}$ input signals are enabled for external use. If SDHC_WP and $\overline{\text{SDHC\_CD}}$ are selected and not used, they must be externally pulled low such that SDHC_WP = 0 (write enabled) and $\overline{\text{SDHC\_CD}}$ = 0 (card detected). If RCW field I2C != 0b100 or 0b101, thereby selecting either I2C3 or GPIO functionality, SDHC_WP and $\overline{\text{SDHC\_CD}}$ are internally driven such that SDHC_WP = write enabled and $\overline{\text{SDHC\_CD}}$ = card detected and the selected I2C3 or GPIO external pin functionality may be used.	It can be configured as a GPIO output pin and leave unconnected.		
SDHC_CLK	O	33 Ω serial resistor must be provided for SDHC_CLK and placed close to P3041 device.	May be left unconnected.		

15 eSPI recommendations

Table 18. eSPI pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
SPI_MISO	I/O	—	Tie high through a 2–10 kΩ resistor to CV_{DD}.		
SPI_MOSI	O	—	Tie high through a 2–10 kΩ resistor to CV_{DD}.		
$\overline{\text{SPI\_CS}}$[0:3]/ SDHC_DAT[4:7]	O	Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.	May be left unconnected.		
SPI_CLK	O	—	May be left unconnected.		

16 USB recommendations

Table 19. USB pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
USB1_UDP	I/O	—	May be left unconnected.		
USB1_UDM	I/O	—	May be left unconnected.		
USB1_VBUS_CLMP	I	A divider network is required on this signal. See HW spec. Section 3.9, “USB Divider Network.”	Tie low through a 1 kΩ resistor to GND.		
USB1_UID	I	—	Tie low through a 1 kΩ resistor to GND.		
USB1_DRVVBUS/ GPIO04	O	—	Tie low through a 1 kΩ resistor to GND.		
USB1_PWRFAULT/ GPIO05	I/O	—	Tie low through a 1 kΩ resistor to GND.		

Table 19. USB pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
USB1_IBIAS_REXT	—	This pin should be pulled low through a 10 kΩ+/- 1% precision resistor to GND.	May be left unconnected.		
USB1_VDD_1P8_DECAP	—	A 1uF to 1.5 uF capacitor connected to GND is required on this signal. A list of recommended capacitors are shown in HW spec Section 3.6.4.2, “USBn_VDD_1P8_DECAP Capacitor Options."	May be left unconnected.		
USB2_UDP	I/O	—	May be left unconnected.		
USB2_UDM	I/O	—	May be left unconnected.		
USB2_VBUS_CLMP	I	A divider network is required on this signal. See HW spec. Section 3.9, “USB Divider Network.”	Tie low through a 1 kΩ resistor to GND.		
USB2_UID	I	—	Tie low through a 1 kΩ resistor to GND.		
USB2_DRVVBUS/ GPIO06	O	—	Tie low through a 1 kΩ resistor to GND.		
USB2_PWRFAULT/ GPIO07	I/O	—	Tie low through a 1 kΩ resistor to GND.		
USB2_IBIAS_REXT	—	This pin should be pulled low through a 10 kΩ+/- 1% precision resistor to GND.	May be left unconnected.		
USB2_VDD_1P8_DECAP	—	A 1uF to 1.5 uF capacitor connected to GND is required on this signal. A list of recommended capacitors are shown in HW spec Section 3.6.4.2, “USBn_VDD_1P8_DECAP Capacitor Options."	May be left unconnected.		

17 GPIO recommendations

Table 20. GPIO pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
GPIO[0:3]	I/O	All signals are configured as inputs when the device comes out of reset and also when HRESET is asserted. Open-drain capability on all ports.	Pull high through a 2–10kΩ to OV_{DD} or leave floating and configured as outputs via the GPIO direction register (GPDIR).		

Table 20. GPIO pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
GPIO4/USB1_DRVVBUS	I/O	General purpose I/O. Each signal can be set individually to act as input or output, according to application. Configure RCW to select GPIO function.	Pull high through a 2–10kΩ to OV_{DD} or leave floating and configured as outputs via the GPIO direction register (GPDIR).		
GPIO5/USB1_PWRFAULT	I/O				
GPIO6/USB2_DRVVBUS	I/O				
GPIO7/ USB2_PWRFAULT	I/O				
GPIO8/ UART1_SOUT	I/O				
GPIO9/ UART2_SOUT	I/O				
GPIO10/ UART1_SIN	I/O				
GPIO11/ UART2_SIN	I/O				
GPIO12/$\overline{\text{UART1\_RTS}}$/ UART3_SOUT	I/O				
GPIO13/$\overline{\text{UART2\_RTS}}$/ UART4_SOUT	I/O				
GPIO14/$\overline{\text{UART1\_CTS}}$/ UART3_SIN	I/O				
GPIO15/$\overline{\text{UART2\_CTS}}$/ UART4_SIN	I/O				
GPIO16/IIC3_SCL/ $\overline{\text{SDHC\_CD}}$	I/O				
GPIO17/IIC3_SDA/ SDHC_WP	I/O				
GPIO18/ $\overline{\text{DMA1\_DREQ0}}$	I/O				

Table 20. GPIO pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
GPIO19/$\overline{\text{DMA1\_DACK0}}$	I/O	General purpose I/O. Each signal can be set individually to act as input or output, according to application. Configure RCW to select GPIO function.	Pull high through a 2–10kΩ to OV_{DD} or leave floating and configured as outputs via the GPIO direction register (GPDIR).		
GPIO20/$\overline{\text{DMA2\_DREQ0}}$/ ALT_MDVAL	I/O				
GPIO[21:29]/IRQ0[3:11]	I/O				
GPIO30/ TSEC_1588_ALARM_OUT2	I/O		Pull high through a 2–10kΩ to LVDD or leave floating and configured as outputs via theh GPIO direction register (GPDIR)		
GPIO31/ TSEC_1588_PULSE_OUT2	I/O				

18 DFT recommendations

Table 21. DFT pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{SCAN\_MODE}}$	I	See HW specification, this is a test pin for factory use only and must be pulled up (100 Ω –1 kΩ) to OVDD for normal machine operation.			
TEST_SEL	I	See HW specification, This is a test pin for factory use only and must be pulled down (1 kΩ – 2 kΩ) to GND for normal machine operation.			

19 Power management recommendations

Table 22. Power management termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
ASLEEP	O	System Ready. Must NOT be pulled down during power-on reset.			

20 Trust recommendations

Table 23. Trust termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{TMP\_DETECT}}$	I	If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. 1 kΩ pull-down resistor strongly recommended.	Tie high to OVDD (High power trust is not used). If no aspect of Trust Arch is to be used, the following Trust Arch pins must be tied to GND. – PO_VDD – TMP_DETECT – LP_TMP_DETECT		
$\overline{\text{LP\_TMP\_DETECT}}$	I	If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. 1 kΩ pull-down resistor strongly recommended.	Tie high to VDD_LP (Low power trust is not used). If no aspect of Trust Arch is to be used, the following Trust Arch pins must be tied to GND. – PO_VDD – TMP_DETECT – LP_TMP_DETECT		

21 Clock recommendations

Table 24. Clock pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
EC1_GTX_CLK125	I	If any of the eTSECs are used in gigabit mode, connect it to a 125 MHz clock.	Pull low through a 2–10 kΩ resistor to GND.		
EC2_GTX_CLK125	I	If any of the eTSECs are used in gigabit mode, connect it to a 125 MHz clock.	Pull low through a 2–10 kΩ resistor to GND.		
CLK_OUT	O	CLK_OUT is for monitoring purposes only, not for clocking other devices.	May be left unconnected. This output is actively driven during reset rather than being three-stated during reset.		

Table 24. Clock pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
RTC	I	The default source of the time base is the CCB clock divided by eight. For more details, see the E500CORERM.	Pull low through a 2–10 kΩ resistor to GND.		
SYSCLK	I	Must always be connected to an input clock of 67–133 MHz.	Must always be connected to an input clock of 67–133 MHz.		

22 System control recommendations

Table 25. System control pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{PORESET}}$	I	It is required to be asserted per specification in relation to minimum assertion time and during power-up/power-down. It is an input only pin and must be asserted to sample power on configuration pins.			
$\overline{\text{HRESET}}$	I/O	Pull up high through a 2–10 kΩ resistor to OVDD. This pin is an open drain signal.			
$\overline{\text{RESET\_REQ}}$	O	Must NOT be pulled down during power-on reset.			
CKSTP_OUT	O	Pull up high through a 2–10 kΩ resistor to OVDD. This pin is an open drain signal.			

23 Debug recommendations

Table 26. Debug pin termination checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
$\overline{\text{EVT0}}$	I/O	Debug Event. EVT[0:1] and EVT[4] are used as part of the Aurora Debug Interface. EVT1 I/O Recommend a pull-up to OVDD be used.	Pull high through a 2–10kΩ to OV_{DD}		
$\overline{\text{EVT1}}$	I/O				
$\overline{\text{EVT2}}$	I/O				
$\overline{\text{ETT3}}$	I/O				
$\overline{\text{EVT4}}$	I/O				
$\overline{\text{EVT5}}$/IIC4_SCL	I/O	Debug Event. Configure RCW to select debug function.	Tie high through a 2–10 kΩ resistor to OV_{DD}.		
$\overline{\text{EVT6}}$/IIC4_SDA	I/O				
$\overline{\text{EVT7}}$/$\overline{\text{DMA2\_DACK0}}$/ ALT_MSRCID0	I/O				
$\overline{\text{EVT8}}$/$\overline{\text{DMA2\_DDONE0}}$/ ALT_MSRCID1	I/O				
$\overline{\text{EVT9}}$/IRQ_OUT	I/O				
MDVAL	O	—	May be left unconnected.		
MSRCID0	O	Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.	May be left unconnected.		
MSRCID1	O	—	May be left unconnected.		
MSRCID2	O	—	May be left unconnected.		
ALT_MDVAL/ $\overline{\text{DMA2\_DREQ0}}$/GPIO20	O	Configure RCW to select alternate debug function.	May be left unconnected.		

Table 26. Debug pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
ALT_MSRCID0/ DMA2_DACK0/EVT7	O	Configure RCW to select alternate debug function.	May be left unconnected.		
ALT_MSRCID1/ DMA2_DDONE0/EVT8	O	Configure RCW to select alternate debug function.	May be left unconnected.		

24 JTAG recommendations

24.1 JTAG pin termination recommendations

Table 27. JTAG Pin Termination Checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
TCK	I	If COP is used, connect as needed and strap to OVDD via a 10 kΩ pull up.	If COP is unused, tie TCK to OVDD through a 10 kΩ resistor. This prevents TCK from changing state and reading incorrect data into the device.		
TDI	I	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin3 of the COP connector.	May be left unconnected.		
TDO	O	Connect to Pin1 of the COP connector.	May be left unconnected.		
TMS	I	This pin has a weak internal pull-up P-FET that is always enabled. Connect to Pin9 of the COP connector.	May be left unconnected.		
$\overline{\text{TRST}}$	I	Connect as shown in Figure 2.	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω resistor.		

24.2 JTAG system-level recommendations

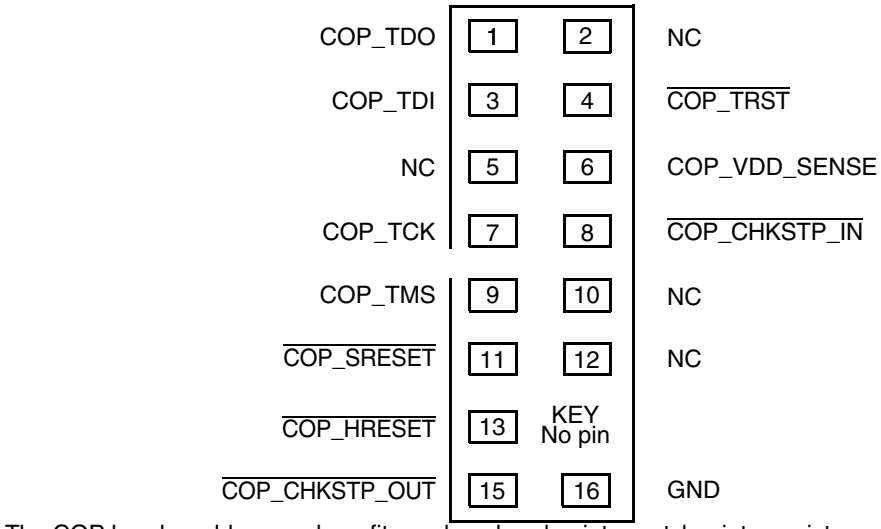
Table 28. JTAG system-level checklist

Item	Remarks (for customer use)	Completed
General		
1. Configure the group of system control pins as shown in Figure 2. **Note:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.		

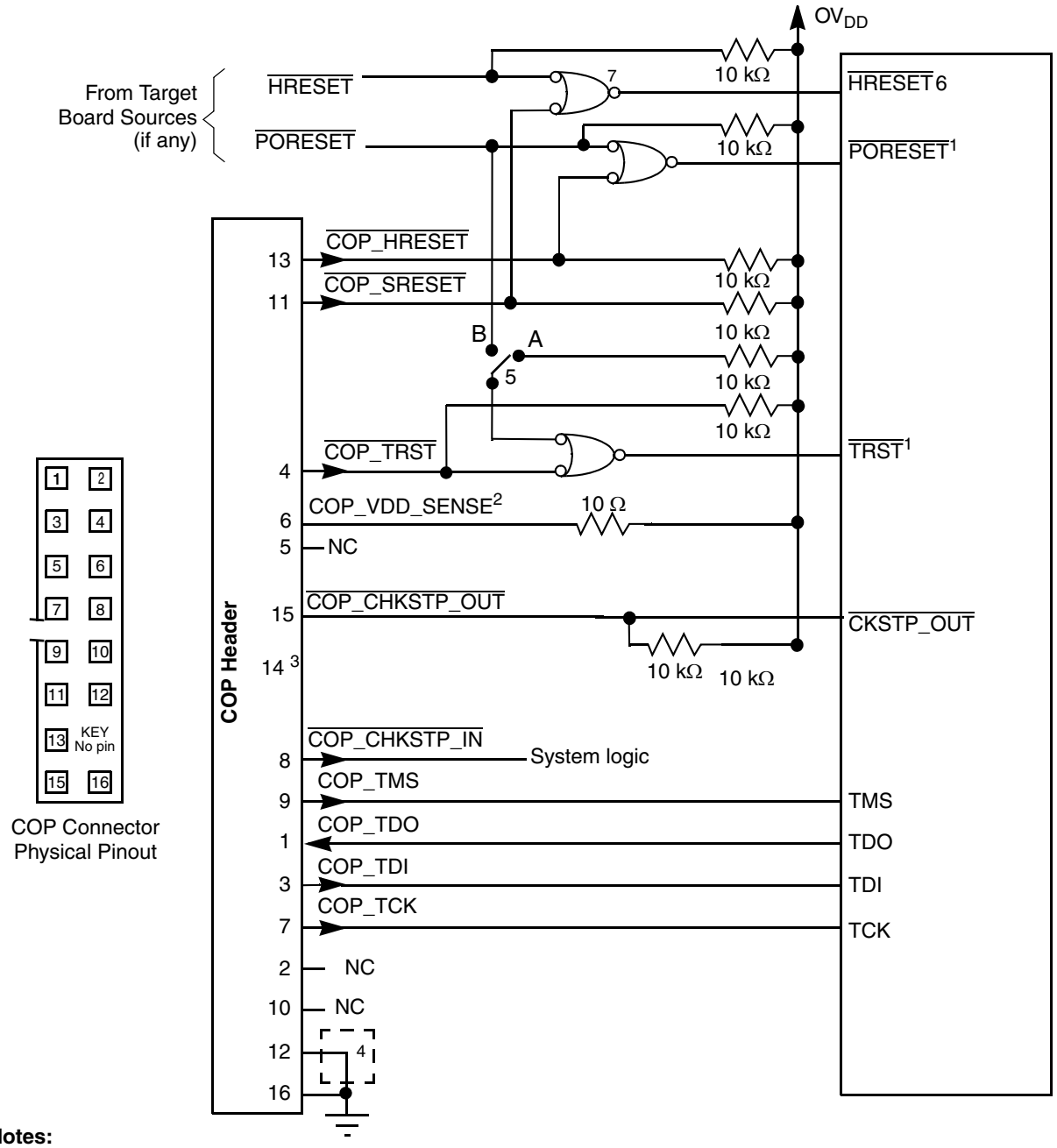
Table 28. JTAG system-level checklist (continued)

Item	Remarks (for customer use)	Completed
2. The common on-chip processor (COP) function of these processors allows a remote computer system, typically a PC with dedicated hardware and debugging software, to access and control the internal operations of the processor. The COP interfaces primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.		
Boundary-scan testing		
3. Ensure that $\overline{\text{TRST}}$ is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. **Note:** While the JTAG state machine can be forced into the Test Logic Reset state using only the TCK and TMS signals, systems generally assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.		

Table 28. JTAG system-level checklist (continued)

Item	Remarks (for customer use)	Completed
4. Follow the arrangement shown in Figure 2 to allow the COP port to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.		
5. The COP interface has a standard header, shown in the following figure, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key. There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in this figure is common to all known emulators.  **Note:** The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.		

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 2. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion will give unpredictable results.



Notes:

1. The COP port and target board must be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch must be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch must be closed to position B.
6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.
7. This is an open-drain gate.

Figure 2. JTAG Interface Connection

25 No connect recommendations

Table 29. No Connect Pin Termination Checklist

Signal name	Signal type	Used	Not used	Remarks (for customer use)	Completed
RSVD	—	All RSVD pins must left unconnected (floating).			

26 Thermal recommendations

26.1 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

26.2 Thermal system-level recommendations

Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

Table 30. Thermal system-level checklist

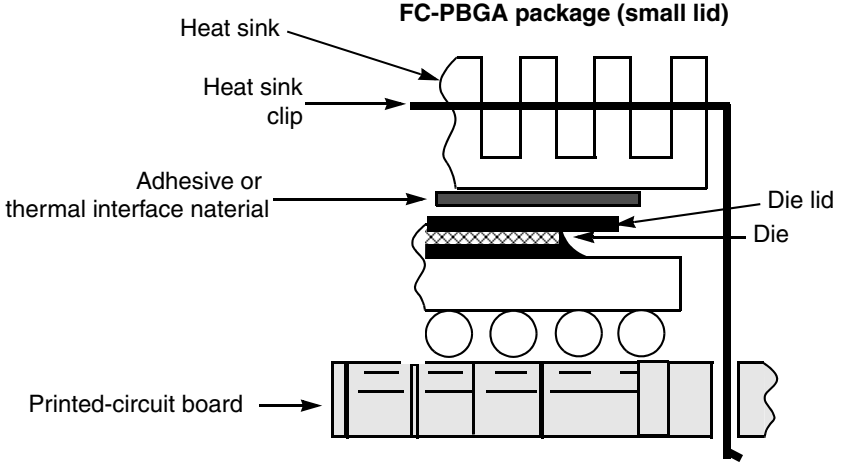
Item	Remarks (for customer use)	Completed
1. Use the recommended thermal model. Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.		
2. Use this recommended board attachment method to the heat sink: **FC-PBGA package (small lid)**  		
3. Ensure the heat sink is attached to the printed-circuit board with the spring force centered over the package.		
4. Ensure the spring force does not exceed 10 pounds force (45 Newtons).		
5. A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance.		
6. Ensure the method of mounting heat sinks on the package is by means of a spring clip attachment to the printed-circuit board.		

Table 30. Thermal system-level checklist (continued)

Item	Remarks (for customer use)	Completed
7. A thermal simulation is required to determine the performance in the application.[4]		

Note:

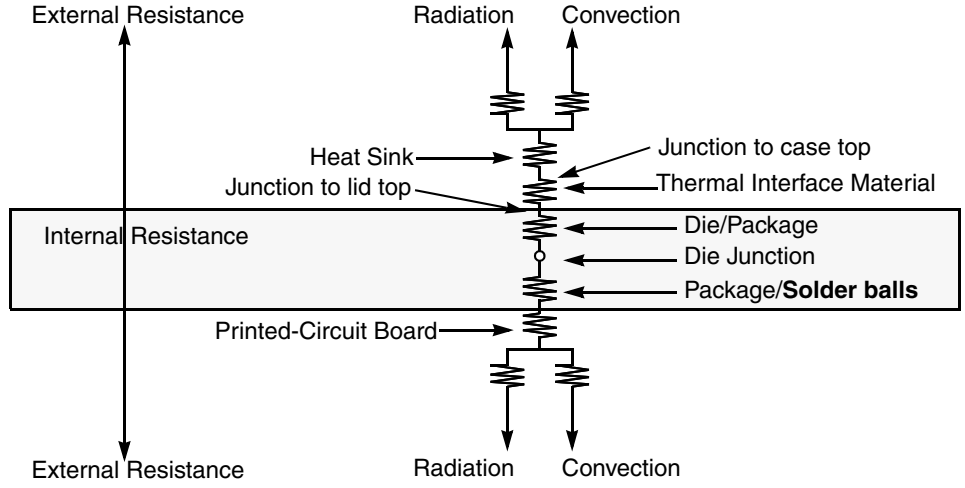
1. The performance of thermal interface materials improves with increased contact pressure; the thermal interface vendor generally provides a performance characteristic char tto guide improved performance.
2. The system board designer can choose among several types of commercially-available heat sinks to determine the appropriate one to place on the device. Ultimately, the final selection of an appropriate heat sink depends on factors such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.
3. The system board designer can choose among several types of commercially-available thermal interface materials.
4. A Flotherm thermal model of the part is available.

26.3 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

This figure depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.



(Note the internal versus external package resistance)

Figure 3. Package with heat sink mounted to a printed-circuit board

With this package, heat flow is both to the board and to the heat sink. A thermal simulation is required to determine the performance in the application. A Flotherm thermal model of the part is available.

27 Revision history

This table summarizes changes to this document.

Table 31. Document revision history

Rev. Number	Date	Change
0	04/2014	• Initial public release.

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