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Application Note

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Migrating Software Applications from the S12 (XE/XS/P) and S08 to S12G Microcontrollers

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1 Introduction

This application note is intended to help you migrate applications from the S12XE, S12XS, S12P and S08 families to the S12G family of microcontrollers. This document compares the S12G family and the other devices, pointing out differences you may want to consider when choosing a replacement MCU and migrating applicable software.

The S12G family is intended for automotive applications and maintains functional compatibility with the S12XS and S12P families, incorporating many of the features present on those devices. CAN and LIN/J2620 communication modules are implemented to target virtually any automotive application. The major advantage of the S12G family lies in its ability to maintain the performance of larger families, such as the S12XE, but with a lower pin count. The power consumption is also improved on the S12G family because it was manufactured with 180 nm technology (unlike other MCUs, such as the S08, made with 250 nm

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technology). The 180 nm process helps decrease current consumption and reduces the size of the MCU (compared to the 250 nm process). For specific information on the S12G family, refer to the reference manual as well as any errata, both of which are documented at www.freescale.com.

Table 1 highlights the modules and peripherals for each member of the S12G microcontroller family. As mentioned previously, this family focuses on small pin counts ranging from TSSOP 20 to LQFP 100 pins. As a result, applications requiring multiple input/output pins or increased special modules, such as a larger number of ADC channels, are not suited for porting to an S12G microcontroller. Also, notice that the maximum frequency is 25 MHz, so applications running at higher frequencies will need to be recalibrated.

Table 1. Comparison between S12G family members

Feature	S12GN16	S12GN32	S12GN48	S12G48	S12G64	S12G96	S12G128	S12G192	S12GA192	S12G240	S12GA240
CPU	CPU12V1										
Flash memory [Kbytes]	16	32	48	48	64	96	128	192	192	240	240
EEPROM [Bytes]	512	1024	1536	1536	2048	3072	4096	4096	4096	4096	4096
RAM [Bytes]	1024	2048	4096	4096	4096	8192	8192	11264	11264	11264	11264
MSCAN	—	—	—	1	1	1	1	1	1	1	1
SCI	1	1	2	2	2	3	3	3	3	3	3
SPI	1	1	2	2	2	3	3	3	3	3	3
16-Bit Timer channels	6	6	6	6	6	8	8	8	8	8	8
8-Bit PWM channels	6	6	6	6	6	8	8	8	8	8	8
10-Bit ADC channels	8	8	12	12	12	12	12	16	—	16	—
12-Bit ADC channels	—	—	—	—	—	—	—	—	16	—	16
RVA (Ref. Voltage Attenuator)	—	—	—	—	—	—	—	—	Yes	—	Yes
8-Bit DAC	—	—	—	—	—	—	—	—	2	—	2
ACMP (analog comparator)	1	1	1	1	1	—	—	—	—	—	—
PLL	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Osc.	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Internal 1 MHz RC oscillator	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
20-pin TSSOP	Yes	Yes	—	—	—	—	—	—	—	—	—
32-pin LQFP	Yes	Yes	Yes	Yes	Yes	—	—	—	—	—	—
48-pin LQFP	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
48-pin QFN	Yes	Yes	—	—	—	—	—	—	—	—	—

Table 1. Comparison between S12G family members (continued)

Feature	S12GN16	S12GN32	S12GN48	S12G48	S12G64	S12G96	S12G128	S12G192	S12GA192	S12G240	S12GA240
64-pin LQFP	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
100-pin LQFP	—	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes
Supply voltage	3.13–5.5 V										
Execution speed	Static–25 MHz										

2 Non-implemented features

Some modules were not implemented on the S12G family in order to maintain the microcontroller's low cost and focus on the automotive market. These non-implemented modules include the following:

- XGATE coprocessor
- Enhanced capture timer (ECT)
- Inter-integrated circuit module (I^2C)
- Periodic interrupt timer (PIT)

Applications that currently use one or more of these modules would need to be modified to accommodate the S12G family architecture.

2.1 XGATE coprocessor

The XGATE coprocessor is typically available on microcontrollers with large banks of flash memory, such as the S12XE family. It is important to check that a program already using the XGATE fits on the S12G microcontroller's flash memory. Once this is validated, interrupt assignations need to be reallocated. The XGATE coprocessor is mainly used to manage interrupts in parallel. On the S12G, these interrupts are managed by the main core, which reduces real-time processing. The S12G family is not oriented to high processing tasks, or demanding calculations.

2.2 Enhanced capture timer (ECT)

The enhanced capture timer typically used for ABS applications works as a timer module (TIM) with some extra features. It consists of a 16-bit timer with a software-programmable counter. It can be used for waveform measurement or waveform generation. Pulse widths can vary from microseconds to many seconds.

Table 2 shows the differences between the ECT and a TIM, like the one implemented on the S12G. The main difference between the two is that the ECT has two accumulators, whereas the TIM has one. Another extra feature of the ECT is that these two 16-bit accumulators can be divided into four 8-bit independent accumulators.

Table 2. Comparison between features on ECT and TIM modules

Feature	ECT	TIM
Buffer Size	16-bit	16-bit
16-bit Pulse Accumulators	2	1
Input Capture channels	8	8
16-bit Modulus counter	1	—

Aside from these features, the ECT can be easily replaced by the TIM module since both have the same 8 channels routed to the pins, and all of them can trigger an overflow interrupt.

2.3 Inter-integrated circuit communication module (I^2C)

There are two options for migrating applications that need to communicate using I^2C: either emulate the I^2C protocol with general-purpose inputs/outputs (GPIOs) or, if possible, change the communications protocol. On an S12G, LIN, CAN, SCI, or SPI can be used to communicate with microcontrollers. For automotive applications, CAN is used frequently because it offers the EMI tolerance and bandwidth required. Most of the S12G family members (S12G48 and above) have an MSCAN module with five receive buffers, three transmit buffers, and programmable wake-up functionality. All of the S12G family members also have at least one SCI and one SPI module for serial communication with peripheral devices and other microcontrollers.

For more information on CAN communication and the MSCAN module, refer to AN3034, *Using MSCAN on the HCS12 Family*, available at www.freescale.com.

2.4 Periodic interrupt timer (PIT)

The periodic interrupt timer generates interrupts on a particular timebase in order to activate events, such as a scheduler. Since the S12G family does not have a PIT, software modifications will be required to generate these interrupts from some other source. All the S12 families have a real-time interrupt that allows the generation of an interrupt on a given frequency. But if more than one periodic interrupt is needed, the TIM can be used. Although the PIT and the TIM modules work differently, it is possible to generate periodic interrupts with a TIM module.

Figure 1 shows the block diagram of the PIT24B4C module, which has four channels and can generate four independent interrupts on different time bases. The PIT acts as countdown timer, and when each of the channels reaches zero, the corresponding interrupt is generated. Each channel has a dedicated register where the initial count of that channel is stored. There are two prescalers that tune the PIT frequency and allow the user to have more control over the periodic interrupts.

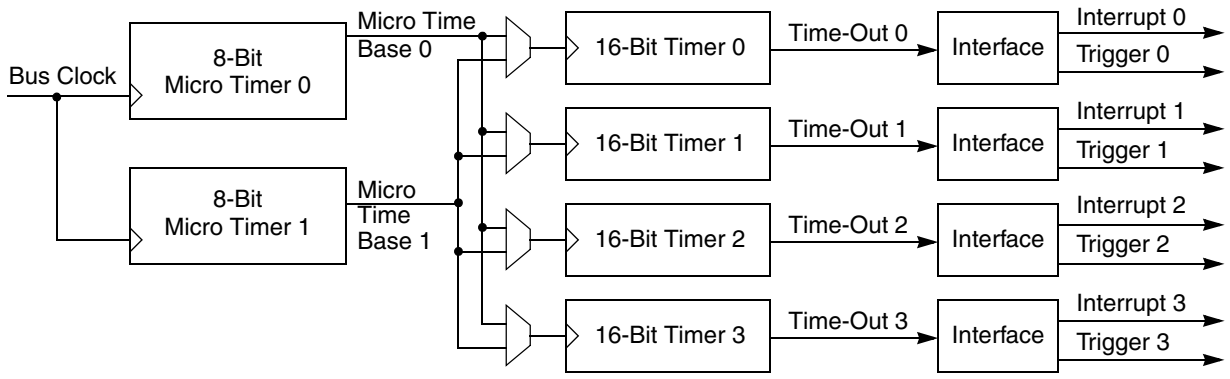

Figure 1. PIT block diagram

The TIM manages input captures and output compares, and the latter can be used to generate periodic interrupts. The block diagram for the TIM can be found on Figure 2. Unlike the PIT, the TIM is linked to physical pins on the device and is therefore configurable; this could be a desirable characteristic, depending on the application.

The TIM has an up counter that overflows constantly, which can be used to trigger an interrupt by setting a desired value on the Timer Input Capture/Output Compare Register (TCxH and TCxL) and activating an output compare. The TIM constantly compares the value of the timer with the values in TCxH and TCxL (one per channel) and generates an interrupt when the values match. Each channel can be set to a different target value and generate interrupts at different times. The TIM also has a prescaler that allows you to change the frequency for the module.

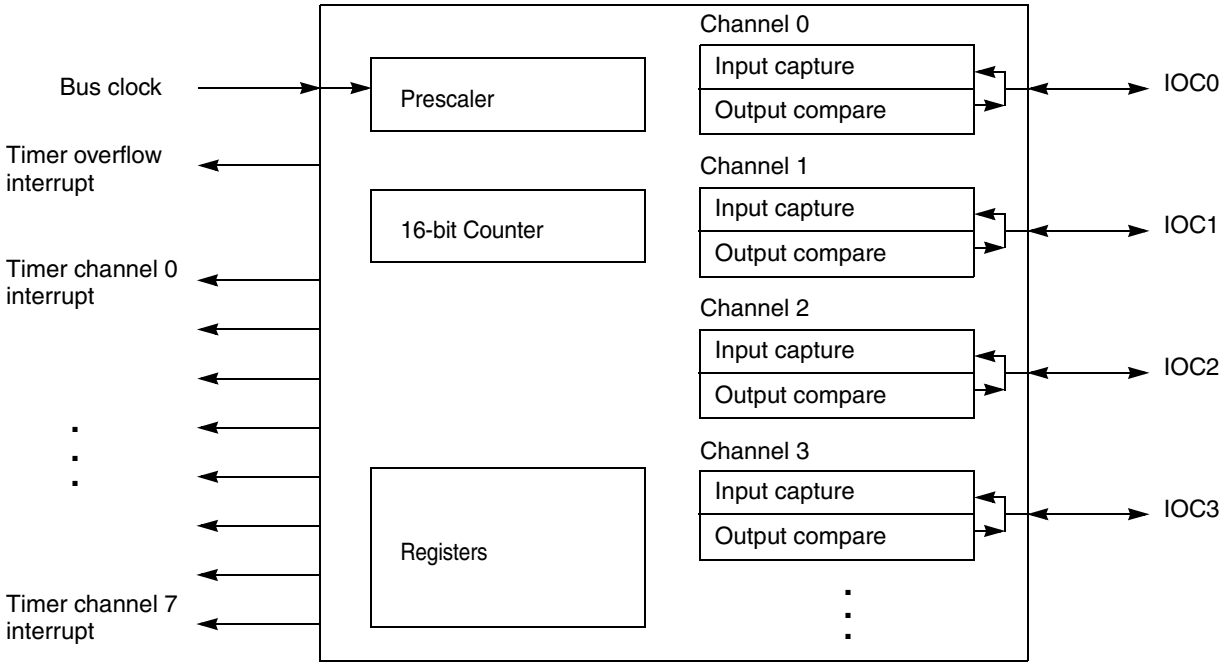

Figure 2. TIM block diagram

3 Extra features

The most remarkable features included on the S12G family are the increased analog capabilities of the larger S12Gs, such as the S12GA192 and S12GA240, where the “A” in the device name identifies the MCUs with better analog characteristics. These functionalities include a 12-bit ADC module, an 8-bit DAC module, and a Reference Voltage Attenuator (RVA) for increased ADC resolution. Since these modules are not included in all S12G devices, extra care is advised when selecting an MCU from this family.

3.1 Digital-to-analog converter (DAC)

The digital-to-analog converter (DAC) is an 8-bit module that delivers an output voltage between VRL and VRH calculated from a digital value. It is mostly used for control systems where an analog voltage is used as an input for the controlled system, as in a potentiometer. The system consists of a resistor network that generates the output voltage required and an operational amplifier (OPAMP) to buffer the DAC’s output. A block diagram of the DAC module can be found in Figure 3. The DAC’s OPAMP can be used independently by the user since its pins are directly mapped to a physical pin on the MCU, as seen in the block diagram. This is particularly useful for users who want to use OPAMP logic implementations (comparator, amplifier, summing amplifier, and so on) with a software configurable DAC voltage value.

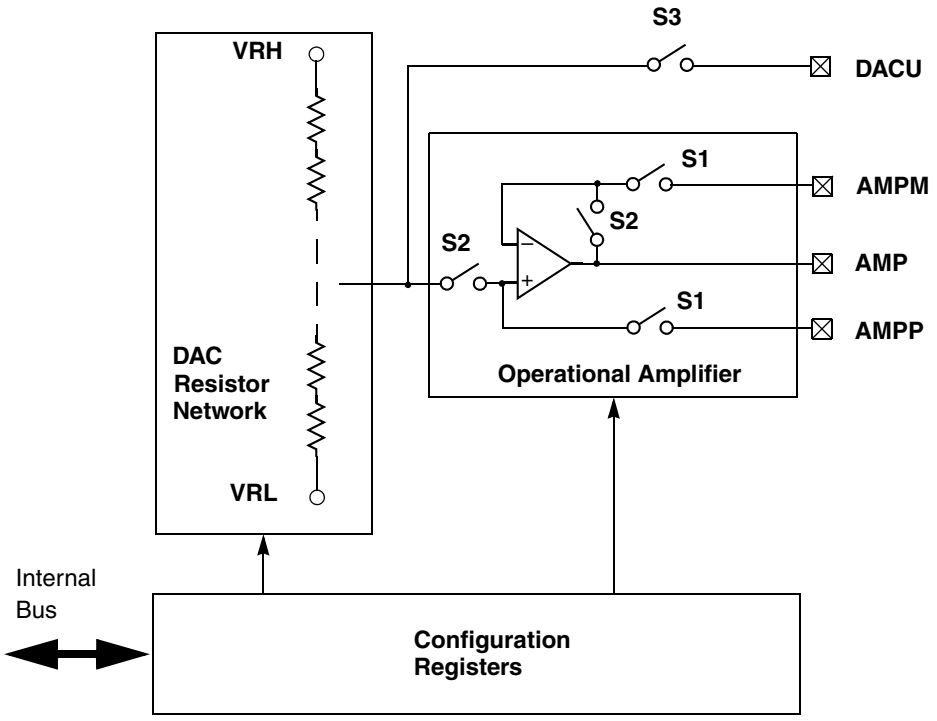

Figure 3. The DAC block diagram

3.2 Reference voltage attenuator (RVA)

The S12G family is the first to implement a reference voltage attenuator (RVA) module. This module reduces by half the reference voltage used by the ADC, improving its resolution by a factor of two. Only

two S12G MCUs have this module (which comes together with the 12-bit ADC module). Figure 4 shows the register with the only bit used to configure the RVA: the RVAON bit, which enables or disables the RVA.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	RVAON
W								
Reset	0	0	0	0	0	0	0	0

Figure 4. The RVACTL register

3.3 Analog comparator (ACMP)

Some S12G family members have an independent analog comparator (ACMP) module that provides independent external signal compare capabilities. The MCUs that have an ACMP can be found on Table 1. The analog comparator consists of an operational amplifier (OPAMP) configured as a comparator connected to an input capture channel. The ACMP has two analog input signals (ACMPP and ACMPM) and one digital output (ACMPO). Voltages within the 5V operating range of the MCU can be accepted as inputs, but the output is digital. When ACMPP is greater than ACMPM, the output is set high and vice versa (assuming the module is enabled). The output signal of the ACMP is routed to the ACMPO pin, and it can additionally be connected to an input capture channel that generates interrupts on rising edges, falling edges or toggles.

4 Clock module considerations

The S12G family's clock, reset, and power management unit (CPMU) is in charge of managing the clock source and the voltage delivered to the MCU. The CPMU has the following characteristics:

- A Pierce oscillator that provides a low-noise, low-power clock source using crystals or resonators
- Phase locked loop (PLL), a highly accurate frequency multiplier
- Internal reference clock that runs at 1 Mhz
- Voltage regulator working from 3.13 V to 5.5 V, providing a steady voltage supply
- Autonomous periodic interrupt (API)

Depending on the CPU core, the clock management module may be different from one another. The S12G and S12P families come with a CPU12 core which has a CPMU module. On families that have the CPU12X core (such as the S12XS and S12XE) the clock module is replaced by the clocks and reset generator (CRG). The CRG works very similarly to the CPMU with the exception that the CRG does not have an autonomous periodic interrupt, though it does have a clock monitor. Also, some minor differences can be found on the register names and bit distribution. In Appendix A, "CMPU vs. CRG register map," the register map for CPMU and CRG modules can be compared.

There is no major problem in migrating an application from the S08 microcontrollers since there is no dedicated module for clock or reset managements on that device. There are only isolated functionalities such as RTI (which is included in both CRG and CPMU modules) or the MCU reset flags (which are also

included on both modules). The implementation of these functionalities on the S12G is simple since only registers were moved; functionality remains the same.

In general, when making a migration to the S12G family, the main consideration regarding clock configurations is the maximum frequency achievable by the CPU. In this case the maximum is 25 MHz.

5 Memory management

5.1 EEPROM

The S12G family also includes an EEPROM memory module, an easy-to-use, non-volatile data storing mechanism. In this case, the sector is divided into only 4 bytes, which simplifies memory management, since no large memory regions are erased at once. EEPROM sizes range from 512 bytes to 4 Kbytes, depending on the S12G MCU selected.

6 Conclusion

Freescale's S12G family presents a cost efficient, high-performance alternative for applications that need small pin counts. The versatility and flexibility of this family makes it the perfect candidate for most automotive applications due to its exceptional analog characteristics and safe communication protocols. The small pin count allows the S12G's to fit small areas without sacrificing the performance of a 16-bit MCU while retaining the low power consumption and code efficiency of the 8-bit families. For more references on the modules included on each S12G MCU, please refer to the latest reference manual.

Appendix A CMPU vs. CRG register map

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0034	CPMU SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0035	CPMU REFDIV	R	REFFRQ[1:0]		0	0	REFDIV[3:0]			
		W								
0x0036	CPMU POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0037	CPMUFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	OSCIF	UPOSC
		W								
0x0038	CPMUINT	R	RTIE	0	0	LOCKIE	0	0	OSCIE	0
		W								
0x0039	CPMUCLKS	R	PLLSEL	PSTP	0	COP OSCSEL1	PRE	PCE	RTI OSCSEL	COP OSCSEL0
		W								
0x003A	CPMUPLL	R	0	0	FM1	FM0	0	0	0	0
		W								
0x003B	CPMURTI	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	CPMUCOP	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x003D	RESERVEDCPMUTEST0	R	0	0	0	0	0	0	0	0
		W								
0x003E	RESERVEDCPMUTEST1	R	0	0	0	0	0	0	0	0
		W								
0x003F	CPMU ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x02F0	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x02F1	CPMU LVCTL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								
0x02F2	CPMU APICTL	R	APICLK	0	0	APIES	APIEA	APIFE	APIE	APIF
		W								
0x02F3	CPMUACLKTR	R	ACLKTR5	ACLKTR4	ACLKTR3	ACLKTR2	ACLKTR1	ACLKTR0	0	0
		W								
0x02F4	CPMUAPIRH	R	APIR15	APIR14	APIR13	APIR12	APIR11	APIR10	APIR9	APIR8
		W								
0x02F5	CPMUAPIRL	R	APIR7	APIR6	APIR5	APIR4	APIR3	APIR2	APIR1	APIR0
		W								
0x02F6	RESERVEDCPMUTEST3	R	0	0	0	0	0	0	0	0
		W								

Figure A-1. CPMU Register Summary

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x02F7	RESERVED	R	0	0	0	0	0	0	0	0
		W								
0x02F8	CPMU IRCTRIMH	R	TCTRIM[4:0]					0	IRCTRIM[9:8]	
		W								
0x02F9	CPMU IRCTRIML	R	IRCTRIM[7:0]							
		W								
0x02FA	CPMUOSC	R	OSCE	Reserved	OSCPINS_EN	Reserved				
		W								
0x02FB	CPMUPROT	R	0	0	0	0	0	0	0	PROT
		W								
0x02FC	RESERVEDCPMUTEST2	R	0	0	0	0	0	0	0	0
		W								

Figure A-1. CPMU Register Summary (continued)

Address	Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000	SYNR	R	VCOFRQ[1:0]		SYNDIV[5:0]					
		W								
0x0001	REFDV	R	REFFRQ[1:0]		REFDIV[5:0]					
		W								
0x0002	POSTDIV	R	0	0	0	POSTDIV[4:0]				
		W								
0x0003	CRGFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	ILAF	SCMIF	SCM
		W								
0x0004	CRGINT	R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		W								
0x0005	CLKSEL	R	PLLSEL	PSTP	XCLKS	0	PLLWAI	0	RTIWAI	COPWAI
		W								
0x0006	PLLCTL	R	CME	PLLON	FM1	FM0	FSTWKP	PRE	PCE	SCME
		W								
0x0007	RTICTL	R	RTDEC	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x0008	COPCTL	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W			WRTMASK					
0x0009	FORBYP[2]	R	0	0	0	0	0	0	0	0
		W								
0x000A	CTCTL[2]	R	0	0	0	0	0	0	0	0
		W								
0x000B	ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure A-2. CRG Register Summary

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