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Application Note

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Migration Differences Between MPC5604B/C / SPC560B/C4 512 K Cut 1 to Cut 2

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1 Introduction

Freescale and ST Microelectronics have created an e200Z0 core-based Power Architecture family of devices targeted at automotive body applications. The part numbering scheme is slightly different, depending on whether the device is produced by Freescale or ST as below. Note these devices feature 512 Kbytes of Flash memory.

- Freescale — MPC5604B / MPC5604C
- ST — SPC560B4 / SPC560C4

This document details the changes that have been implemented going between Cut 1.1 and Cut 2 of the device.

Reading this document will expedite migration time for customers, who are currently using Cut 1.1 silicon and will require to migrate to the Cut 2 device.

Contents

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This document is not intended to replace the reference manual or device errata list and differences pointed out in this document should be cross referenced with the relevant sections in the latest reference manual and errata document.

The table below shows the full part numbers and device identification for each device from each silicon vendor.

Table 1. Device Identification

Device Manufacturer	Part Numbers	Maskset		JTAG ID	
		Cut 1.1	Cut 2	Cut 1.1	Cut 2
Freescale	MPC5604B, MPC5604C	2M07N	0M27V	0x1AE4001D	0x0AE4101D
ST Microelectronics	SPC560B4, SPC560C4	FB50X11Z	FB50X20B	0x1AE40041	0x0AE41041

For simplicity throughout this document, the MCU will be referred to as the MPC5604B.

For differences between the B and C variants, please consult the reference manual.

2 Summary of Differences

This section gives a summary of all the differences between the MPC5604B 512 K flash size silicon revisions Cut 1.1 and Cut 2. These differences are described in more detail in the following sections. For ease of navigation, the section number provides a link to the appropriate section.

Table 2. Summary of Differences

Description	Cut 1.1	Cut 2	Section
SRAM size increase	32 K SRAM	48 K SRAM	3.1
Additional GPIO on JTAG pins	Dedicated JTAG pins	Added PH[9] and PH[10] to TMS and TCK	4.1
Medium speed pad allocation		27 additional medium pads	4.2
GPIO state during and after reset	High-Z in reset, then input with weak pull-up	High-Z during and after reset except JTAG and ABS pins	4.3
Debug through LPM	Not supported	Supported	5.1
JTAG operation in safe mode	JTAG pins tri-state by default in SAFE mode	SMC modified, so JTAG pins remain active in SAFE mode	5.2
Nexus TAP change		Change to TAP command	5.3
Peripheral Clock Prescalers	Disabled out of reset	Enabled out of reset	6.1
ADC register map change		Fundamentally different to Cut 2. Code change required.	6.2
ADC additional external result register	Four external results registers for ANX[0..3]	32 external results registers covering full external mux	6.3

Table 2. Summary of Differences (continued)

ADC multiplex control		Additional pad-multiplexing options.	6.4
ADC clock prescaler divider	Set to sysclk / 2	Option to use sysclk / 2 when in LPM on 16 MHz IRC	6.5
ADC Abort	Slow abort for chained commands	New “abortchain” control bit added for rapid abort.	6.6
ADC offset calculation	Implemented	Removed. Did not provide any benefit to ADC precision.	6.7
LINFlex Configuration change	All four LINFlex modules support master / slave	LINFlex 0 is master /slave, all others are master only	6.8
LINFlex slave filters	Eight ID filters on LINFlex0	16 ID filters on LINFlex0	6.9
eMIOS additional modes and channel types	Eight modes and three channel types	Added two more channel types with four more modes	6.10
RCHW format	0x0000_005A	0x005A_0000	7.1
Correct reset event disable	Can disable all reset sources in DERD / FERD	Allow ability to lock all reset config registers	7.2
Protection of reset event disable registers	Write-once protection based on 32-bit resolution	Individual 16-bit protection for DERD / FERD	7.3
Unused BAM space abort	Non-BAM code not set to 0x0 so no exception	Non-BAM ROM areas set to 0x0 to force exception	7.4
Invalid clock selection inhibit	System hang, if access clock gated peripheral	No system hang, if access peripheral with clock disabled	8.1
RTC counter update	RTC has to be stopped before updating compare value	Allow RTC compare value to be changed without halting the counter	8.2
RTC operation through non-destructive reset	RTC stops and is reset during reset period	RTC continues to run through non-destructive and watchdog resets	8.3
External 32 kHz Oscillator	Not functional	Functional	8.4
CTU source update		Add Ch24 and Ch48 as trigger sourced for ADC	9.1
CTU PIT / eMIOS configuration	eMIOS ch23 to CTU_23, PIT_3 to CTU_28	eMIOS ch23 not mapped. PIT_3 moved to CTU ch23	9.2
API/RTC Wakeup Source	API/RTC shared wakeup source zero	API wakeup source zero and RTC wakeup source one	10.1
Halt mode defect	Cannot enter Halt	Halt mode working correctly	10.2
Standby mode exit flash control	In RGM_STDBY	In ME_DRUN_MC register	10.3
Vreg power-on current clamp	No current clamping	Current clamp set to 200 mA	10.4

3 Memory and Memory Control

3.1 SRAM Size

The MPC5604B Cut 1.1 MCU has 32 Kbytes of SRAM. This has been increased on the Cut 2 MCU to 48 Kbytes. The additional SRAM has been added below the existing 32 Kbyte block to create a contiguous 48 K block on Cut 2.

Table 3. SRAM Size Differences

Silicon Revision	SRAM Memory		
	Start Address	End Address	Size
MPC5604B Cut 1.1	0x4000_0000	0x4000_7FFF	32 Kbytes
MPC5604B Cut 2	0x4000_0000	0x4000_BFFF	48 Kbytes

CAUTION

When using the Cut 2 device, you need to ensure that the RAM-initialisation routine is modified to include the additional memory space, in order to avoid any ECC errors when reading from the SRAM. Even a 16-bit write could cause an ECC error, as it is implemented as a 32-bit read-modify write in order to update the ECC.

4 Pin Configuration

4.1 Additional GPIO on JTAG Pins

In order to provide additional two GPIO pins, the MPC5604B Cut 2 device allows the JTAG TCK and TMS pins to be re-assigned as GPIO. Two new ports, PH[9] and PH[10], have been created for this purpose.

Table 4. JTAG Pins

Silicon Revision	JTAG Pin Assignment	
	TMS	TCK
MPC5604B Cut 1.1	TMS	TCK
MPC5604B Cut 2	TMS or PH[9]	TCK or PH[10]

By default, PH[9] and PH[10] are assigned as JTAG, and the customer must re-configure these to be GPIO in the SIU pad configuration register (see the reference manual for details).

There are some limitations that you must be aware of:

- The functionality of PH[9] and PH[10] cannot be debugged using a JTAG debug interface.
- If external application hardware is connected to PH[9] or PH[10], this may interfere with JTAG signals, making it impossible to enter debug mode without disconnecting the external hardware. This could be solved with an external multiplexer or jumpers.

- Setting the SIU to GPIO on PH[9] or PH[10] will prevent communication with the debugger, so debugging normal application code is impossible after the PCR of PH[9] or PH[10] has been modified to GPIO. These pins can only be set back to TCK/TMS via software (in other words, this cannot be done automatically by a JTAG debugger).

NOTE

All references to JTAG are also applied to Nexus and these pins impact both JTAG and Nexus debug, as the signals are used in both interfaces.

4.2 Medium Speed Pad Allocation

The MPC5604B Cut 2 device has additional medium speed pads, in order to support a larger number of high-drive current pads (medium speed pads support 3.8 mA, whereas the slow pads support 2 mA). The table below shows the pads that have been changed from slow pads on Cut 1.1 to medium / slow pads on Cut 2.

Table 5. Additional Medium Speed Pads

Pad	Pad	Pad	Pad	Pad	Pad	Pad
PA[5]	PC[12]	PE[5]	PF[12]	PG[7]]	PG[15]	PH[6]
PB[2]	PC[15]	PE[6]	PG[2]	PG[11]	PH[0]	PH[7]
PC[0]	PE[1]	PE[15]	PG[4]	PG[12]	PH[3]	PH[8]
PC[4]	PE[2]	PF[10]	PG[6]	PG[13]	PH[4]	

Note that not all of these pads are available in all packages! Consult the device reference manual for details. This gives a total of 40 medium speed pads in the 144 QPF package and 25 medium speed pads in the 100 QFP package.

Customers must be careful of the number of pads that are switched together with the resulting increase in current. The sum of the current on each pad segment must not exceed the maximum current, as defined in the device datasheet.

4.3 Input/Output State During and After Reset

On Cut 1 devices, the input/output pins are set to high impedance (tri-stated) during reset. Once reset has been released, the input/output pins are set to input with weak pull-ups enabled.

On Cut 2 devices, the input/output are set to high impedance during reset and remain in this state, once the reset has been released.

Table 6. I/O State During and After Reset

Silicon Revision	Input/Output Pins During Reset	Input/Output Pins After Reset
MPC5604B Cut 1.1	High Impedance	Input, weak pull-up
MPC5604B Cut 2	High Impedance	High Impedance except JTAG and ABS that are input, weak pull-up

The following pins are critical to boot operation and are not in high-impedance state during reset:

- PA[9] (FAB) is pull-down. Without external strong pull-up the device starts fetching from flash.
- PA[8] (ABS) is pull-up.
- RESET pad is driven low. This is pull-up only after PHASE2 reset completion.
- JTAG pads (TCK, TMS, and TDI) are pull-up, whilst TDO remains tri-state.
- Nexus output pads (MDO[n], MCKO, EVTO, MSEO) are forced to output.

4.4 GPIO Pin Configuration in Standby Mode

On Cut 2 devices, if GPIO pull-ups are active on standby entry, the pull-up will remain active on standby exit, until such a point as the pull-up is cleared by software.

5 Debug

5.1 Debug Through LPM

It is desired that there is debug capability right up the point the MCU enters low-power mode, and that debug capability is re-initiated as soon as the MCU starts to wake up.

Debug handshaking has been added to Cut 2 to notify the debugger that a low-power mode entry is about to take place. This allows the debugger to cease communication with the MCU during low-power mode without any errors. Similarly, once the MCU starts to wake up, handshaking is used to inform the debugger of the wakeup. With the debugger attached, transition from low-power mode can only be completed once the debugger has acknowledged the wakeup.

5.2 JTAG Operation in SAFE Mode

On Cut 1 devices, the default state of the SMC (Safe Mode Control) bits in the PCR (Pad Configuration Registers) defaults to zero. This means that when the MCU enters SAFE mode, the device pins are tri-stated. If a debugger is connected at this point, then the debug session is terminated as soon as the pins tri-state.

On Cut 2 devices, the SMC bit for the JTAG pins defaults to one after reset. This keeps the JTAG pins alive in safe mode, thus allowing debug through safe mode by default.

Table 7. JTAG Pins SMC Control

Silicon Revision	Default PCRx_SMC state	Comments
MPC5604B Cut 1.1	0	JTAG pins disabled in safe mode
MPC5604B Cut 2	1 for JTAG pins	JTAG pins active in safe mode

5.3 Nexus Configuration

The information in this section is only applicable to customers who are working with the NPC (Nexus Port Controller), for example a JTAG-based flash-programming solution. Most development tool vendors have already implemented this change for Cut 2.

On Cut 1.1 devices, the following TAP controller commands are in place:

- ACCESS_AUX_TAP_ONCE 10001 Grants the platform ownership of the TAP.
- ACCESS_AUX_TAP_NPC 10010 Grants the Nexus Port Controller (NPC) ownership of the TAP.

On Cut 2 Devices, these commands are modified to be in-line with previous eSYS devices with:

- ACCESS_AUX_TAP_ONCE 10001 Grants the platform ownership of the TAP.
- ACCESS_AUX_TAP_NPC 10000 Grants the Nexus Port Controller (NPC) ownership of the TAP.

6 Peripherals

6.1 Peripheral Clock Prescalers

On Cut 1.1 devices, the system clock divider enable bits DE0, DE1, and DE2 within the System Clock Divider Configuration Registers are cleared out of reset. This means that any attempt to access an off-platform peripheral without enabling the relevant clock divider will result in a system crash.

On Cut 2 devices, the system clock divider enable bits are set out of reset to enable all the peripheral clock prescalers.

Table 8. System Clock Dividers

Silicon Revision	DE0, DE1, DE2 in GCM_SC_DC[0..2]	Implications
MPC5604B Cut 1.1	Cleared out of reset	System clock to peripherals is disabled out of reset
MPC5604B Cut 2	Set out of reset	System clock to peripherals is enabled out of reset

6.2 ADC Register Map Change

The ADC memory map and register description has fundamentally changed between Cut 1.1 and Cut 2 devices. This was to bring the ADC implementation more in-line with the format of other peripherals (for example including a Module Configuration Register).

Migrating ADC code between Cut 1.1 and Cut 2 requires a code re-write to use the new register and bit field names. There is a new header file available to support the new interface on Cut 2.

There are also some functional changes to the ADC going from Cut 1.1 to Cut 2 that are detailed in the next three sections.

6.3 ADC Additional External Result Registers

The ADC has four external channels ANX[0..3]. These can be used with four external 8-bit multiplexers (controlled by the MA[0..2] bits) to provide up to 32 extended ADC channels.

Cut 1.1 devices have a single result register for each of the four external ADC channels.

On Cut 2 devices, there are 32 external results registers, so there is a unique results register for each supported external channel. The results are automatically stored in the appropriate external channel, thus allowing the user to treat an externally multiplexed channel in the same manner as an internal channel.

Table 9. RGM_DERD and RGM_FERD Write-Once Protection

Silicon Revision	External Multiplexed Channels	Implications
MPC5604B Cut 1.1	Four results registers, one per ANX[0..3] channel.	Need to read result register before another channel on same external multiplexer is used again.
MPC5604B Cut 2	32 results registers, one for each potential externally-multiplexed channel.	External ADC channels can be treated the same as internal channels in software.

6.4 ADC Multiplex Control

On Cut 1 devices, the ADC multiplexer pins, MA[0..2], are brought out in two possible positions, as detailed in the table below.

On Cut 2 devices, an additional pad multiplexing for MA[0] and MA[1] has been added.

Table 10. MA[0..2] Pad Multiplexing Locations

Register Bits	Description	Alternate Function	MPC5604B Cut 1.1	MPC5604B Cut 2
MA[0]	PE7	AF3	•	
	PH8	AF3	•	•
	PC3	AF2	--	•
MA[1]	PE6	AF3	•	•
	PH7	AF3	•	•
	PC10	AF3		•
MA[2]	PE5	AF3	•	•
	PH6	AF3	•	•

6.5 ADC Clock Prescaler Divider

On Cut 1.1 devices, the ADC clock prescaler has a fixed divide ratio of system clock / 2. This gives a minimum conversion time of 2 µS when running from the 16 MHz IRC. If the device is in the dynamic stage of a low-power sequence, this will extend the time that the user has to stay operational, rather than in a LP mode, so increasing the average power consumption.

To address this problem on Cut 2 devices, an ADCCLKSEL (ADC Clock Frequency Select) bit was added to the ADC_MCR (Main Configuration Register). This bit can be written to set the ADC clock to the system frequency.

Table 11. ADC Clock Prescaler

Silicon Revision	ADC Clock Prescaler	ADC Clock
MPC5604B Cut 1.1	Hard Wired	sys_clk / 2
MPC5604B Cut 2	ADCCLKSEL = 0	sys_clk / 2
	ADCCLKSEL = 1 *	sys_clk

* The configuration of ADC clock = system clock is only valid for LPM wakeup when running on the 16 MHz IRC. The ADCCLKSEL bit can ONLY be written in ADC power down mode. In all other cases, the ADC clock should be set to system clock / 2.

6.6 ADC Abort Modification

On Cut 1.1 devices, if an ADC conversion chain is to be aborted, this does not happen immediately. All conversions of the chain need to be aborted individually, resulting in a delay before a new conversion chain can be issued.

On Cut 2 devices, an “ABORTCHAIN” bit has been added to the ADC_MCR (Main Configuration Register). The exact behavior is dependent on the Mode bit. In summary, setting the ABORTCHAIN bit immediately aborts all conversion chains. As soon as a new conversion is requested, the ABORTCHAIN bit is automatically cleared. Depending on mode, an ECH (end of chain) interrupt is generated and the NSTART and JSTART bits are also cleared. For more details consult the device reference manual.

Table 12. ADC Conversion Chain Abort

Silicon Revision	Chain Abort Mechanism
MPC5604B Cut 1.1	Individual abort for each conversion
MPC5604B Cut 2	Immediate via ABORTCHAIN

6.7 ADC Offset Calculation

Cut 1.1 devices have an ADC offset calculation mechanism. This was proven not to improve the overall ADC performance, as the intrinsic ADC precision is better than the offset calculation resolution.

The offset calculation mechanism has been removed for Cut 2 devices.

6.8 LINFlex Slave Configuration Change

Cut 1.1 devices have LIN slave features on all of the four LINFlex modules (each slave port has eight identifiers filters).

On Cut 2 devices, there is only one LINFlex module (LinFlex 0) that provides slave functionality. The remaining three LINFlex modules have been changed to master only.

Table 13. LINFlex Configuration

Silicon Revision	LINFlex 0		LINFlex 1		LINFlex 2		LINFlex 3	
	Master	Slave	Master	Slave	Master	Slave	Master	Slave
MPC5604B Cut 1.1	•	•	•	•	•	•	•	•
MPC5604B Cut 2	•	•	•	--	•	--	•	--

Customers must ensure that if they are using the LINFlex in slave mode on Cut 1.1, the application code will need to be changed, if this was not using LINFlex channel zero.

6.9 LINFlex Slave Filters

Cut 1.1 devices had eight identifier (ID) filters on all of the four LINFlex channels (all channels supported slave mode).

On Cut 2 devices, LINFlex channel zero (the only channel supporting slave mode) has had the number of ID filters increased from eight to 16.

Table 14. LINFlex Slave Filters

Silicon Revision	LINFlex 0	LINFlex 1	LINFlex 2	LINFlex 3
MPC5604B Cut 1.1	Eight ID Filters	Eight ID Filters	Eight ID Filters	Eight ID Filters
MPC5604B Cut 2	16 ID Filters	N/A (Master Only)	N/A (Master Only)	N/A (Master Only)

6.10 eMIOS Additional Modes and Channel Types

The eMIOS on Cut 1 devices supports eight different operating modes via three different channel types (X, Y, and F).

On Cut 2 devices, two additional channel types (G and H) have been added to support additional four modes, as detailed in the table below.

Table 15. eMIOS Modes

Mode Description	Mode Name	Existing channels on Cut 1.1 (and Cut 2)			New additional channels on Cut 2	
		Type X	Type Y	Type F	Type G	Type H
General Purpose Input/Output	GPIO	•	•	•	•	•
Single Action Input Capture	SAIC	•	•	•	•	•
Single Action Output Compare	SAOC	•	•	•	•	•
Modulus Counter	MC	•	--	--	--	--
Modulus Counter Buffered (Up/Down)	MCB	•	--	--	•	--
Output Pulse width and Frequency Modulation (Buffered)	OPWFMB	•	--	--	•	--
Output Pulse Width Modulation (Buffered)	OPWMB	•	•	--	•	•
Output Pulse Width Modulation Trigger	OPWMT	•	•	--	•	•
Additional Modes supported only on Cut 2 via new channels						
Input Pulse Width Measurement	IPWM	--	--	--	•	•
Input Period Measurement	IPM	--	--	--	•	•
Double Action Output Compare	DAOC	--	--	--	•	•
Center-aligned Output PWM Buffered with dead-time insertion	OPWMCB	--	--	--	•	--

On Cut 2 devices, the new channel types are implemented as follows:

- eMIOS 0 ch1-7, channel type G
- eMIOS 0 ch9-15, channel type H
- eMIOS 1 ch9-15, channel type H

For more details on the specifics of each mode and channel groupings, consult the device reference manual.

7 Reset and BAM

7.1 Reset Configuration Halfword (RCHW)

The RCHW (Reset Configuration Half Word) has been changed from being in the lower to the upper 32-bits of the address space, as defined in the table below.

Table 16. RCHW Differences

Silicon Revision	RCHW Format
MPC5604B Cut 1.1	0x0000_005A
MPC5604B Cut 2	0x005A_0000

The user must ensure that the flash RCHW is updated. Otherwise a valid RCHW will not be found and the device will not successfully boot from flash.

7.2 Correct Reset Event-Disable Feature

On Cut 1.1 devices, it was possible to disable all reset events by writing to the RGM_FERD and RGM_DERD bits. This was never intended as a supported mode of operation, since it is not desirable to be able to lock out all reset sources.

On Cut 2, the distribution of reset sources in the DERD and FERD registers has been changed as shown in the table below. In addition, the DERD register has been set to read-only, so the reset sources within DERD cannot be disabled.

Table 17. Reset Event Disable via RGM_DERD and RGM_FERD

Register Bits	Description	MPC5604B Cut 1.1	MPC5604B Cut 2
RGM_FERD (Functional Event Reset Disable Register)			
D_EXR	Disable External Reset	--	Read Only
D_Flash	Disable code or data flash error reset	•	•
D_LVD45	Disable 4.5 V LVI detected reset	•	•
D_CMU0_FHL	Disable CMU0 Clock higher / lower than ref	•	•
D_CMU0_OLR	Disable Oscillator freq lower than reference	•	•
D_PLL / D_FMPLL	Disable PLL0 fail reset (Cut 1.1) Disable FMPLL fail reset (Cut 2)	•	•
D_CHKSTOP	Disable checkstop reset	--	Read Only
D_Soft	Disable Software reset	--	Read Only
D_Core	Disable Core reset	•	•
D_JTAG	Disable JTAG-initiated reset	•	•
RGM_DERD (destructive Event Reset Disable Register)			
D_LVD27		--	Read Only
D_SWT		•	Read Only
D_LVD12_PD1		--	Read Only
D_LVD12_PD0		--	Read Only

Note that the RGM_FERD and RGM_DERD registers are ‘write-once’. For details on a change that was made to this implementation between Cut 1.1 and Cut 2 devices, see the following section.

For further details on the FERD and DERD registers, consult the device reference manual.

7.3 Write-Once Protection of Reset Configuration Registers

On Cut 1.1 devices, the RGM_DERD and RGM_FERD registers are configured such that write-once protection to these registers is provided as a 32-bit block. Thus, any write to the DERD or FERD register (be it 16-bits or otherwise) will prevent further writes to either register. The only way to correctly configure this is to write to the DERD and FERD registers in a single 32-bit write.

On Cut 2 devices, the mechanism has been changed such that the RGM_DERD and RGM_FERD registers each have their own 16-bit write-once mechanism. This is somewhat irrelevant, since the DERD register has been set to read-only in Cut 2, however it means that any attempt to write to DERD will not impact the write-once mechanism for FERD.

Table 18. RGM_DERD and RGM_FERD Write-Once Protection

Silicon Revision	Write Protection Mechanism	Implications
MPC5604B Cut 1.1	Any write to DERD or FERD would write-protect both registers.	If configuring both registers, need to do so with single 32-bit write.
MPC5604B Cut 2	Individual 16-bit protection on each register.	Write to DERD (read-only) will not block subsequent write to FERD.

7.4 Unused BAM Space Abort

The MPC5604B BAM code is implemented as an 8 K ROM block at the bottom of the memory map (0xFFFF_C000 to 0xFFFF_FFFF). The BAM code itself is considerably smaller than the 8 K ROM block. It is desirable to trap any attempt to execute non-BAM code within this ROM block. In Power Architecture, an instruction with all bits set to zero is defined as an illegal instruction, which can be trapped.

On Cut 1.1 devices, non-BAM locations were left as non-zero, so if the PC was set to a non-BAM location within the ROM block, an undefined operation would result.

On Cut 2 devices, unused locations within the ROM block have been set to zero, to any attempt to execute from within this area will result in an exception.

This has no real impact for customer code, but is listed here in the case customers notice the change to the BAM and are concerned that there is a functional change in the BAM code.

8 Clocks (Including RTC)

8.1 Invalid Clock Selection Inhibit

On Cut 1.1 devices, whenever an attempt was made to access a peripheral that had the peripheral clock disabled, the system hung with no response.

On Cut 2 devices, this has been fixed such that the system no longer hangs. If the RAE bit is set within the SSCM_ERROR register, then the user will be notified of an access problem with an IVOR2 exception. The clock status of each peripheral (enabled or disabled) can be determined by reading the ME_PSx registers.

Table 19. Unclocked Peripheral Behavior

Silicon Revision	Behavior on Accessing Unclocked Peripheral
MPC5604B Cut 1.1	Non-recoverable system hang.
MPC5604B Cut 2	System does not hang. User notified via IVOR2 exception.

8.2 RTC Counter Updates

On Cut 1.1 devices, the RTC has to be halted (by writing to the CNTEN bit in the RTC Control register) before the RTC compare value (RTCVAL) is changed. This not only stopped the counter, but also had the effect of resetting the counter.

A modification has been made on Cut 2 devices, so that the RTCVAL can be changed without halting the counter.

Table 20. Real-Time Counter

Silicon Revision	Change RTCVAL	Comments
MPC5604B Cut 1.1	Halt Counter, then change RTVAL	Counter is reset when CNTEN is cleared
MPC5604B Cut 2	Change RTVAL when counter is running	No need to stop counter

NOTE

For customers who have written code to change the counter value in Cut 1.1, you need to be careful of the fact that the counter is reset when CNTEN is cleared. On Cut 2 you may get a timer compare almost immediately after modifying the RTVAL.

8.3 RTC Operation Through Non-Destructive Reset

On Cut 1.1 devices, when a non-destructive reset (for example a functional reset or watchdog reset) is issued, the RTC (real-time clock) is reset.

On Cut 2 devices, the clocking circuitry has been changed so that the RTC will continue to run and keep time through a non-destructive reset.

Table 21. RTC Operation Through Non-Destructive Reset

Silicon Revision	RTC Behavior	Implications
MPC5604B Cut 1.1	RTC is reset	Loss of time keeping
MPC5604B Cut 2	RTC continues to run	No loss of time keeping

8.4 External 32 kHz Oscillator

On Cut 1.1 devices, there was a fault, which prevented the 32 kHz external oscillator from functioning. This has been fixed on Cut 2 devices so an external 32 kHz oscillator can be used. For a list of devices that have been qualified to function correctly, consult the device reference manual and datasheet.

9 CTU (Cross Triggering Unit)

9.1 CTU Source Update

The Cross Triggering Unit (CTU) provides a mechanism for an eMIOS or PIT timer event to synchronize an ADC conversion. The CTU provides the ADC a channel number to define which channel triggers the conversion.

On Cut 2 devices, channel 24 of eMIOS_0 and eMIOS_1 has been added as a trigger source for the ADC. These channels, both type X, support OPWMT mode, which can be used in conjunction with the ADC for lighting applications.

Table 22. Additional CTU Sources

Silicon Revision	Additional CTU Channels	CTU Source Number
MPC5604B Cut 2	eMIOS_0 Channel 24 (Type X)	24
	eMIOS_1 Channel 24 (Type X)	48

For full details of the CTU channels consult the device reference manual, where is a table showing all of the CTU channel sources.

9.2 CTU PIT / eMIOS Configuration Change

On Cut 1 devices, the PIT_3 is mapped to CTU channel 28 and eMIOS_0 channel 23 is mapped to CTU channel 23.

On Cut 2 devices, PIT_3 has been moved to CTU channel 23.

Table 23. CTU PIT Trigger Source

Silicon Revision	CTU Channel 23	CTU Channel 28
MPC5604B Cut 1.1	eMIOS_0 Channel 23	PIT_3
MPC5604B Cut 2	PIT_3	Reserved

For the full CTU trigger source mapping, consult the device reference manual.

10 Power, Low Power, and Wakeup

10.1 API / RTC Wakeup Source

On Cut 1 devices, the RTC and API shared the same wakeup source.

On Cut 2 devices, the API is wakeup source zero and the RTC is wakeup source one.

Table 24. Wakeup Sources

Silicon Revision	Source Zero	Source One
MPC5604B Cut 1.1	Shared API/RTC	PA0*
MPC5604B Cut 2	API	RTC

*Note that the Cut 1.1 wakeup source one, PA0, has been replaced by the RTC on Cut 2 devices. PA0 wakeup has been moved to the end of the wakeup table. All other wakeup sources remain the same between revisions. If you were using the API, RTC, or PA0 wakeup sources, then you need to ensure that Cut 2 device code takes account of these changes. Consult the device reference manual for the full wakeup source list.

10.2 Halt Mode Defect Fixed

Cut 1 devices have a problem entering Halt mode due to synchronization problem. This has been fixed on Cut 2 devices.

10.3 Standby Mode Exit Flash Control

The DFlash and CFlash can be independently controlled to be enabled on exit from standby mode (entry into DRUN mode). The mechanism for this is different between Cut 1.1 and Cut 2 devices.

On Cut 1.1, the DFlash and CFlash enable out of standby are controlled via the DRUN_DFLA and DRUN_CFLA bits in the RGM_STDY register.

On Cut 2, the DFlash and CFlash DRUN entry state after Standby mode are controlled via the DFLAON and CFLAON bits in the ME_DRUN_MC register.

Table 25. Standby Mode Exit Flash Control

Silicon Revision	Enable DFLASH	Enable CFLASH
MPC5604B Cut 1.1	DRUN_DFLA bit in RGM_STDY register	DRUN_CFLA bit in RGM_STDY register
MPC5604B Cut 2	DFLAON bit in ME_DRUN_MC register	CFLAON bit in ME_DRUN_MC register

10.4 Voltage Regulator Powerup Current Clamping

On Cut 1.1 devices, there is a potential issue when exiting standby mode, whereby the voltage regulator can draw a large current spike. This current draw was not regulated and required sizeable bulk storage capacitors on the customer board to prevent the voltage dipping with potential reset consequences.

On Cut 2 devices, the voltage regulator has been current-clamped to 200 mA, so the bulk-storage capacitors on the customer board can be smaller and more optimized.

Note that hardware designed for Cut 1.1 will be fully functional with Cut 2 devices, but if the bulk capacitors have been reduced for Cut 2 hardware, this hardware will not support Cut 1.1.

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