

Freescale Semiconductor

Application Note

Document Number: AN3442 Rev. 0, 09/2007

MPC7410 Package Options

by Allen Christenson. NCSG Linda Bal, NCSG Freescale Semiconductor, Inc. Austin, TX

The purpose of this application note is to discuss the packaging options available for the MPC7410 product family. The original Ceramic Ball Grid Array (CBGA) package is scheduled for end-of-life (EOL) in mid-2008; this application note covers other packaging options for MPC7410 designs. The packages are described along with details of differences between the two primary package styles. Design and package migration implications are addressed in this document.

1 References

The following documents contain related information on the MPC7410 packages. The latest *MPC7410 Hardware Specification* information supersedes any information in this Application Note.

- MPC7410 RISC Microprocessor Hardware Specifications, Rev. 6 or later (Document Number: MPC7410EC). Referred to as the "MPC7410 Hardware Specification" in this document.
- *Chip Errata for the MPC7410* (Document Number: MPC7410CE).

Contents

1.	References	
2.	MPC7410 Packages 2	
3.	Differences Between CBGA and HCTE Packages 2	
4.	Package Compatibility 6	
5.	System Design Considerations 6	
6.	Revision History 8	



© Freescale Semiconductor, Inc., 2007. All rights reserved.



MPC7410 Packages

- Manufacturing with the Land Grid Array Package (Document Number: AN2920).
- General Soldering Temperature Process Guidelines (Document Number: AN3300).

2 MPC7410 Packages

The MPC7410 is available in several packages as shown in Table 1. The Ordering Information section of the *MPC7410 Hardware Specification* contains information on the part numbering nomenclature. There are normally two characters following the "7410" digits of the part number that indicate the package code of the device; those codes are shown in Table 1.

Packaging Designator in Part Number	Package Description	Comments
RX	CBGA: Ceramic Ball Grid Array	This package is scheduled for EOL in mid-2008; not recommended for new designs. C5 spheres contain lead (Pb).
НХ	HCTE_CBGA: High Coefficient Thermal Expansion Ceramic Ball Grid Array	C5 spheres contain lead (Pb).
VU	HCTE_CBGA (Lead Free C5 Spheres): High Coefficient Thermal Expansion Ceramic Ball Grid Array with Lead Free C5 Spheres	C5 spheres are lead free (Pb-Free).
VS	HCTE_LGA: High Coefficient Thermal Expansion Land Grid Array	This package does not have C5 spheres attached.

2.1 Package Options for Migrating from the CBGA Package

- The recommended replacement part for the RX (CBGA) is the HX (HCTE_CBGA) which has the same high lead (Pb) spheres as found in the CBGA package.
- The RoHS compliant recommended replacement packages are:
 - VU (HCTE_CBGA package with lead free C5 spheres) for customers requiring a lead free solder sphere package.
 - VS (HCTE_LGA package) has no solder spheres and may be attached to the printed circuit board (PCB) using either a Pb or Pb-free solder paste, depending on the system board requirements, with superior board level reliability when compared to the RX (CBGA) package. The VS package offers the most assembly-to-board process flexibility.

3 Differences Between CBGA and HCTE Packages

The difference between the end-of-life CBGA (RX) package and its HCTE (HX, VU and VS) replacements is the ceramic substrate technology. The new packages utilize a ceramic technology which has properties that provide improved board level reliability and enable the offering of RoHS compliant



parts. Parametric differences, basic package outline differences, and board level reliability are provided in this section.

3.1 Package Parameter Differences

The details of the differences between CBGA and HCTE packages are provided in Table 2.

Attribute CBGA HCTE Comments RX HX, VU, VS Package Designator and All top view package dimensions remain Dimensions the same. Key dimensions and mechanical outline of MPC7410 package options are shown in Figure 1. Refer to MPC7410 Hardware Specification, Rev 6 or later for complete package dimension information. Technology Type HTCC HITCE LTCC High Temperature High Thermal **Co-fired Ceramic** Coefficient of (Alumina) Expansion - Low Temperature **Co-fired Ceramic** Coefficient of Thermal Expansion, 12.3 6.8 · Seven times better board level reliability CTE (@23 C) based upon Freescale reliability testing. Refer to Section 3.3, "Package Reliability Data". HCTE Coefficient of Thermal Expansion more closely matched to typical PCB coefficient of thermal expansion of 14. Thermal Conductivity (W/m-K) 17 2 Effective thermal conductivity for HCTE found to be similar to CBGA based on measured data. (Similar thermal conductivity due to the copper filled vias in HCTE package between die and substrate; see Section 5.2, "Thermal Resistance") for more information. Refer to Table 3 and the MPC7410 Hardware Specification, Rev 6 or later for thermal Thermal Resistance R_{PJA} resistance information. Conductor Material Molybdenum (Mo) Copper (Cu) base 3 Conductor Resistance ($m\Omega/sq$) 8 60% lower conductor resistance for HCTE packages. Dielectric Constant (@1 MHz) 9.8 5.3 Decrease time-of-flight delay in HCTE

Table 2. MPC7410 CBGA vs. HCTE Differences

75

175

280

350

package by 25%.

Young's Modulus (GPa)

Bending Strength (MPa)



Attribute	CBGA	HCTE	Comments
Moisture Sensitivity Level	MSL1 260ºC	MSL1 260ºC	
Substrate Color	Purple	Light Green	

Table 2. MPC7410 CBGA vs. HCTE Differences

3.2 Package Mechanical Outline Differences

Figure 1 illustrates the mechanical outlines and key dimensional differences for the MPC7410 packages. Refer to *MPC7410 Hardware Specification, Rev 6* or later for complete package dimension information.







3.3 Package Reliability Data

Figure 2 shows PCB temperature cycling reliability testing data (Weibull plot) for the different MPC7410 packages.



Abbreviations:

W/rr: Weibull in rank regression order. SAC: Tin Silver Copper (Pb-Free) alloy. SnPb: Tin Lead. Eta: Number of cycles to 63.2% failure. Beta: Slope of curve fit line. r^2: Goodness of fit. n/s: number of samples tested / samples still good at last read point.

Figure 2. PCB Reliability Data for MPC7410 Packages



Package Compatibility

4 Package Compatibility

- **Testing** CBGA (RX), HCTE_CBGA (HX and VU), and HCTE_LGA (VS) packages are tested to and meet the same electrical timing specifications outlined in the *MPC7410 Hardware Specification*.
- **Pin Compatibility** HCTE (HX, VU, and VS) devices are pin-pin compatible with the CBGA (RX) package. No board layout changes are required due to pin differences between the two packages. See Section 5.1, "MPC7410 Erratum 18 AVDD Filtering" for possible board layout changes related to Erratum 18 workarounds.
- **IBIS Models** Are available for both CBGA (RX) and HCTE (HX, VU, and VS) packages at www.freescale.com/support.

5 System Design Considerations

AVDD supply pin filtering and thermal solutions need to be evaluated for possible system changes when migrating from CBGA (RX) to HCTE_CBGA (HX, VU, and VS) packages.

5.1 MPC7410 Erratum 18 AVDD Filtering

Erratum 18 in the *Chip Errata for the MPC7410* document explains an internal package noise issue which affects the CBGA (RX) package. The work around includes modifying the AVDD supply pin filter circuit to remove two filter capacitors and increasing the series resistance. Erratum 18 does not apply to the HCTE (HX, VU, and VS) packages; therefore, the work around is not necessary, and the AVDD filter for HCTE (HX, VU, and VS) packages described in the *MPC7410 Hardware Specification* is necessary.

5.2 Thermal Resistance

The junction-to-ambient thermal resistance for the HCTE (HX, VU, and VS) packages is greater than the CBGA (RX) junction-to-ambient thermal resistance by approximately 11% to 16% depending upon the airflow conditions. The junction-to-board thermal resistance for the HCTE_CBGA packages (HX, VU, and VS) is greater than the CBGA (RX) junction-to-board thermal resistance by approximately 23%. Complete details are provided in the *MPC7410 Hardware Specification* and are shown in Table 3.

Because of this increased resistance to the conductivity of heat in the HCTE (HX, VU, and VS) packages, it is recommended that existing thermal solutions for CBGA (RX) packages be re-evaluated for sufficient heat dissipation in HCTE (HX, VU, and VS) applications.

	Symbol	Value			
Characteristic		CBGA (RX)	HCTE (HX, VU, and VS)	Unit	Notes
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board	$R_{ hetaJMA}$	18	20	°C/W	1, 2
Junction-to-ambient thermal resistance, 1m/sec airflow, four-layer (2s2p) board		14	16	°C/W	1, 2

Table 3. Package Thermal Characteristics



			oystem besign	i oonaid	
Table 3. Package Thermal Characteristics (continued)					
		Va			
Characteristic	Symbol	CBGA (RX)	HCTE (HX, VU, and VS)	Unit	Notes
Junction-to-ambient thermal resistance, 2m/sec airflow, four-layer (2s2p) board	R_{\thetaJMA}	13	15	°C/W	1, 2
Junction-to-board thermal resistance	R_{\thetaJB}	9	11	°C/W	3
Junction-to-case thermal resistance	$R_{ extsf{ heta}JC}$	< 0.1	< 0.1	°C/W	4

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
- 2. Per JEDEC JESD51-6 with the board horizontal.
- 3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 4. Thermal resistance between the active portion of the die and the calculated case temperature at the top of the die. The actual value of R JC is less than 0.1 °C/W.

5.3 Thermal Solution (Heat Sink) Mounting Considerations

- The CBGA (RX) and HCTE_CBGA (HX) packages drawings are the same in the MPC7410 Hardware Specification. There should be no heat sink mounting differences issues between these two packages.
- The HCTE_CBGA package with lead free C5 spheres (VU) package dimensions shown in the • *MPC7410 Hardware Specification* and Figure 1:
 - 'A' (overall side profile height from bottom plane of solder spheres to the back (top) of the die)
 - 'A1' (height from bottom plane of solder spheres to the bottom of the package substrate)
 - 'b' (solder sphere diameter)

are less than the same dimensions of the CBGA (RX) package meaning the final mounted HCTE CBGA package with lead free C5 spheres (VU) package will sit closer to the PCB after the soldering assembly process. Care must be taken to ensure the heat sink and thermal interface material is mounted to maintain firm contact with the back of the die of the VU package. Adjustments for heat sink spring clips-to-holes in the PCB and screw mounted heat sinks may be necessary. Heat sinks that spring clip to the edge of the substrate are no longer recommended due to potential substrate package deformation and may not have enough PCB to package clearance to be used in VU package designs.

While the HCTE_CBGA package with lead free C5 spheres (VU) package dimensions: 'A1' and 'b' do not apply to the HCTE LGA (VS) package (refer to MPC7410 Hardware Specification), similar post solder processing dimension concerns with respect to heat sink mounting outlined for the VU package above are applicable for the VS package.



Revision History

6 Revision History

Table 4 provides a revision history for this application note.

Table 4. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	09/06/2007	Initial release.



Revision History

THIS PAGE INTENTIONALLY LEFT BLANK



Revision History

THIS PAGE INTENTIONALLY LEFT BLANK



THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page: www.freescale.com

Web Support: http://www.freescale.com/support

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc. Technical Information Center, EL516 2100 East Elliot Road Tempe, Arizona 85284 +1-800-521-6274 or +1-480-768-2130 www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku Tokyo 153-0064 Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. Technical Information Center 2 Dai King Street Tai Po Industrial Estate Tai Po, N.T., Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 +1-800 441-2447 or +1-303-675-2140 Fax: +1-303-675-2150 LDCForFreescaleSemiconductor @hibbertgroup.com Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale[™] and the Freescale logo are trademarks of Freescale Semiconductor, Inc. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. The PowerPC name is a trademark of IBM Corp. and is used under license. IEEE nnn, nnn,nnn, and nnn are registered trademarks of the Institute of Electrical and Electronics Engineers, Inc. (IEEE). This product is not endorsed or approved by the IEEE. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc., 2007. All rights reserved.

Document Number: AN3442 Rev. 0 09/2007



