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Application Note

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Using the PowerQUICC™ II Auto-Load Feature

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The auto-load (ALD) feature is available on the PowerQUICC™ II (PQ2) family of communications processors. The ALD enables the initialization of the peripheral component interface (PCI) configuration space as the processor comes out of reset so an external PCI master can complete the PQ2 initialization sequence. However, it can be used to configure any internally-mapped register, regardless of whether PCI is used or is even available on the processor. PQ2 Pro (MPC83xx) and PQ3 (MPC85xx) product families use a different mechanism (bootloader) to implement the same function. This application note describes how to implement and use the auto-load (ALD) feature.

Contents

1 Implementing ALD

The ALD feature is indicated by a bit in the hard reset configuration word (HRCW). After the configuration master reads all reset configuration words (including place holders for slave devices that may or may not exist) in the boot ROM/flash memory, it begins its first instruction fetch but also reads a pointer to the ALD data structure. This structure includes all information to be preconfigured into the PQ2 along with an indicator to complete the auto-load activity. All functional settings configured by the ALD are enabled and active when the internal register is updated.

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1.1 Hardware Reset Configuration Word

The PQ2 processor uses a hardware reset configuration word that is read from the boot memory (device controlled by $\overline{CS0}$) to determine several configuration options as the processor comes out of reset. Refer to the reset section of the appropriate reference manual for the physical location in the memory device, along with the format of the hardware reset configuration word. Setting bit 26 enables the auto-load sequence. The reference manual describes this as “CP auto-load” because the sequence is performed by the RISC processor of the communications processor module (CPM) during the reset sequence. However, there are no special dependencies to set up or initialize the CPM to perform the function, nor are there any special cleanup procedures for subsequent CPM activity. Although PCI is mentioned in the description, the LBPC setting does not have to indicate PCI. As noted earlier, the ALD function can be used for non-PCI initialization. The addressing defined by the ISB and BMS bits in the HRCW is important for the specific contents of the ALD data structure.

Figure 1 shows a bus access to 0xFE000004 as a result of setting the ALD_EN bit in the HRCW. Figure 2 shows bus accesses from the PowerPC CPU for boot instructions and from the CP RISC for ALD data structure elements.

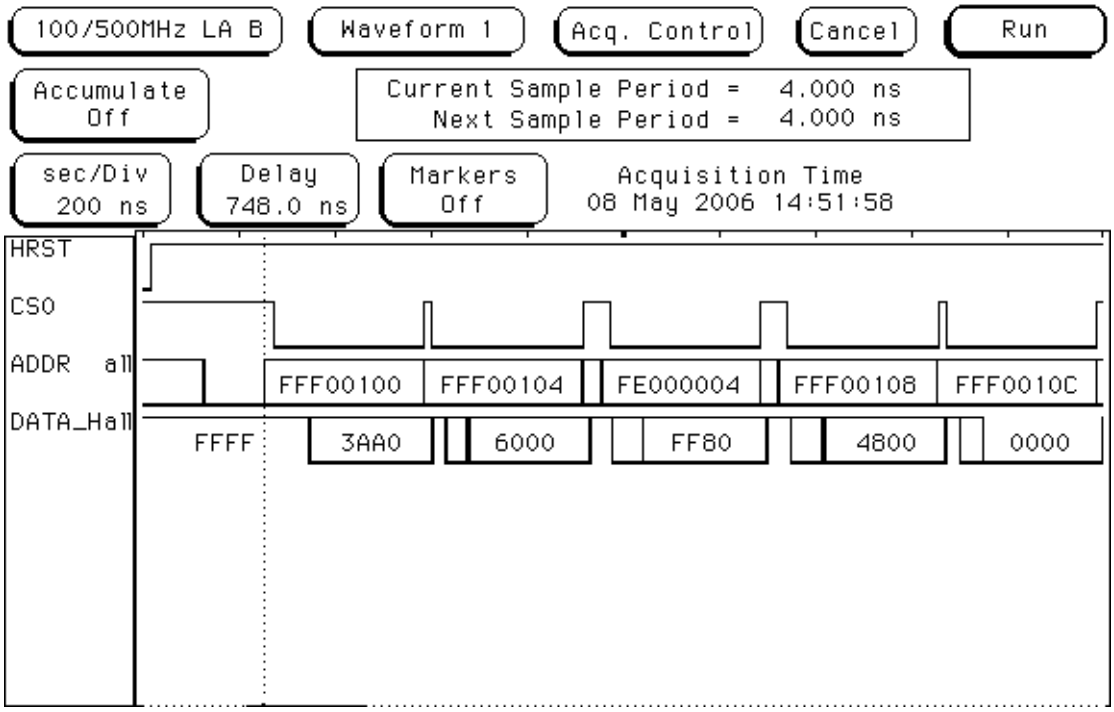

Figure 1. Fetch of ALD Pointer at 0xFE000004 (ALD Pointer = 0xFF801000)

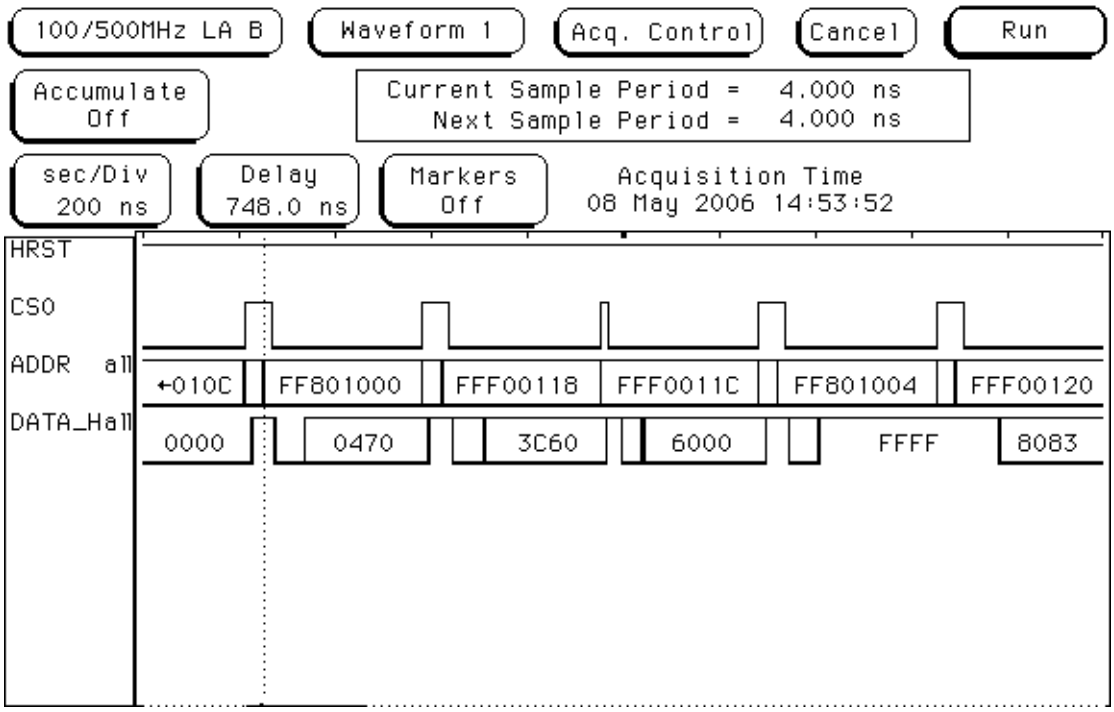

Figure 2. Fetch of First ALD Data Structure Element to Which the ALD Pointer is Pointing

1.2 ALD Data Structure

For details on the initialization of PCI configuration registers, refer to the section in the appropriate reference manual. The manual may refer to the device with the ALD structure as a EEPROM, but this does not imply a serial EEPROM. The device with the ALD structure is simply the existing boot device connected to $\overline{\text{CS0}}$, typically a flash memory or ROM device. On all PQ2 systems, the hardware reset configuration must be written into the boot flash memory/ROM before any attempt to boot the system. The ALD pointer and data structure must also be written beforehand, typically using the same mechanism (PROM burner or JTAG/ICE). In Figure 3, the pointer to the table resides at location 0x04 from the boot device's base address and is interleaved with the hardware configuration reset words. Because the sequence occurs after the reset configuration words are read, the memory controller for the boot device is operational and has configured the $\overline{\text{CS0}}$ controller to use a base address of either 0xFE000000 or 0x0000000 (depending on the value of the BMS bit). The pointer is an absolute value within the entire PQ2 physical memory space, so the upper bits in the address must match the base address of the device as defined by the BMS bit. The format of the data entries is always three words:

- Address of the internal space to be initialized
- Control word to indicate the data size and the end of the table
- Data to be initialized.

The address is the full 32-bit system address, and it is usually the IMMR base plus the offset of the register to be initialized. The higher-order bits in this address must be consistent with the address space defined by the ISB bits in the configuration word. For example, if the ISB = 111, all addresses within the structure should be 0xFFFxxxxx. Also, note that the data follows big endian rules. For data content less than 32 bits, use the most significant bits.

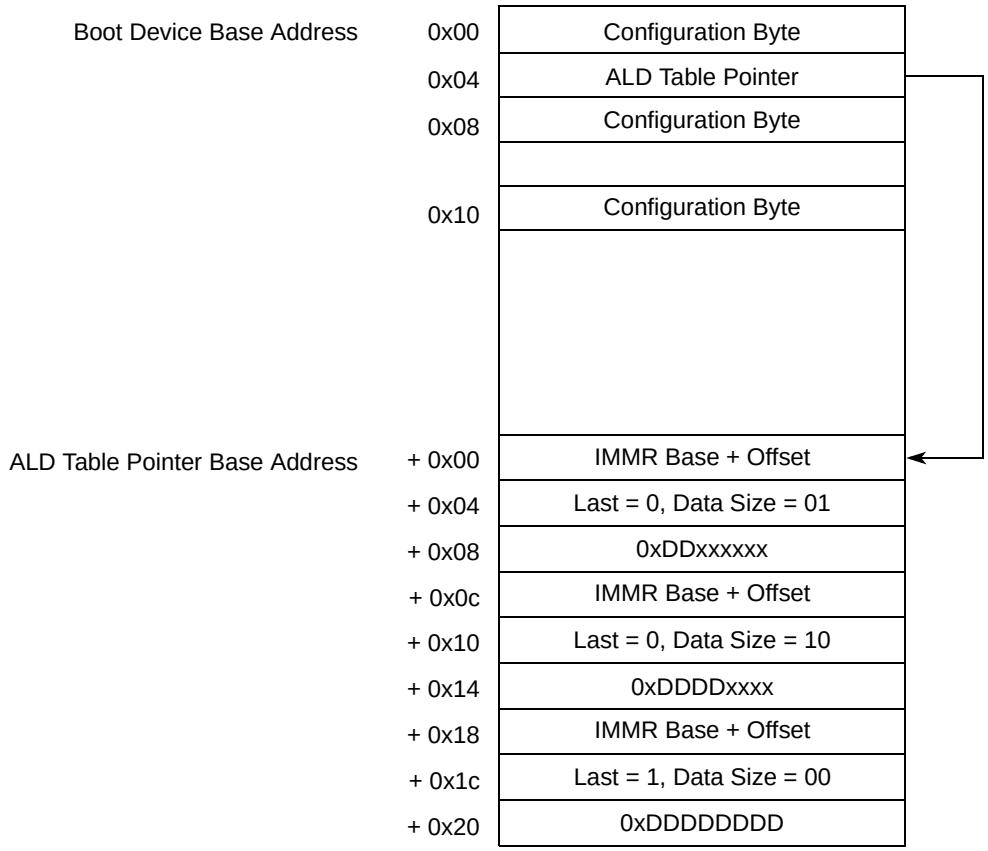

Figure 3. Boot Device Contents ALD Data Structure

2 Usage Recommendations

Use of the ALD to initialize the OR0/BR0 registers is not recommended because it can potentially change the addressing in the middle of the sequence. Also, it has been observed that the watchdog timer starts when the sequence begins. If the core is disabled, or if it stays quiescent for a while as other system tasks occur, the watchdog timer can expire. If this is likely in the system, use the ALD function to disable the watchdog timer.

3 Conclusion

The ALD function is intended to enable enough of the basic PCI configuration to be initialized so an external PCI master can handle most of the processor initialization and control. However, because of the way the mechanism is implemented, this feature can be used for any initialization of the processor. This feature can be used to off-load the internal processor initialization from a boot code task to a simpler data structure configuration of the boot device. To implement this feature successfully, you must be aware of precisely how much processor initialization has completed up to the point where the ALD sequence starts. Also, you must understand the effect this has on the specific contents of the ALD structure.

4 Testing and Validation

The details of the sequence described have been validated in simulation. Also, the ALD feature has been successfully implemented in a live system environment; the specifics listed were found to be critical for proper operation.

5 References

- *MPC8280 PowerQUICC™ II Family Reference Manual*, available at the Freescale web site.

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