Freescale Semiconductor
Application Note

Document Number: AN3271
Rev. 1, 05/2007

Migrating from MFR4200 to MFR4310

by: David Paterson
MCD Applications, East Kilbride, Scotland

1 Introduction

Freescale Semiconductor offers two key standalone FlexRay communication controllers — MFR4200 and MFR4310. These communication controllers are implemented with different FlexRay protocol specifications, version 1.1 and 2.1a respectively. Both devices are interoperable and can communicate with each other in a FlexRay network. This application note describes the differences between interoperability, compatibility, and gives an example of hardware and software configurations to help with migrating from the MFR4200 to MFR4310.

2 Objective

The aim of the document is to detail the differences between the MFR4200 and the MFR4310 and to provide hardware and software configuration examples to demonstrate interoperability and successful migration from MFR4200 to MFR4310. The information contained can help you quickly migrate from MFR4200 to a fully functional MFR4310 FlexRay node or complete network.

Contents

freescale semiconductor

3 Tasks to Build a FlexRay Cluster

This section lists some considerations required to build a FlexRay cluster.

Step 1: Application Data

The following information can be answered by the application:

- Number of nodes
- Minimum cycle time
- Information to transmit per node / communication matrix
- Special requirements, for example degree of reliability and safety

With this information, the following decisions can be made:

- Network topology (star versus bus)
- Cycle length
- Number of static slots

Step 2: Define Frame Size

Based on the communication matrix:

- Define which information should be transmitted in the static segment
- And which in the dynamic segment

Decide on static frame length, cycle time, and number of static frames:

- Find the optimum:
  - Longer cycle time → more static frames can be send
  - Longer frames → less overhead, higher bandwidth

Decide on dynamic frame length and its update rate:

- Define number of dynamic frames per node and cycle
- Try to distribute the frames equally over the cycles

Step 3: Configure FlexRay Node

Based on the decisions made before:

- Define FlexRay communication schedule

Define FlexRay configuration:

- Cycle time, required precision
- Macrotick length
- Atatic slot length, action point offset
- Minislot size, minislot action point offset
- Set NIT length

Decide on dynamic frame length and its update rate:

- Minislot size, minislot action point offset
- Dynamic frame length per node
- Dynamic slot idle phase
- pLatestTx

Define clock synchronization:

- Set synchronization nodes
- Set acceptance range
- Define Startup
- Set cold start nodes
- Configure startup timing

Define wakeup nodes:

- Set wakeup nodes
- Configure wakeup timing

Define error behavior:

- Enable/disable state transitions in case of error

4 MFR4200 Interoperability

MFR4200 is interoperable with any PS V2.0 compliant device.

All features necessary for practical use of FlexRay are implemented in MFR4200 and are compatible to PS V2.0. Workarounds are available for all unimplemented features.

The main differences of MFR4200 to a 100% V2.0 compliant device are primarily on the controller-host interaction which mainly affects the low level drivers. Slight differences of FlexRay mechanisms are noticed only when in-depth analysis is performed, transparent to application level. These differences do not harm interoperability between the devices.

Overall, the MFR4200 can be used in PS V2.0 clusters and MFR4310 can replace MFR4200 with integrated device compatible software drivers and minor layout changes.

5 MFR4200 Compatibility

5.1 Practical Impact of Differences

POC — Protocol overall control:

- MFR4200 does not have READY state
- MFR4200 cannot change automatically from PASSIVE to ACTIVE (automatic error recovery): application must go to ACTIVE via CONFIG

Single slot mode:

- Slightly improves robustness of startup
- Can be modelled with MFR4200 by assigning only one slot to one node

Coding:

- MFR4200 is optimized for 10 MBit/s
- < 10 MBit/s: can be configured, works well with good signal quality; problems with flat edges or bad signal quality on physical layer

Wakeup:

- MFR4200 can send a wakeup symbol, but does not detect media activity during wakeup mode
- No impact if there is only a single node waking up the system or if wakeup is well controlled in application so that it cannot occur during normal operation.

5.2 MFR4310 Feature Changes

Flexray bus lower bit rates support:

- In addition to 10 MBit/s bit rate, support of lower FlexRay channel bit rates was added: 8, 5, and 2.5 MBits/s

There are 128 message buffers available:

- Configured in two regions for any size between 2- and 254-byte payload
- Fast CHI clock input required to support full search of more than 64 buffers in the minimum minislot length (2 μs) i.e., full bandwidth utilization

Message buffer windowing mechanism removed:

- No message buffer windowing mechanism — additional address lines added to the asynchronous memory interface provide an 8-kbyte address space
- Multiple message buffers can be locked simultaneously
- All message buffers payload data can be viewed once the buffer has been locked
- The same memory map implemented on the integrated FlexRay module will be available on the MFR4310

Message buffer layout (byte Endianess):

- Errata in MFR4200 corrected — Data0 swapped from LSbyte to MSbyte etc.

Asynchronous memory interface performance:

- Single read and write access times significantly reduced — down to approximately 70 ns (at 40 MHz) from 150 ns+ — significantly reducing required wait states and improving system performance

Single-channel operation:

- Channel A can be configured to connect to channel A or channel B in single-channel mode of operation

Message buffers dynamically re-configurable:

- A mechanism is provided which allows for secure disabling of any buffer assigned to the static or dynamic part of the cycle
- While disabled, the buffer can be re-configured
- After re-enabling the buffer, it is considered for transmission or reception in the same cycle

5.3 Buffer Access Comparison

MFR4200 active buffer windowing:

- Buffer n lock request issued by host toggling LOCK bit
- Lock granted by CHI, signaled by setting LOCK bit
- Buffer header, status, and payload data appears in active window depending on whether it is transmit, receive, or FIFO buffer
- Buffer is unlocked immediately when host toggles LOCK bit

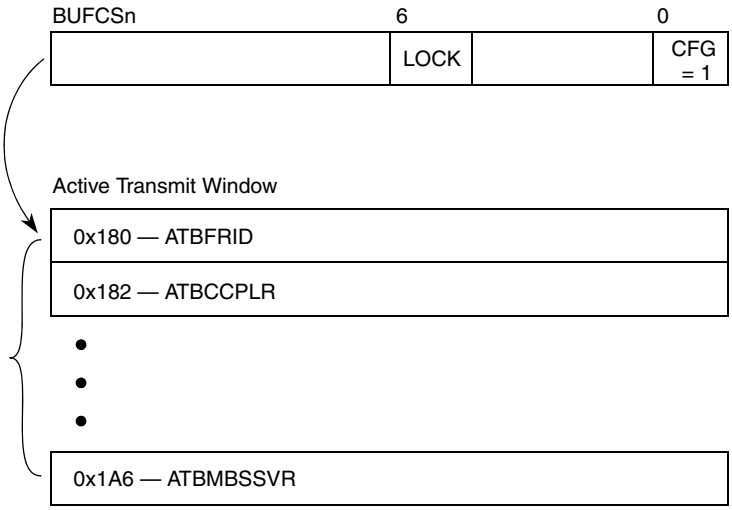

Figure 1. MFR4200 Active Buffer Windowing

PS2.1 device buffer access:

- Buffer n lock request issued by host toggling LCKT bit
- Lock granted by CHI, signaled by setting LCKs bit
- Message buffer index register points to message buffer header field (static)
- Data offset points to message data field (dynamic)
- Buffer is unlocked immediately when host toggles LCKT bit

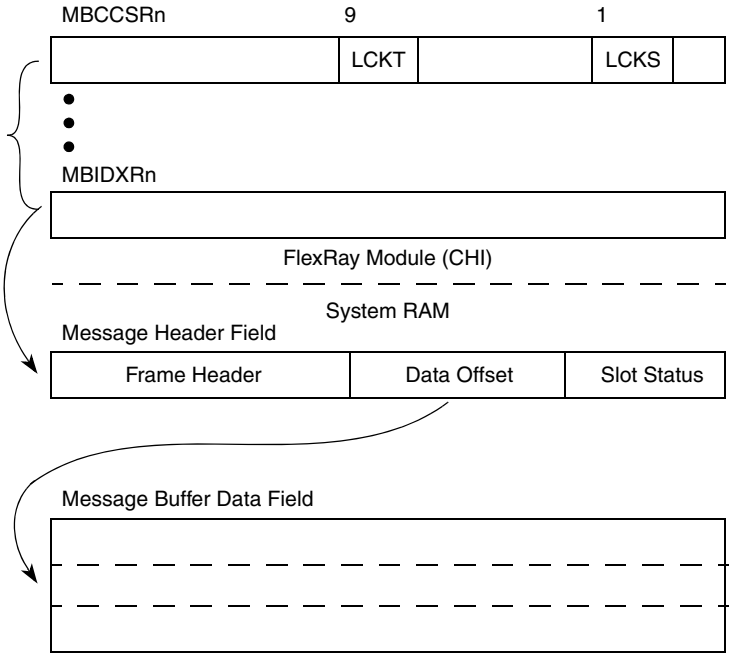

Figure 2. PS2.1 Device Buffer Access

5.4 Pinout Changes

MFR4310 pinout changes are given in this subsection.

Linear address Sspace (HCS12 interface chip select)

As the MFR4310 now has an 8-kbyte address space available, only eight chip select regions are possible in the 16-bit address space and only three ACSn pins are required:

- Pin 18: removed ACS0
- Pin 21: removed ACS1
- Pin 22: removed ACS2
- Pin 27: changed ACS3 to ACS0
- Pin 28: changed ACS4 to ACS1[1]
- Pin 34: changed ACS5 to ACS2[1]

1. Indicates other changes related to this pin

Linear sddress dpace (AMI interface)

Three extra address pins are required:

- Pin 28: added A11[1]
- Pin 34: added A12[1]
- Pin 52: added A10

Two pins were also added to allow 8-bit data access to certain MCUs. Please see the interface application notes relevant to each MCU core. The byte select inputs required are:

- Pin 47: added BSEL#0
- Pin 48: added BSEL#1

128 message buffer support (CHI clock)

With the CHI running with 40-MHz internal clock, 64 message buffers can be searched (for next transmission) in the shortest possible minislot time

- To fully support the available 128 message buffers, a fast CHI clock is required
- Selection of this clock input is done using an IF_SEL option. See the MFR4310 reference manual for details.
- Clock input pin required
  - Pin 32: added CHICLK_CC[1]

PS1.1 bus guardian IF removal (bus guardian interface)

- Pin 32: remove BGT[1]
- Pin 42: remove BGEM1[1]
- Pin 46: remove BGEM2[1]
- Pin 47: remove ARM[1]
- Pin 48: remove MT[1]

Multiplexing balance (configuration/debug functions)

Issues have been seen with pullup/ pulldown component selection when configuration pins have mixed connections to for example, the physical layer.

Debug interface enhanced:

- Move CLK_S[0] to pin 42[1]
- Move IF_SEL[0] to pin 45
- Move CLK_S[1] to pin 46[1]
- Move DBG[2] to pin 42[1]
- Pin 46: add DBG[3][1]
- Pin 48: add DBG[0][1]

1. Indicates other changes related to this pin

In summary, a total of 13 pin functions have been changed:

- 4 relate to HCS12 interface only
- 9 affect AMI and multiplexing

However, the package is compatible:

- No changes made to power supply layout
- No changes made to oscillator layout
- Layout recommendations for the MFR4310 are unchanged from the MFR4200

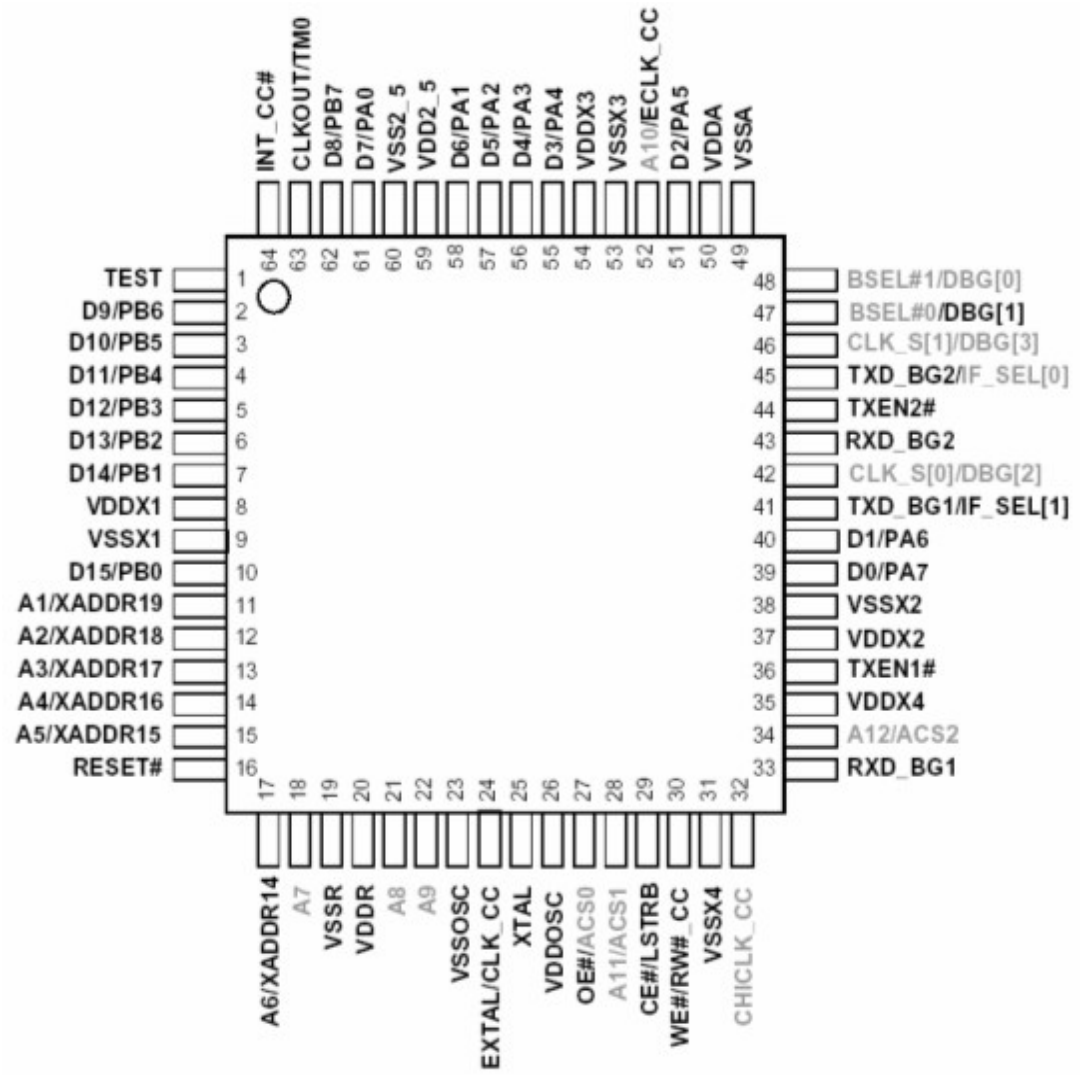

Figure 3. Pinout Differences

5.5 MFR4200/4310 AMI Layout Considerations

The AMI pins shown in Table 1 need layout consideration to allow direct replacement of MFR4200 with MFR4310.

Table 1. Layout Considerations

Pin	Function		Comments
	MFR4200	MFR4310	
52	ECLK	ECLK/A10	ECLK not used for AMI
48[1]	MT/CLK_S1	BSEL1/DBG0	No BG; pullup/down for configuration
47[1]	ARM/DBG/CLK_S0	BSEL0/DBG1	No BG; pullup/down for configuration
46	BGE2	CLK_S1/DBG3	No BG; add pullup/down
45	TXD_BG2	TXD_BG2/IF_SEL0	Add pullup/down, as pin 41
42	BGE1	CLK_S0/DBG2	No BG; add pullup/down
34	ACS5	A12/ACS2	ACS pins not used for AMI
32[2]	BGT/DBG2/IF_SEL0	CHICLK_CC	CHICLK_CC must be disconnected from MFR4200
28	ACS4	A11/ACS1	ACS pins not used for AMI

1 Pins 47 and 48 must be disconnected if 8-bit access is used.

2 Pin 32 must be disconnected if fast CHI clock is used.

5.6 Bus Timing Comparison

Please refer to the MFR4200 and the MFR4310 data sheets for the latest timing diagrams and parameters.

- AMI Interface Timing Diagram
- HCS12 Interface Timing Diagram

6 Hardware Example

6.1 MFR4200/MFR4310 HCS12 Interface

Figure 4 shows the typical connections required for the HCS12 interface to the MFR4200 and the MFR4310. Figure 4 only concerns the key address, data, and control signals. In this example, the ACS signals between the MFR4200 and MFR4310 are connected to port H as general-purpose ports.

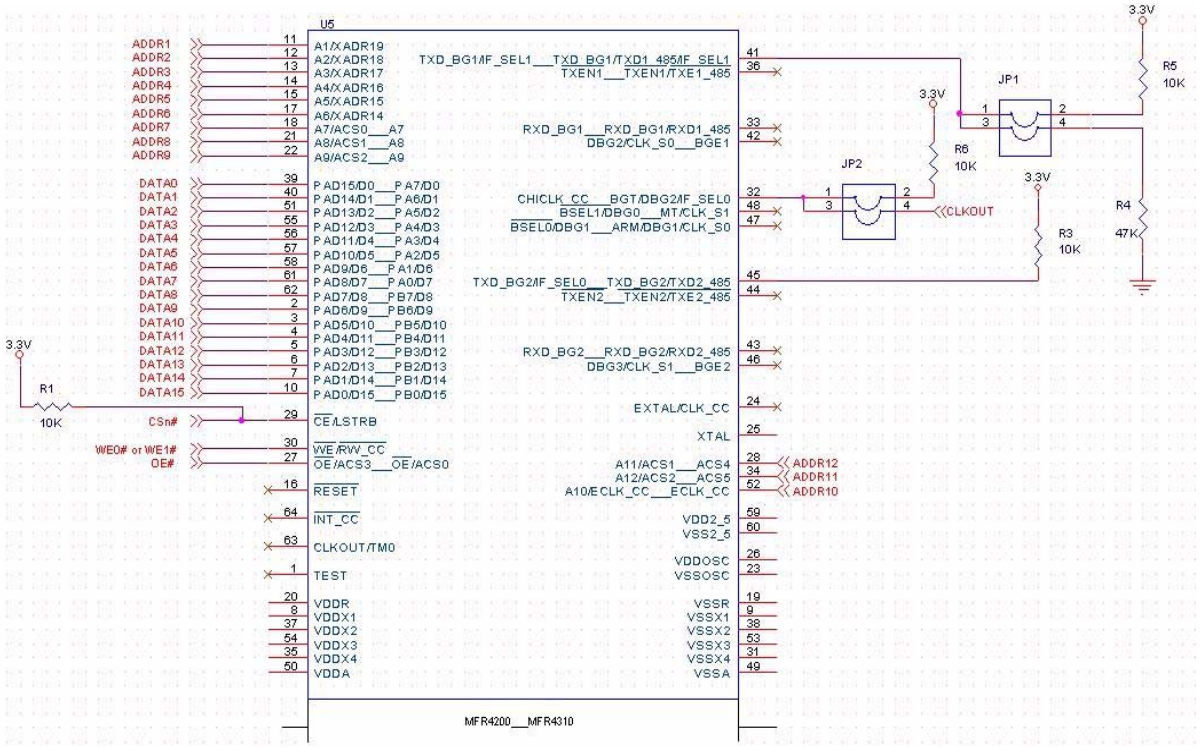

Figure 4. MFR4200/MFR4310 HCS12 Interface Connections

6.2 MFR4200/MFR4310 AMI Interface

Figure 5 shows the typical connections required for the MPC55xx interface to the MFR4200 and the MFR4310. Figure 5 only concerns the key address, data, and control signals.

There must be flexibility with the IF_SEL0 and IF_SEL1 pins for both the MFR4200 and the MFR4310.

It is important that the CHICLK_CC signal of the MFR4310 is disconnected from the MFR4200.

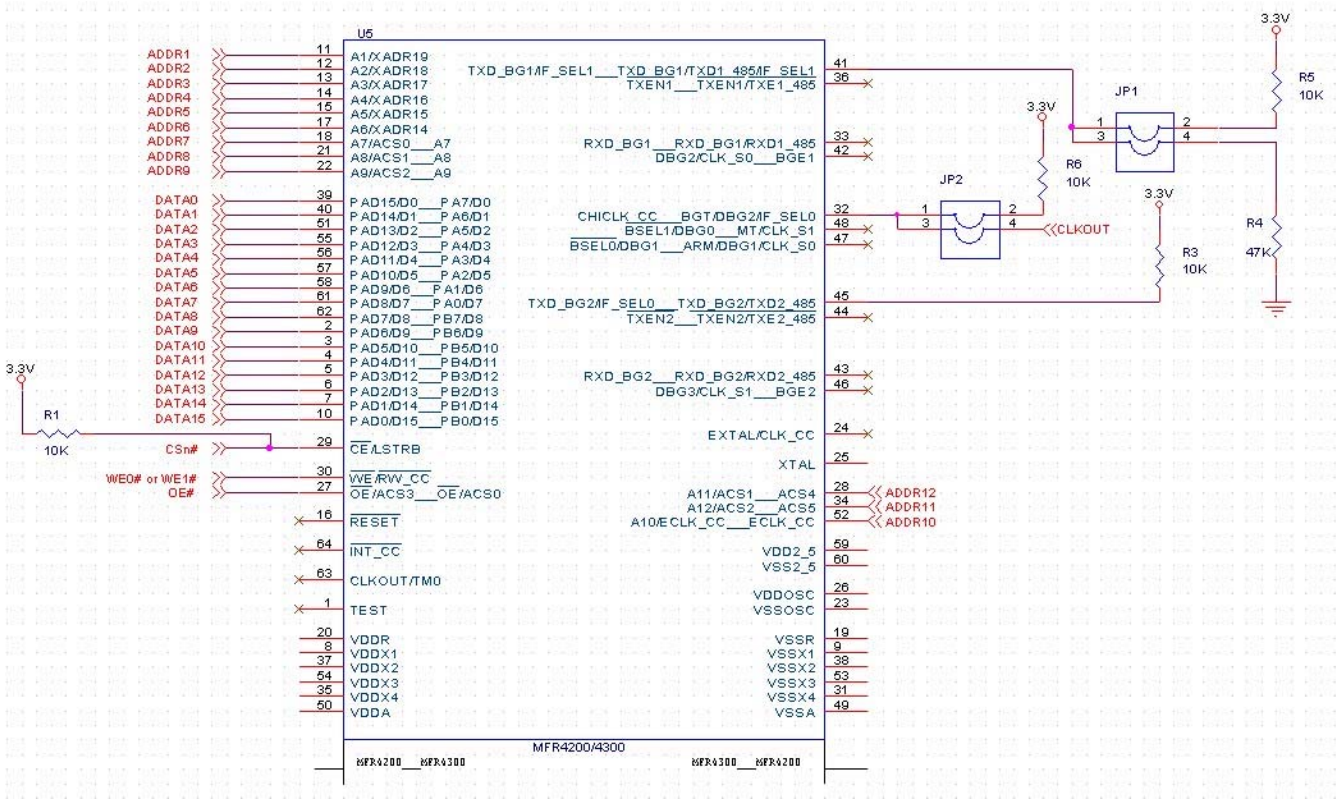

Figure 5. MFR4200/MFR4310 AMI Interface Connections

7 Software Configuration Examples

Please refer to the application note entitled *Incorporating an MFR4310 Node in an MFR4200 Network* (AN3265) for both MFR4200 and MFR4310 software examples.

8 Conclusions

The MFR4310 can replace the MFR4200 with integrated device compatible software drivers and minor layout changes. The application note is based on hardware examples and a application example to show the simplicity of incorporating an MFR4200 node into an MFR4310 network.

9 References

1. *MFR4200 FlexRay Communication Controller Data Sheet* (MFR4200)
2. *MFR4310 FlexRay Communication Controller Reference Manual* (MFR4310RM)
3. *FlexRay Communications System Protocol Specification Version 1.1*
4. *FlexRay Communications System Protocol Specification Version 2.1a*

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com and http://www.flexray.com.

More information on Freescale's FlexRay products can be found at http://www.freescale.com/flexray.

THIS PAGE IS INTENTIONALLY BLANK

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN3271
Rev. 1
05/2007

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics as their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see http://www.freescale.com or contact your Freescale sales representative.

For information on Freescale’s Environmental Products program, go to http://www.freescale.com/epp.

freescale™
semiconductor