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Application Note

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Interfacing MPC5500 Microcontrollers to the MFR4310 FlexRay Controller

by: Robert Moran
MCD Applications, East Kilbride, Scotland

1 Introduction

Freescale Semiconductor offers a range of standalone FlexRay communication controllers (MFR4xxx) that can be interfaced with 16-bit and 32-bit microcontrollers (MCU). This application note describes the hardware, software and timing considerations necessary for reliable communication between the MFR4310 controller and the MPC55xx family of MCUs.

2 Objective

This document demonstrates the simplicity of the hardware interface between the MFR4310 and the MPC55xx, and discusses hardware and software considerations when configuring the MPC55xx for operation with the MFR4310. The information contained can help you quickly design a FlexRay node using the MPC55xx family of MCUs. Evaluation boards with software are available from Freescale, to assist in the development of FlexRay applications. (See http://www.freescale.com/flexray.)

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Note: In this document, active-low signals are indicated by a “#” at the end of the signal name, e.g. “IRQn#”.

3 Hardware Design Requirements

The MPC55xx family interfaces with the MFR4310 via the external bus interface (EBI). On the MPC55xx the EBI provides individual address, data and control signals. The MFR4310 must be connected to the MPC55xx using the MFR4310 MPC mode. The devices can be connected together without additional glue logic, which simplifies the design and reduces the system cost.

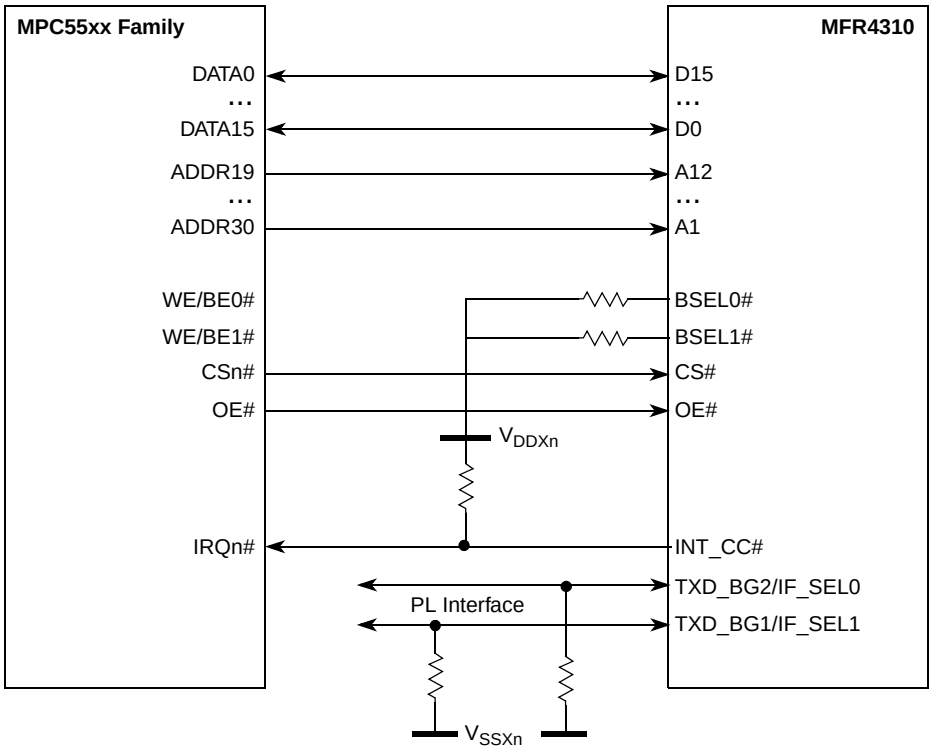

Figure 1. Connecting MFR4310 to MPC55xx MCUs

3.1 Selecting the MPC Mode

The interface mode required for operating the Controller Host Interface (CHI) is the MPC interface.

There is one “CHI and Host Interface Clock” for MPC mode — CHICLK_CC. This is the selectable external CHI clock input.

Note the following implementation constraints:

- The minimum external clock frequency for CHICLK_CC (when selected) is 20 MHz.
- The maximum external clock frequency for CHICLK_CC is 76 MHz

Table 1. MFR4310 Interface Select

Pin		Interface	CHI and Host Interface Clock	CRSR.ECS
IF_SEL0	IF_SEL1			
0	0	MPC Interface	CHICLK_CC	1
0	1	HCS12 synchronous interface	CLK_CC	0
1	0	Asynchronous memory interface[1]	CLK_CC	0
1	1	Asynchronous memory interface	CHICLK_CC	1

1 This is the default interface (i.e. if no external pull resistors are connected to IF_SEL0 and IF_SEL1, the internal pullup on IF_SEL0 and the internal pulldown on IF_SEL1take effect).

To select the MPC Interface, IF_SEL0 and IF_SEL1 should both be pulled low.

3.2 Bus Signals

3.2.1 Data and Address Pins

On the MFR4310, D0 is the least significant bit (LSB) of the data bus, and A1 is the LSB of the address bus; however, on the MPC55xx, ADDR0 is the most significant bit of the address. Therefore, the data and address pins must be connected in reverse order to the MFR4310, i.e., with D0 on the MFR4310 connected to DATA15 on the MPC55xx, and A1 on the MFR4310 connected to ADDR30 on the MPC55xx.

3.2.2 Control Signals

The MFR4310 has a 16-bit data bus, however 8-bit data access is possible via BSEL0# and BSEL1# signals.

NOTE

Chip selects CS[0:3]# on the MPC55xx can be used to interface to the MFR4310. However, note that CS0# is the global chip select for boot memory.

3.2.3 Voltage Levels

The MFR4310 must be configured for 3.3 V I/O (by powering V_{DDR} with 3.3 V) to allow correct interfacing to the MPC55xx, whose EBI pins must also be powered from 3.3 V. Refer to the electrical specifications provided in the MPC55xx reference manual (Reference 1) and MFR4310 data sheet (Reference 2).

4 Software

The software setup described in this section is concerned mainly with initializing the MPC55xx to allow the MFR4310 controller host interface to function properly. This involves configuring the EBI pads and memory controller to locate the MFR4310 into the MPC55xx memory map.

When both devices have been initialized, the MPC55xx can read and write the MFR4310 registers.

4.1 Pad Configuration for EBI Operation

Each pin on the MPC55xx must be initialized individually to select the pin function, direction, and static electrical attributes. This is controlled by the appropriate MPC55xx system integration unit_pad configuration registers (SIU_PCRs).

NOTE

The number of the PCR required to configure the pad relates to the GPIO number for the pad, for example CS0 (GPIO0) uses PCR0. Refer to the signal description and system integration unit chapters of the appropriate MPC55xx reference manual (Reference 1) for more detailed information.

The MPC55xx memory controller must be initialized for the EBI to use the correct chip select, and the correct number of wait states (which depends on the internal bus frequency). See Section 4.3, “Wait State Requirements” for specific details. Figure 2 shows the steps needed to allow communication between the devices.

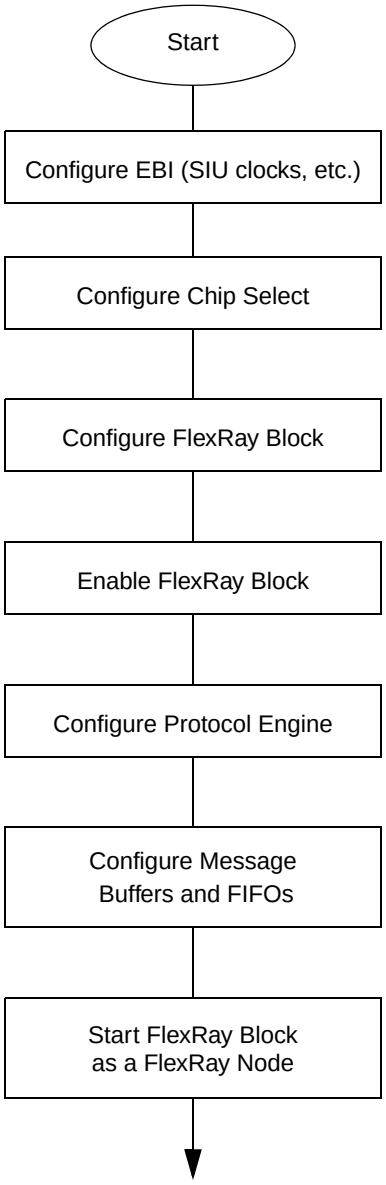

Figure 2. Configuration Flow

4.2 Chip Select Configuration

As shown Figure 2, the second step in the initialization sequence is to configure the chip select on the MPC55xx. The memory controller controls the chip select generation for the MPC55xx. There are four chip selects on the MPC55xx, any one of which can be chosen as the chip select to the MFR4310.

NOTE

CS0# is the global chip select, which is used primarily for booting from external FLASH memory. If it is used for this primary purpose, it cannot be used for MFR4310 communication, and a different chip select must be used.

The option registers (EBI_OR[0:3]) and base registers (EBI_BR[0:3]) are used to configure the chip select. Refer to the memory controller section of the MPC55xx reference manual (Reference 1) for more information on chip select configuration.

4.3 Wait State Requirements

A number of wait states are required for successful read/write accesses between the MPC55xx and the MFR4310. Table 2 details the number of wait states required for successful operation when running with the external CHI clock.

This number should be set in the memory controller option register, bits SCY.

Table 2. Minimum Wait States Required — CHICLK_CC as the Interface Clock

MPC5500 System Frequency (MHz)	MPC5500 EBI Frequency (MHz)	CHICLK_CC (MHz)	Minimum Wait States in SCY
132	66	66	3
128	64	64	3
112	56	56	2
84	42	42	2
80	40	40	2
66	33	33	2
40	20	20	2

4.4 MPC55xx Chip Select and FMPLL Settings

From Table 2 the wait states that are required for successful read/write cycles, with or without the external CHI clock between the MPC55xx and MFR4310 are shown.

For the minimum wait state configuration using the CHI clock it has been shown that a minimum of 3 wait states are required. This can be set in the option register OR[SCY] field of the EBI.

For example, if CS1# is being used for communication with the MFR4310, the following register settings could be used.

Chip Select

```
EBI.CS[1].BR.R  = 0x20080803     ;Base address = 0x20080000, 16 bit port size,
                                 ;burst inhibit, valid chip select
EBI.CS[1].OR.R  = 0xFFF80030     ;Address Mask = 13 bit, 3 wait states
```

FMPLL

```
FMPLL.SYNCR.R   = 0x1E900000     ;MFD = 29, RFD = 2, PREDIV = 1, PLL will ;loose
                                 ;lock
while (FMPLL.SYNSR.B.LOCK != 1)  ;Wait for PLL to lock before continuing.
FMPLL.SYNCR.R   = 0x1E800000     ;MFD = 29, RFD = 0, PREDIV = 1. The system
                                 ;frequency is now 132 MHz, the EBI frequency
```

```
;is 66 MHz.
```

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	0	0	1	BA												
W																
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg. Addr. Base + 0x0010 (EBI_BR0); Base + 0x0018 (EBI_BR1); Base + 0x0020 (EBI_BR2); Base + 0x0028 (EBI_BR3); Base + 0x0040 (EBI_CAL_BR0); Base + 0x0048 (EBI_CAL_BR1); Base + 0x0050 (EBI_CAL_BR2); Base + 0x0058 (EBI_CAL_BR3)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	BA	0	0	0	PS	0	0	0	0	BL	WEBS	TBDIP	0	0	BI	V
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Reg. Addr. Base + 0x0010 (EBI_BR0); Base + 0x0018 (EBI_BR1); Base + 0x0020 (EBI_BR2); Base + 0x0028 (EBI_BR3); Base + 0x0040 (EBI_CAL_BR0); Base + 0x0048 (EBI_CAL_BR1); Base + 0x0050 (EBI_CAL_BR2); Base + 0x0058 (EBI_CAL_BR3)

= Unimplemented or Reserved

Figure 3. EBI Base Registers (BR[0:3])

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
R	1	1	1	AM												
W																
Reset	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg. Addr. Base + 0x0014 (EBI_OR0); Base + 0x001C (EBI_OR1); Base + 0x0024 (EBI_OR2); Base + 0x002C (EBI_OR3); Base + 0x0044 (EBI_CAL_OR0); Base + 0x004C (EBI_CAL_OR1); Base + 0x0054 (EBI_CAL_OR2); Base + 0x005C (EBI_CAL_OR3)

	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
R	AM	0	0	0	0	0	0	0	SCY				0	BSCY		0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Reg. Addr. Base + 0x0014 (EBI_OR0); Base + 0x001C (EBI_OR1); Base + 0x0024 (EBI_OR2); Base + 0x002C (EBI_OR3); Base + 0x0044 (EBI_CAL_OR0); Base + 0x004C (EBI_CAL_OR1); Base + 0x0054 (EBI_CAL_OR2); Base + 0x005C (EBI_CAL_OR3)

= Unimplemented or Reserved

Figure 4. EBI Option Registers (OR[0:3])

4.5 Interface Considerations

BSEL0# and BSEL1# must be pulled up to 3.3V, as shown in Figure 1. This will restrict accesses to 16-bits wide.

4.6 Module Version Register (MVR)

The MFR4310 module version register (MVR) contains a value specific to the mask set as defined in Table 3 (0x8566 in the case of the 1M63J mask set).

Table 3. MFR4310 Part ID and Module Version Numbers

Device	Mask Set Number	Part ID		
		PIDR	AVNR	MVR
MFR4310	1M63J	4310	0000	8566

When the power-on reset signal is asserted the Clocks and Reset Generator (CRG) asserts the system reset signal. The CRG will deassert synchronously the system reset signal approximately 16420 EXTAL/CLK_CC clock periods after the deassertion of the power-on reset signal. See ‘Clocks and Reset Generator (CRG)’ chapter in the MFR4310 Reference Manual (Reference 2).

5 Conclusions

The FlexRay controller can be connected to the MPC55xx family of MCUs, without any glue logic being required, as the EBI on the MPC55xx interfaces directly with the MPC interface on the MFR4310. Software configuration is also straightforward and the MFR4310 is simply memory mapped into the global address space.

6 References

1. MPC5553/MPC5554 Reference Manual (MPC5553/4RM)
2. MFR4310 FlexRay Communication Controller Reference Manual (MFR4310RM)

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com

More information on FlexRay and FlexRay products can be found at http://www.freescale.com/flexray

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+44 1296 380 456 (English)
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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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