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Application Note

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Interfacing HCS12 Microcontrollers to the MFR4200 FlexRay Controller

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1 Introduction

Freescale Semiconductor offers a range of standalone FlexRay communication controllers (MFR4xxx) that can be interfaced with 16-bit and 32-bit microcontrollers (MCU). This application note describes the hardware, software, and timing considerations necessary for reliable communication between the MFR4200 controller and the HCS12 family of MCUs.

2 Objective

The aim of the document is to demonstrate the simplicity of the hardware interface between the MFR4200 and the HCS12, and to provide an example of the software used to configure the HCS12 for operation. The information contained can help you quickly design a fully functional FlexRay node based on the HCS12 family of MCUs. Evaluation boards with software are available from Freescale to assist in the development of FlexRay applications. (See http://www.freescale.com/flexray.)

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Note: In this document, active-low signals are indicated by a “#” at the end of the signal name, e.g. “IRQn#”.

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3 Hardware Design

The MFR4200 FlexRay controller has two separate controller host interfaces (CHI) on board — an HCS12 interface, for direct connection to Freescale's HCS12 family of microcontrollers, and an asynchronous memory interface (AMI) for asynchronous connection to all other microcontrollers. The HCS12 interface clock signal, used to synchronize the data transfer, can run at a maximum rate of 8 MHz.

Chip selection for the HCS12 interface is generated internally using the following signals:

- The expanded address signals XADDR[14:19] input values (HCS12 is in the Paged or Unpaged mode of its External Bus Interface (EBI)) are compared with the logical 0's.
- The six most significant bits of the demultiplexed address bus, PAD[10:15], are compared with the pattern set up externally on the address chip select pins, ACS[0:5]. PAD10 is compared with ACS0, PAD11 with ACS1, …PAD15 with ACS5.

NOTE

The address decoding phase of a read/write operation is passed if all the comparisons described above are passed.

The devices can be connected together without additional glue logic, thereby simplifying the design and reducing the system cost.

3.1 Selecting the HCS12 Mode

There are two modes of operation for the controller host interface (CHI), the AMI mode and the HCS12 mode. The HCS12 mode is used to interface to the HCS12 Family of microcontrollers.

To select the HCS12 mode, IF_SEL1 must be at the logic high level and IF_SEL0 must be at the logic low level. When using 3.3 V V_{DDIO}, for example, IF_SEL1 must be pulled high using a 16 kΩ pullup resistor, and IF_SEL0 must be pulled low using a 47 kΩ pulldown resistor. (Similarly, at 3.3 V V_{DDIO}, INT_CC# must be held high by a 16 kΩ pullup resistor.)

3.2 Paged Mode and Unpaged Mode

There are two modes of operation that can be used when interfacing the HCS12 and MFR4200 microcontrollers — paged and unpaged mode.

Figure 1 and Figure 2 show block diagrams with all the EBI connections that are necessary for each mode of operation.

Table 1 provides a description of each signal and pin that must be connected to interface the MFR4200 to a typical HCS12 MCU, the MC9S12DP256B in a 112-pin LQFP package.

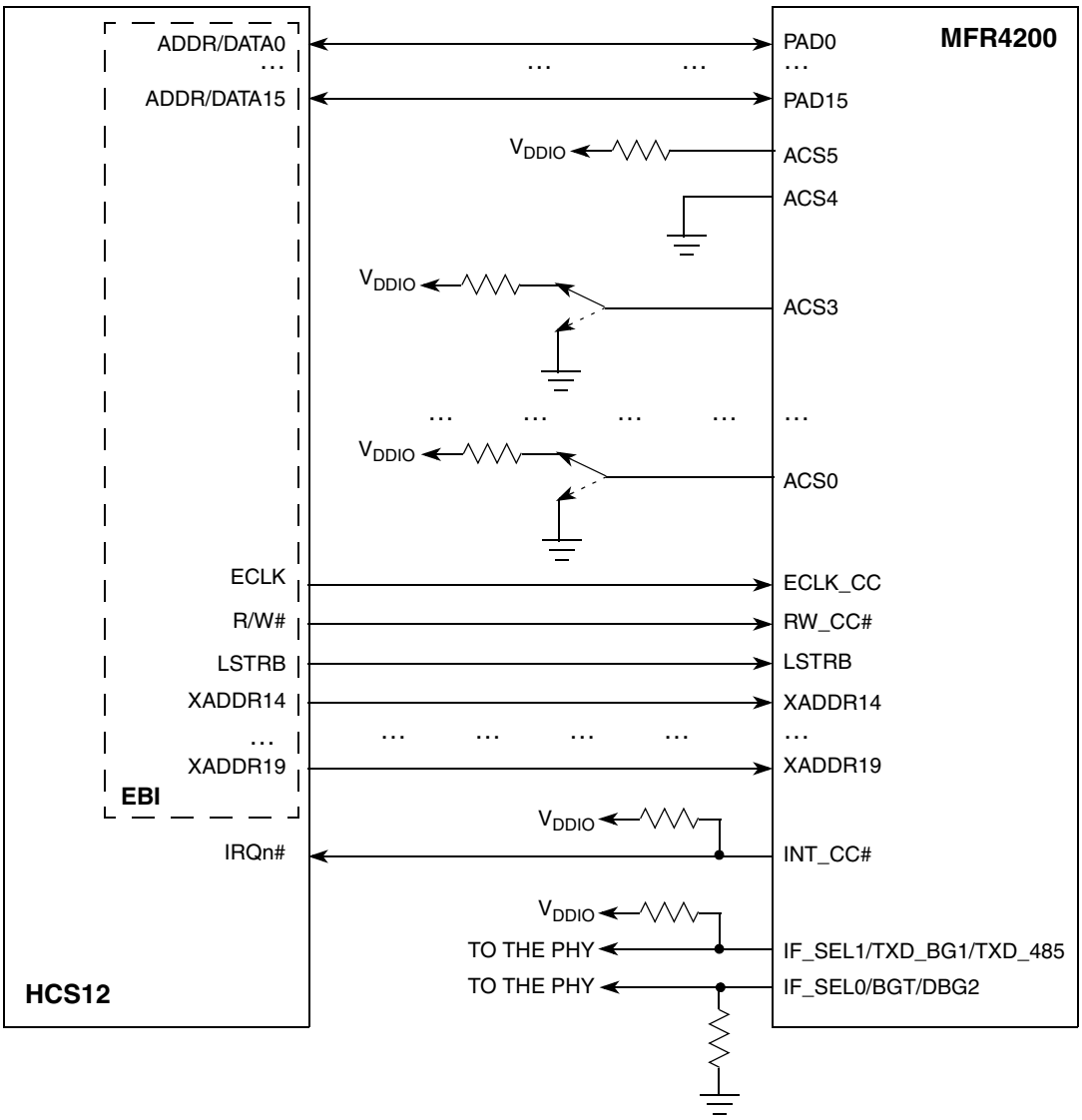

Figure 1. Connecting MFR4200 to HCS12 with Page Mode Support

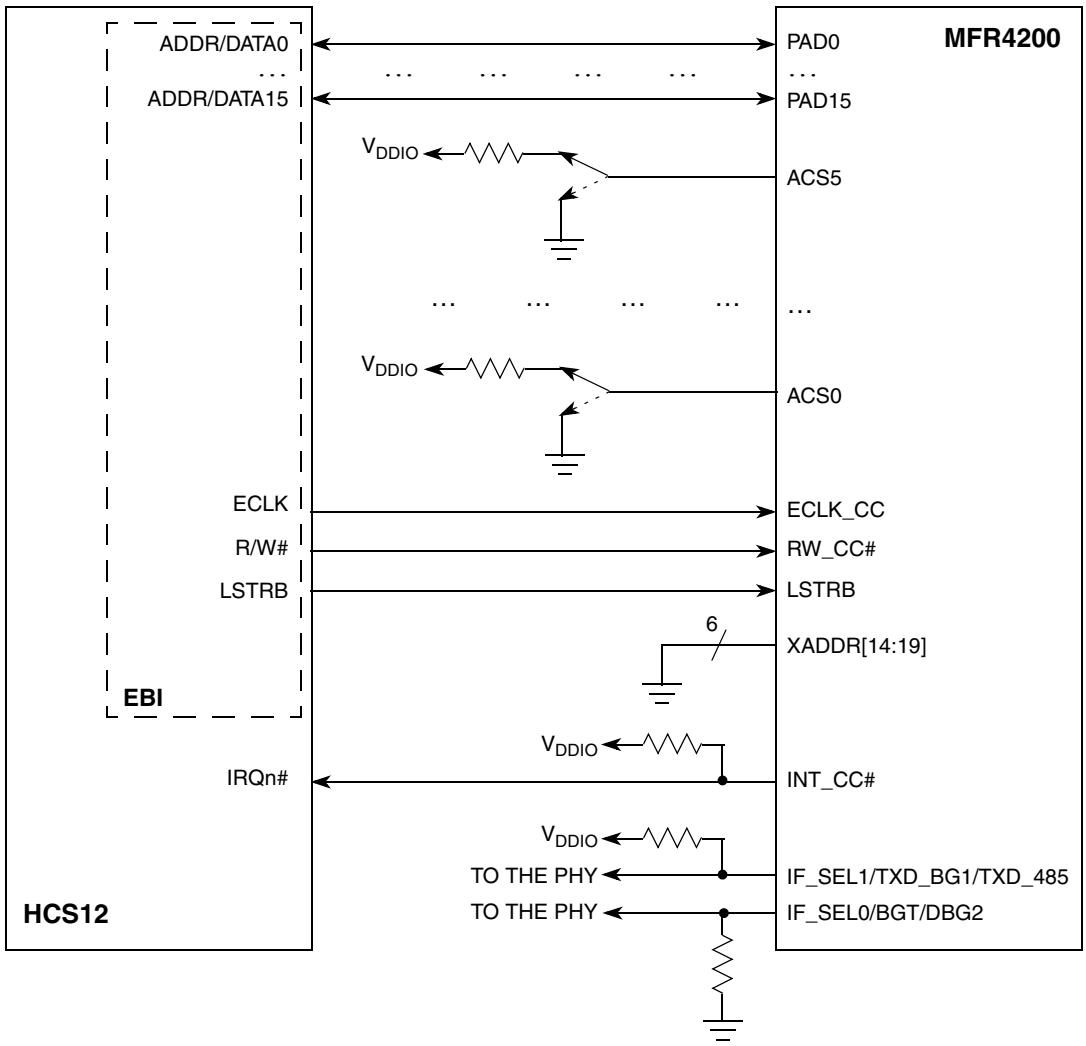

Figure 2. Connecting MFR4200 to HCS12 with Unpaged Mode Support

Table 1. Interface Signal Description

HCS12 to MFR4200 Connection				
MC9S12DP256B (112-Pin LQFP)		**MFR200**		**Comments**
Signal	**Pin**	**Signal**	**Pin**	
ADDR0/DATA0/PB0	24	D15/PAD0	10	HCS12 data/address bus (LSB)
ADDR1/DATA1/PB1	25	D14/PAD1	7	HCS12 data/address bus
ADDR2/DATA2/PB2	26	D13/PAD2	6	HCS12 data/address bus
ADDR3/DATA3/PB3	27	D12/PAD3	5	HCS12 data/address bus
ADDR4/DATA4/PB4	28	D11/PAD4	4	HCS12 data/address bus
ADDR5/DATA5/PB5	29	D10/PAD5	3	HCS12 data/address bus
ADDR6/DATA6/PB6	30	D9/PAD6	2	HCS12 data/address bus
ADDR7/DATA7/PB7	31	D8/PAD7	62	HCS12 data/address bus
PA0/ADDR8/DATA8	57	D7/PAD8	61	HCS12 data/address bus
PA1/ADDR9/DATA9	58	D6/PAD9	58	HCS12 data/address bus
PA2/ADDR10/DATA10	59	D5/PAD10	57	HCS12 data/address bus
PA3/ADDR11/DATA11	60	D4/PAD11	56	HCS12 data/address bus
PA4/ADDR12/DATA12	61	D3/PAD12	55	HCS12 data/address bus
PA5/ADDR13/DATA13	62	D2/PAD13	51	HCS12 data/address bus
PA6/ADDR14/DATA14	63	D1/PAD14	40	HCS12 data/address bus
PA7/ADDR15/DATA15	64	D0/PAD15	39	HCS12 data/address bus
XADDR14/PK0	8	A6/XADDR14	17	Extended addresses (page mode)
XADDR15/PK1	7	A5/XADDR15	15	Extended addresses (page mode)
XADDR16/PK2	6	A4/XADDR16	14	Extended addresses (page mode)
XADDR17/PK3	5	A3/XADDR17	13	Extended addresses (page mode)
XADDR18/PK4	20	A2/XADDR18	12	Extended addresses (page mode)
XADDR19/PK5	19	A1/XADDR19	11	Extended addresses (page mode)
ECLK/PE4	39	ECLK_CC	52	HCS12 clock input
R/W#/PE2	54	WE#/RW_CC#	30	HCS12 read/write select signal
LSTRB/TAGL0/PE3	53	CE#/LSTRB	29	HCS12 low-byte strobe signal
GPIO (or PU/PD)		ACS0–ACS5	18, 21, 22, 27, 28, 34	HCS12 address select inputs
GPIO		RESET#	16	Hardware reset input
PE1/IRQ#	55	INT_CC#	64	Controller interrupt output
		BGT/DBG2/IF_SEL0	32	Host interface selection = LOW (HCS12 mode)
		TXD_BG1/TXD1_485/IF_SEL1	41	Host interface selection = HIGH (HCS12 mode)

4 Timing Considerations

For the HCS12 and the MFR4200 communication controller to communicate reliably, the timing between the HCS12 and the MFR4200 must be matched. There is a requirement for the addition of stretch cycles[1] to match the timing characteristics. Refer to Section 8, "MFR4200 HCS12 Timing Specifications" for specific timing diagrams. A minimum of one stretch cycle must be inserted when running with an 8 MHz external clock. Table 3 summarizes the read and write timing for one stretch cycle, which is required for successful operation. The number of stretch cycles that can be added is controlled in the Miscellaneous System Control Register (MISC). Refer to the Module Mapping Control (MMC) section of the user manual. The available options are shown in Table 2.

Table 2. Stretch Cycle Selection

External Access Stretch Bit Definition	
EXSTR[1:0]	**Number of E Clocks Stretched**
00	0 cycles
01	1 cycle
10	2 cycles
11	3 cycles

Table 3. HCS12 to MFR4200 Timing Parameters with One Stretch Cycle

Num	Rating	Specified		1 Wait	
		Min	Max	Measured	Comment
1	Pulse width, ECLK low	25	—	685	PASS
2	Pulse width, ECLK high	114	—	190	PASS
3, 11	Address valid time to E rise	11	—	54	PASS
4	Write data delay time	—	7	4	PASS
5	ECLK rise to write data invalid	71	—	184	PASS
6 (4)	Write data hold time	2	—	2	PASS
7	RW delay time	—	7	0	PASS
8	RW valid time to ECLK rise	14	—	56	PASS
9	RW hold time	2	—	2	PASS
10	Data hold to address	2	—	54	PASS
12	Multiplexed address hold time	2	—	64	PASS
13	ECLK high access time (ECLK high to read data valid)	50	75	70	PASS
14	Read data setup time	13	—	120	PASS
15	Read data hold time	0	—	97	PASS

1. When accessing on-chip peripherals and memories, the HCS12 performs 8-bit and 16-bit core accesses in a single cycle. However, when the core accesses locations on the external bus using the expanded modes, the accesses are stretched and take more than a single cycle to complete. The minimum amount of stretching is one additional bus cycle, but can be increased. See Table 2 for details.

5 Software

The software setup is concerned mainly with selection of the correct MCU operating mode, configuration of the HCS12 for communication with the MFR4200, and linking into the correct area of the memory map.

5.1 Mode Configuration and EBI Operation

As already stated, the HCS12 must be configured into normal expanded mode to enable the bus interface. In this mode, ports A and B are configured for the data/address bus, and port E is configured for the control signals. During initialization, the EBI is configured, and the mode is set to normal expanded wide (BDM allowed) mode by writing MODC = 1, MODB = 1, and MODA = 1 in the MODE register. The EBI must be initialized to use the correct chip select and to select the correct number of stretch cycles. See Section 4, "Timing Considerations" for specific details.

Figure 3 shows the steps required to configure the HCS12 MCU for communication with the MFR4200 controller.

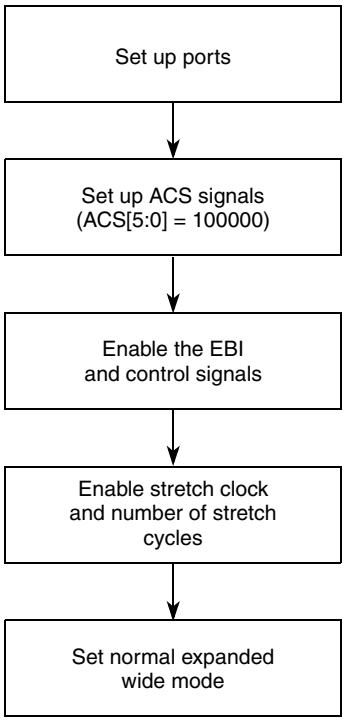

Figure 3. Initialization Flow Diagram

5.2 Placement of MFR4200 in Memory Map

The global address, associated with each chip select signal, is generated by a concatenation of the HCS12 local address [15:0] with the global page index register, where the page index bits are effectively used to select which of the 128 x 64 Kbyte pages is to be accessed. In order to access global addressing, specific global instructions must be used.

For example:

GLDD — Load double accumulator D (A:B) from global memory.

GSTAA — Store the contents of accumulator A into global memory

In Metrowerks CodeWarrior, the FAR qualifier is used to tell the compiler to use the global instructions included in the HCS12 CPU. An example of how to place the MFR4200 registers into the memory map is shown below.

Example:

```
#define BASE_ADDRESS 0x8000

#define    MNR    (*(volatile unsigned int* far)(0x000 + BASE_ADDRESS))

#define    MVR    (*(volatile unsigned int* far)(0x002 + BASE_ADDRESS))

#define    MCR0   (*(volatile unsigned int* far)(0x004 + BASE_ADDRESS))
```

In this option, the placement of the memory map can be changed by modifying the BASE_ADDRESS. The selected BASE_ADDRESS of 8000 is in the CS2# address range.[1]

6 Conclusions

The FlexRay controller can be connected to the HCS12 Family of MCUs, with a maximum interface clock frequency (to synchronize data transfer) of 8 MHz.

Due to this specific interface between the HCS12 microcontrollers and MFR4200 FlexRay controller, no glue logic required. Software configuration is also straightforward, the peripheral being simply memory-mapped into the global address space.

7 References

1. MC9S12DP256B Data Sheet
2. MFR4200 FlexRay Communication Controller Data Sheet

These documents are available on the Freescale Semiconductor web site at http://www.freescale.com.

More information on FlexRay and FlexRay products can be found at http://www.freescale.com/flexray

1. Many alternative methods of defining the MFR4200 register exist.

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