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Start-of-Frame Example Code

1 Introduction

This example code demonstrates how to program the MPC8272 to successfully generate Start-of-Frames (SOFs) for a USB host controller. The code includes proper CRC checking, as well as a byte ordering mechanism. The main purpose of the code is to show an example of the minimum programming requirements necessary to generate the SOFs. A few caveats are illustrated which are important to realize when designing a USB host interface with the MPC8272.

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2 Development Environment

The following equipment and settings were used to build the project:

- CodeWarrior™ for PPC version 8.6
- CodeWarrior Ethernet TAP
- Windows XP™
- MPC8272ADS
- MPC8272 processor
- Input clock -> 100MHz
- JP8 -> Host mode
- SW5 -> b10100100
- SW2 -> b0010
- HP1662A Logic Analyzer
- USB 1.1 probe from Future Plus Systems
- MPC850FADS

3 Details

The MPC8272 is a CPM-based product, which uses microcode to aid in the execution of various protocols. The USB controller also uses microcode to implement the protocol. In this example, the microcode is responsible for forming the Start-of-Frame packet and loading it into the FIFO for transmission. The user is responsible for programming the device to provide a hardware timer which will generate the 1ms time base that the host controller uses for packet transmission. The user is also responsible for generating the correct frame number and its corresponding CRC value, then placing the correct values in the FRAME_N register.

In this example, the SOF packets were prepared using the USBER[SOF] event register as a software trigger. This particular bit was used because it indicates that a SOF was just received by the controller. The next frame value should be prepared at the beginning of the previous frame reception to provide ample time. At this point, it's important to point out why there's a frame being received in the host controller. The FRAME_N register is used in both host and device mode with different functionality. Every time the host controller transmits a frame, the SOF packet is immediately received back on the receive line and placed in the FRAME_N register. If the CRC is valid for the particular frame, the valid bit will be set. After valid frame transmission, the FRAME_N register will contain only the frame number.

Another caveat about setting up the controller in host mode is that the MPC8272 is designed such that Endpoint 0 emulates the host's communication pipes. All host transmit and receive data happens over Endpoint 0. Therefore, in order to initialize the host controller, Endpoint 0 has to be initialized and at least one TxBD programmed. For this example, EP0's TxBD was minimally initialized to be the only BD in the ring and have a data length of zero.

The USB parameter RAM requires a certain amount of programming. Besides FRAME_N, the RSTATE value has to be cleared. Endpoint 0's PRAM also has to be minimally initialized. Clear the TSTATE bits, program the upper 16 bits of the IMMR value into HIMMR and set up TBASE are the main points.

4 File Structure

Main files:

mpc8272.h	Updated header file for MPC8272
main.c	Complete file for generating SOFs & CRCs
PQ27e_init.cfg	Generic Metrowerks configuration file

5 Verification

The code was verified using the HP1662A logic analyzer. The MPC8272ADS was connected upstream to the probe and the probe's Mictors were connected to the logic analyzer. On the downstream side of the probe, an MPC850FADS was used to provide the host with at least one device on the bus. This removes the reset signaling from the analyzer capture and provides a cleaner output. Numerous tests show the SOFs incrementing correctly and that the correct CRC value is being decoded by the analyzer.

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