Freescale Semiconductor
Application Note

DDR-SDRAM Layout Considerations for MCF547x/8x Processors

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This application note describes various design criteria that board and system designers should consider when implementing Double Data Rate (DDR) Synchronous Dynamic Random Access Memory (SDRAM) designs with the MCF547x and MCF548x ColdFire family of microprocessors. This application note discusses the critical parts of a DDR SDRAM memory sub-system design, particularly those related to printed circuit board (PCB) layout.

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1   Introduction

The MCF547x & MCF548x families are the first ColdFire microprocessor units (MPUs) with integrated FPU (Floating Point Unit) and MMU (Memory Management Unit) modules. They represent the highest performance devices currently available within the ColdFire processor family; the MCF547x @ 266 MHz offers 410 Dhrystone V2.1 mips (millions of instructions per second).

To provide the best price/performance ratio for embedded system designers, the ColdFire family has an integrated SDRAM memory controller module on-chip.

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This memory controller module has been through various revisions over the last eight years as DRAM memory architectures evolved, driven mainly by the requirements of the personal computer (PC) market. The most recent DRAM controller included on the MCF547x/8x family is a completely new design that supports the latest DRAM architecture: DDR SDRAM. These DRAM devices utilize a Stub Series Terminated Logic Version 2 (SSTL_2) means of connection and signalling between the MPU and the DDR SDRAM as described in JEDEC standard EIA/JESD8-9 (See Section 5, "References"). The advantage that DDR SDRAM offers over the previous standard DRAM memory SDR (Single Data Rate) SDRAM, is that data is clocked on both edges of the synchronous clock that is shared between the MPU and the DDR SDRAM. The result is a potential doubling of the bandwidth between the MPU and the DDR SDRAM.

As these V4e core ColdFire MPUs (MCF547x/548x families) utilize a full Harvard architecture on-chip, the extra bus bandwidth offered by the DDR SDRAM can be used to great effect to increase data/instruction throughput on the MPU. This is true particularly when processing blocks of data to/from some of the high speed peripheral modules on-chip (i.e., the PCI V2.2 bus controller, the two 10/100baseT Fast ethernet controllers and the one USB 2.0 high speed (480 Mbps) device port). The DDR SDRAM interface on this family of processors always runs at half the core frequency of the processor. For example, for the 266 MHz MCF547x processor the DDR SDRAM interface will operate at 133 MHz and clock data twice during every external clock cycle, thus offering a data throughput similar to the internal core buses running at 266 MHz. This in turn minimizes the performance penalty paid for off-chip accesses when fetching either code or data from the DDR SDRAM.

To locate any published errata or updates to this document, please refer to the website at http://www.freescale.com/coldfire.

2 DDR SDRAM Overview

The following terminology is used throughout this application note:

- SDRAM block—any group of DRAM memories selected by one of the MCF547x/8x SD_CS[3:0] signals. The MCF547x/8x can support up to four independent memory blocks. The base address of each block is programmed in the SDRAM chip select configuration registers (CSxCFG).
- SDRAM bank—an internal partition in an SDRAM device. For example, a 64-Mbit SDRAM component might be configured as four 512K x 32 banks. Banks are selected through the SD_BA[1:0] signals.
- SDRAM—RAM that operate like asynchronous DRAM, but with a synchronous clock, a pipelined, multiple-bank architecture, and faster speeds.
- Single data rate (SDR) SDRAM—SDRAM that drives/latches data and command information on the rising edge of the synchronous clock.

- Double data rate (DDR) SDRAM—SDRAM that latches command information on the rising edge of the clock; data is driven/latched on both the rising and falling edges of the clock rather than just the rising edge. This doubles data throughput rate without an increase in frequency. Currently the DDR SDRAM price continues to close on SDR SDRAM, and DDR SDRAM is already cheaper than SDR SDRAM in commodity densities, as shown in Figure 1.

Figure 1. SDR vs. DDR SDRAM Pricing

Spot Price - June, 2004				
Source: http://w w w .dramexchange.com				
Memory	Size	Config	Speed	Avg Price
SDR	256 Mb	32Mx8	133MHz	$ 5.00
DDR	256 Mb	32Mx8	400MHz	$ 4.80

Thus, in terms of price/performance, DDR SDRAM has recently overtaken SDR SDRAM.

As detailed above, data transactions are enabled on the rising and falling edges of the clock cycle, theoretically doubling the bandwidth of a DDR SDRAM based system as shown in Figure 2.

Figure 2. SDR and DDR SDRAM Data Latching
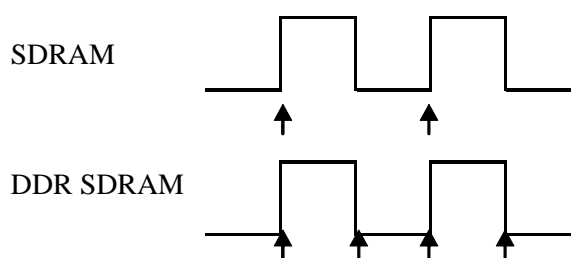
Therefore, the technology roadmap for SDRAM is to migrate to DDR SDRAM, initially utilizing memory configurations that already exist for SDR SDRAM.

In these high bandwidth SSTL signalling systems, the focus is on the system designer to ensure that the routing and termination of the address, control and data signals of the DDR SDRAM interface are such that they minimize noise and signal slew. These areas have become far more critical because the SSLT_2 signalling system, used by DDR SDRAM, by it's very nature (a set of balanced transmission lines requiring both series and parallel termination) is far more sensitive to noise and signal slew than previous SDR SDRAM signals. What may be new to system designers, and needs to be carefully considered, is the idea of a termination or switching voltage, as well as the standard supply voltage for the DDR SDRAM. For current DDR SDRAM the supply voltage is usually +2.5V, which is normally specified to operate at a +/-5% supply tolerance. The system designer must also supply a termination (VTT) or reference voltage (VREF) that is exactly halfway between VDD (supply +2.5V) and VSS (system ground 0V): an ideal +1.25V. This voltage can either be derived from the supply voltage using discrete components, or an integrated switching regulator with integrated MOSFETs. The latter is preferred, as well as one that is implemented on the MCF547x/MCF548x validation board (schematics and gerbers for this board design are available via the Freescale ColdFire website - www.freescale.com/coldfire). In volumes of 10K or more, this switching regulator will add approximately $3-4 to the overall system cost. Apart from the VREF supply, the only additional cost to a DDR SDRAM system is the addition of discrete termination

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resistors, both series (22 ohm) and parallel (51 ohm), to most of the DDR SDRAM signals between the MPU and the DDR SDRAM. On the validation board these termination resistors are housed in resistor packs to save PCB space.

2.1 DDR SDRAM Controller Implemented on the MCF547x/8x Family

The MCF547x/8x SDRAM controller contains a glueless interface to both SDR and DDR SDRAMs. Systems can contain either SDR SDRAM or DDR SDRAM, but a system containing both forms of SDRAM is not supported. The memory port width is fixed at 32 bits. Once data arrives on-chip there is a 64-bit data bus interface to the internal XLB 64-bit bus; this avoids any bandwidth bottlenecks on the SDRAM interface. The SDRAM controller also supports 32-byte critical word first burst transfers to aid with cache line fills. In terms of SDRAM device internal configurations supported, the controller can support up to 13 row address lines, up to 12 column address lines, 2 bits of bank address, and a maximum of four SDRAM chip selects. The maximum row bits plus column bits can be less than or equal to 24. Given current SDRAM memory devices, this enables support for up to 1 Gbyte of memory to be accessed: either 13+11 or 12+12 bits of, respectively, RA (Row Address) + CA (Column Address), 2-bit BA (Bank Address), and four chip selects (CS). The minimum memory configuration supported is 8 Mbytes: an 11-bit RA, 8-bit CA, 2-bit BA and one chip select. The SDRAM controller also supports page mode to maximize the data rate, SDRAM sleep mode, and self-refresh mode. Please note, error detection and parity checking are not supported by this SDRAM controller.

As stated the SDRAM controller supports up to 13 row addresses and up to 12 column addresses. When the SDRAM controller receives the internal module enable signal, it latches the internal bus address lines addresses[27:2] and multiplexes them into row, column, and row bank addresses. Addresses[9:2] are always used for CA[7:0], addresses[11:10] are always used for BA[1:0], and addresses[23:12] are always used for RA[11:0]. Addresses[27:24] can be used for additional row or column address bits, as needed.

NOTE

The SDRAM controller only supports an external 32-bit data bus. It is not possible to connect a smaller device(s) to only part of the SDRAM's data bus. For example, if 16-bit wide devices are used, then two 16-bit devices must be connected as a 32-bit port.

Table 1 shows the address multiplexing schemes available for this SDRAM controller.

Table 1. SDRAM Address Multiplexing

Device	Configuration	Row bit x Col bit x Banks	Total Block Size	SDCR [MUX] Setting	Internal Address						
					27	26	25	24	23–12	11–10	9–2
64 Mbits	512K x 32 bit	11 x 8 x 4	8 MB	00	—	—	—	—	RA11-0	BA1-0	CA7-0
	4M x 16 bit	12 x 8 x 4	16 MB	00	—	—	—	—			
	8M x 8bit	12 x 9 x 4	32 MB	00	—	—	—	CA8			
		13 x 8 x 4		01	—	—	—	RA12			
	16M x 4 bit	12 x 10 x 4	64 MB	00	—	—	CA9	CA8			
		13 x 9 x 4		01	—	—	CA8	RA12			
128 Mbits	4M x 32 bit	12 x 8 x 4	16 MB	00	—	—	—	—	RA11-0	BA1-0	CA7-0
	8M x 16 bit	12 x 9 x 4	32 MB	00	—	—	—	CA8			
		13 x 8 x 4		01	—	—	—	RA12			
	16M x 8 bit	12 x 10 x 4	64 MB	00	—	—	CA9	CA8			
		13 x 9 x 4		01	—	—	CA8	RA12			
	32M x 4 bit	12 x 11 x 4	128 MB	00	—	CA11	CA9	CA8			
		13 x 10 x 4		01	—	CA9	CA8	RA12			
256 Mbits	16M x 16 bit	12 x 10 x 4	64 MB	00	—	—	CA9	CA8	RA11-0	BA1-0	CA7-0
		13 x 9 x 4		01	—	—	CA8	RA12			
	32M x 8 bit	12 x 11 x 4	128 MB	00	—	CA11	CA9	CA8			
		13 x 10 x 4		01	—	CA9	CA8	RA12			
	64M x 4 bit	12 x 12 x 4	256 MB	00	CA12	CA11	CA9	CA8			
		13 x 11 x 4		01	CA11	CA9	CA8	RA12			
512 Mbits	32M x 16 bit	12 x 11 x 4	128 MB	00	—	CA11	CA9	CA8	RA11-0	BA1-0	CA7-0
		13 x 10x 4		01	—	CA9	CA8	RA12			
	64M x 8bit	12 x 12 x 4	256 MB	00	CA12	CA11	CA9	CA8			
		13 x 11 x 4		01	CA11	CA9	CA8	RA12			

All memory devices of a single chip select block must have the same configuration and row/column address width; however, this is not necessary between different blocks. If mixing different memory organizations in different blocks, the following guidelines will ensure that every block is fully contiguous:

- If all devices' row address width is 12 bits, the column address can be greater than or equal to 8 bits.
- If all devices' row address width is 13 bits, the column address can be greater than or equal to 8 bits.
- If all devices' column address width is 8 bits, the row address can be greater than or equal to 11 bits.
- x8 and x16 data width memory devices can be mixed (but not in the same space).

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- x32 data width memory devices cannot be mixed with any other width.

SDR SDRAM design requires special timing consideration for the SD_DQS[3:0] signals. For reads from DDR SDRAMs, the memory will drive the SD_DQSx pins so that the data lines and SD_DQSx signals have concurrent edges. The MCF547x/8x SDRAMC is designed to latch data 1/4 clock after the SD_DQS[3:0] edge. For DDR SDRAM, this ensures that the latch time is in the middle of the data valid window. The SDRAMC also uses the SD_DQS[3:0] signals to determine when read data can be latched for SDR SDRAM; however, SDR memories do not provide SDR_DQS outputs. Instead the SDRAMC provides an SDR_DQS output that is routed back into the controller as SD_DQS[3:0]. The SDR_DQS signal should be routed such that the valid data from the SDRAM reaches the MCF547x/8x at the same time or just before the SDR_DQS reaches the SD_DQS[3:0] inputs. When routing SDR_DQS, the outbound trace length should be matched to the SDCLK trace length, thus matching the trace length between the CPU and the SDR SDRAM for the other SDR SDRAM control signals. This will align SDR_DQS to the SDCLK as if the memory had generated the SD_DQS pulse. The inbound trace should be routed along the data path. Alternatively, a signal buffer/driver could be inserted to ensure that the SD_DQS[3:0] signals are all driven correctly, which would in turn add a delay to the initial SD_DQS signal. This should synchronize the SD_DQS signal so that the data is latched in the middle of the data valid window as shown below in Figure 3.
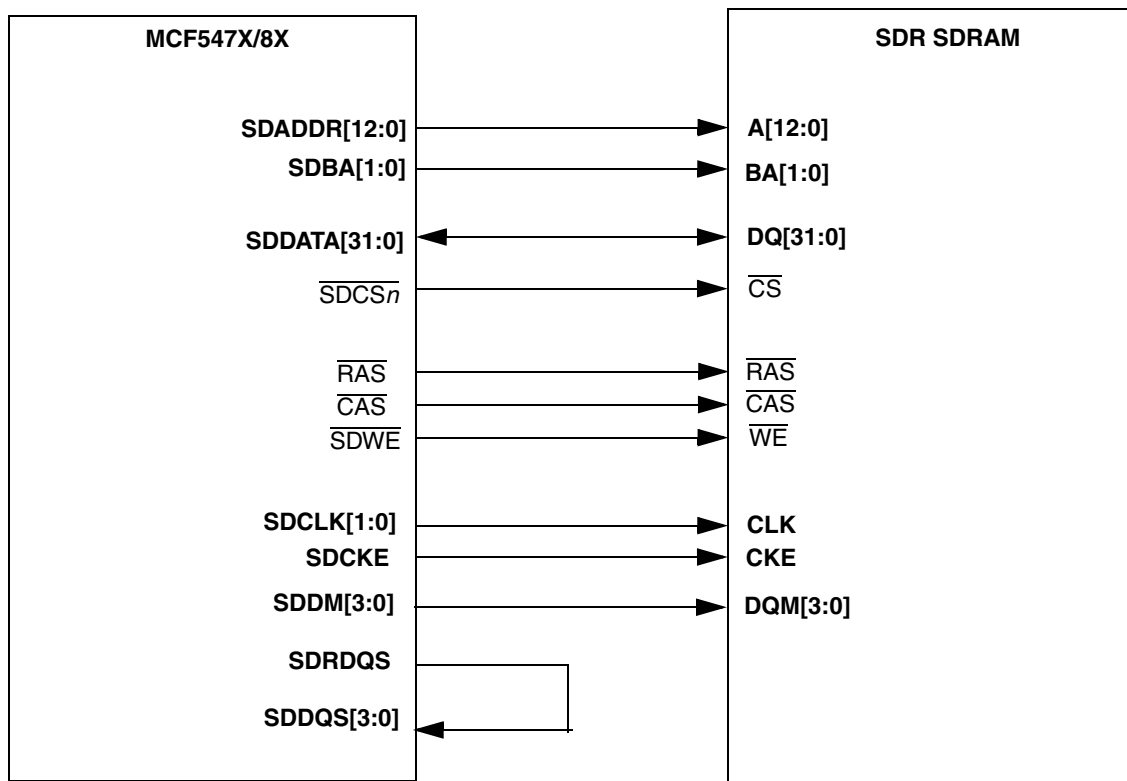
Figure 3. MCF547X/8X Connections to SDR SDRAM

DDR DRAM connection is far simpler, as shown in Figure 4; however, please look at the layout guidelines for routing between the MPU and the DDR SDRAM in Section 2.2, "Layout Guidelines." These are critical to DDR SDRAM operating correctly within a system.

For further details of the SDRAM controller, please refer to the Reference Manuals available for either the MCF547x or MCF548x microprocessor families. See Section 5, "References."

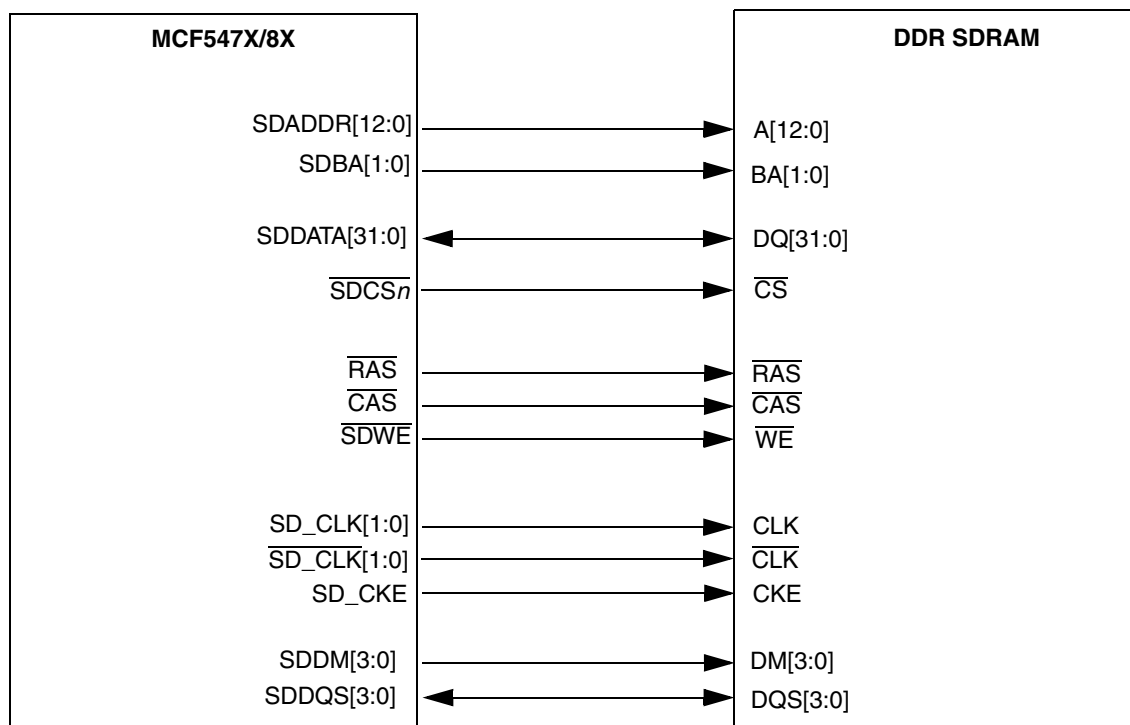**Figure 4. MCF547X/8X Connections to DDR SDRAM**

2.2   Layout Guidelines

Due to the critical timing required by DDR SDRAM, there are a number of considerations that should be taken into account during PCB layout:

- Minimize overall trace lengths between the MPU and DDR SDRAM. Trace lengths should be kept < 6 inches (15cm) if possible. NOTE: the layout of this particular board was constrained by the fact that a SMT socket was used on the first of these boards to validate first silicon functionality. As a result, the nearest tall components had to be at least 1.5" or 4 cm from the center of the footprint for the MCF547x/8x processor. In an embedded system without this constraint, the components could and should be placed as close as possible to the MPU, particularly the DDR SDRAM components.

- Each DQS, DM, and DQ group of signal traces must have identical loading and similar routing to maintain timing and signal integrity.

- Control and clock signals are routed point-to-point.

- Trace length for clock, address, and command signals should match to within +/- 1.25cm (500mil).

- Route DDR signals on layers adjacent to a ground plane, to minimize noise.

- Use a VREF plane under the SDRAM.

- VREF is decoupled from both SDVDD and VSS (GND).
- To avoid crosstalk, keep address and command signals separate (i.e. a different routing layer) from the data and data strobes.
- Use different resistor packs for command/address and data/data strobes.
- Use single series, single parallel termination (25 ohm series and 50 ohm parallel values are recommended, but standard resistor packs with similar values can be substituted).
- Series termination should be between the MCF547x and memory, but closest to the processor.
- Parallel termination is at the end of the signal line (close to the DDR SDRAM).
- 0.1 uF, 1nF & 100pF decoupling capacitors (COG or NPO dielectric) are used with the termination resistor packs.

Figure 5 shows the recommended termination for each of the signals between the MPU & DDR SDRAM. The series termination (25 ohms) should be placed as close to the MPU as possible and the parallel termination (50 ohms) as close as possible to DDR SDRAM. There can be some variation as to the specific termination values used as PCB manufacturing materials vary and hence overall board impedance can vary.
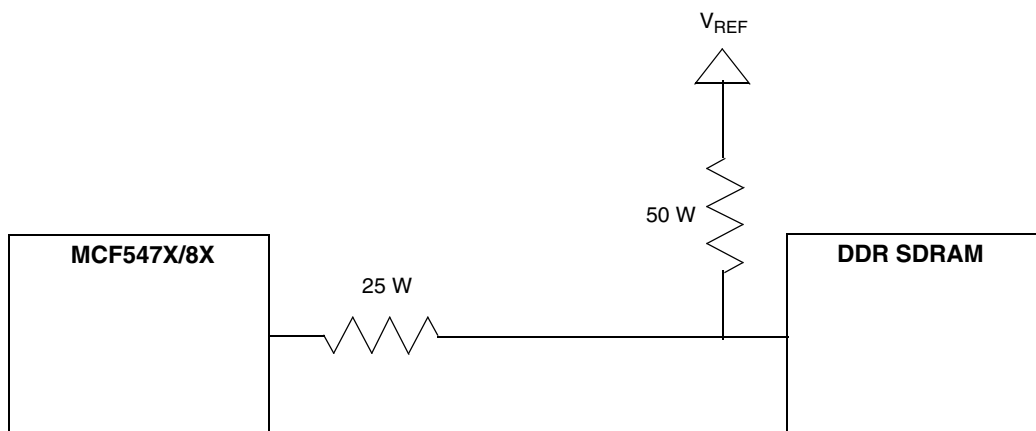
Figure 5. MCF547X/8X DDR SDRAM Termination Circuit

The validation PCB has 8 layers, the board stack for these layers is as follows:

- Top Layer - signal routing
- Power Plane - +3.3V
- Power Plane - +2.5V
- Routing Layer - Inner 1 routing
- Routing Layer - Inner 2 routing
- Power Plane - +1.5V
- Ground Plane
- Bottom layer - signal routing

The majority of the signal routing on this PCB was kept to the top and bottom layers to allow access to these signals in case they required modification. On a production system many of these signals could be routed on the inner layers of the board close to the ground plane to minimize noise, as suggested above. The track and space tolerances used on the board were a minimum of 6 thousandths of an inch. There was no variation of track width, which should be avoided because it can cause signal reflections. The PCB is constructed using FR4 material.

3 MCF547x/8x Validation Board DDR Layout

The following diagrams are taken from the MCF547x/8x validation board layout files. These files are available on the Freescale ColdFire website: http://www.freescale.com/coldfire. They are Gerber format files that show the whole PCB rather than concentrating on the connection between MPU and DDR SDRAM, as shown in the following diagrams.
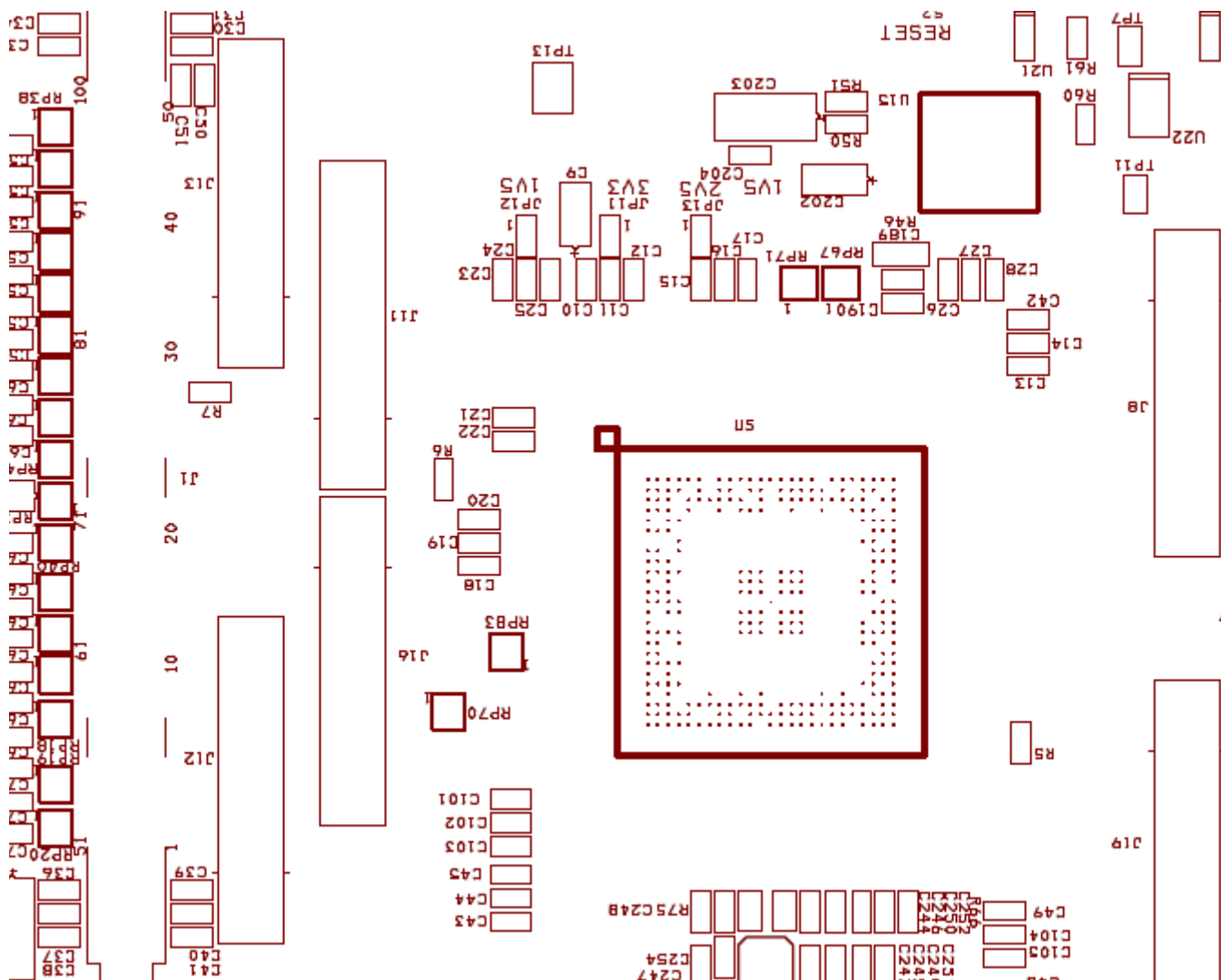
Figure 6. MCF547x/8x Validation Board Silkscreen

Figure 6 shows a portion of the top silk screen for the MCF5475/5484 validation board that details the MPU and DDR SDRAM memory module. The bounding box just below the U5 silkscreen label contains the SMT (Surface Mount Technology) BGA (Ball Grid Array) footprint for the MPU. J11, J12, J13 and J16 are SMT logic analyzer connectors for sampling the DDR SDRAM signals that might not be required in a system design, allowing the DDR SDRAM to be physically closer to the MPU. To the left of the MPU and beyond these connectors is the DDR SDRAM DIMM (Dual In-line Memory Module) outline. The outline for this part can be seen next to the pin numbering running up the diagram where 10, 20, 30 etc. represent the pin numbers on the DDR SDRAM DIMM. These numbers are particularly useful if the DIMM requires probing with an oscilloscope. The physical positioning of the DDR SDRAM DIMM was selected so that the control and address/data bus signals associated with the DDR SDRAM from the MPU had as physically short a path as possible, thus minimizing clock, control, and bus slew in the design. The area left unpopulated around U5 (MPU) on the top side of the board is deliberate: it allows a BGA socket to be fitted to test early the MCF5475 and MCF5485 silicon. The components closest to the MPU are the

decoupling capacitors that provide filtering on the three supply rails +3.3V, +2.5V and +1.5V DC in an attempt to by-pass as much digital noise as possible. An important consideration for the system designer is the selection of the value and dielectric material of these by-pass capacitors. Remember, it is not just the fundamental core MPU frequency (up to 266 MHz) that we need to filter. The third, fifth and seventh harmonics of this fundamental frequency (798 MHz, 1330 MHz, and 1862 MHz for a core frequency of 266 MHz) will also contain significant amounts of energy that can cause problems when attempting to get a finished system through EMC/CE testing. This is why there are not only 0.1uF and 1nF bypass capacitors in the design, but also 100pF capacitors on the MPU supplies close to the MPU. For bypass capacitors less than 0.1uF in value, a dielectric of either COG or NPO is preferred to X7R, as the former materials are far more self-resonant at these frequencies, and therefore liable to absorb far more digital switching noise.
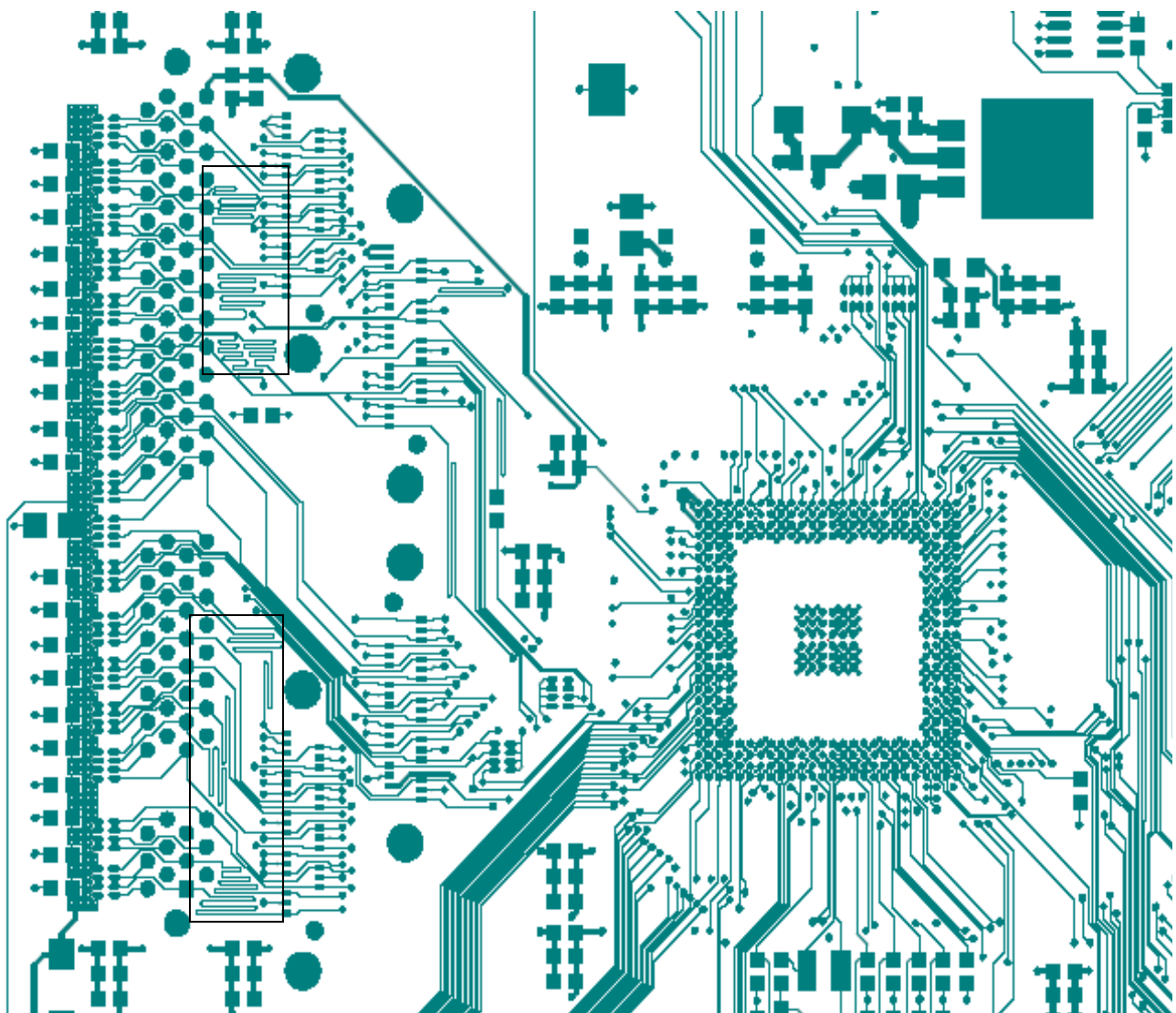
Figure 7. MCF547x/8x Validation Board Top Layer

Figure 7 details the top layer of signalling routing on the validation board between the MPU and the DDR SDRAM DIMM. There are several things of interest to the system designer. Firstly, look at some of the

tracks between the MPU and the DDR SDRAM footprint (the four columns of through board connections at a diagonal offset to the left of the MPU). If you look closely you will see that several of the signals have extra path lengths built into the tracking. This is done by looping the signal path back onto itself two or three times. Solid line bounding rectangles have been drawn around some of the more obvious examples. This routing has been done deliberately to try to keep all the DDR SDRAM signal track lengths within +/-1.25cm (500mil) of each other, thereby minimizing skew and delays between the MPU and DDR SDRAM. Secondly, note that to the left of the DDR SDRAM DIMM footprint there are footprints for a long line of termination resistor packs; flood filled under these is the power plane of VREF/VTT copper. This flood filling minimizes voltage drift and allows bulk decoupling of the plane to reduce system switching noise on this supply. To aid with the reduction of this switching noise behind the resistor pack footprints are a set of by-pass/decoupling capacitor footprints. Each resistor pack has at least one by-pass capacitor associated with it. Again, these capacitors contain COG or NPO dielectric material to absorb as much switching noise as possible via self-resonance.
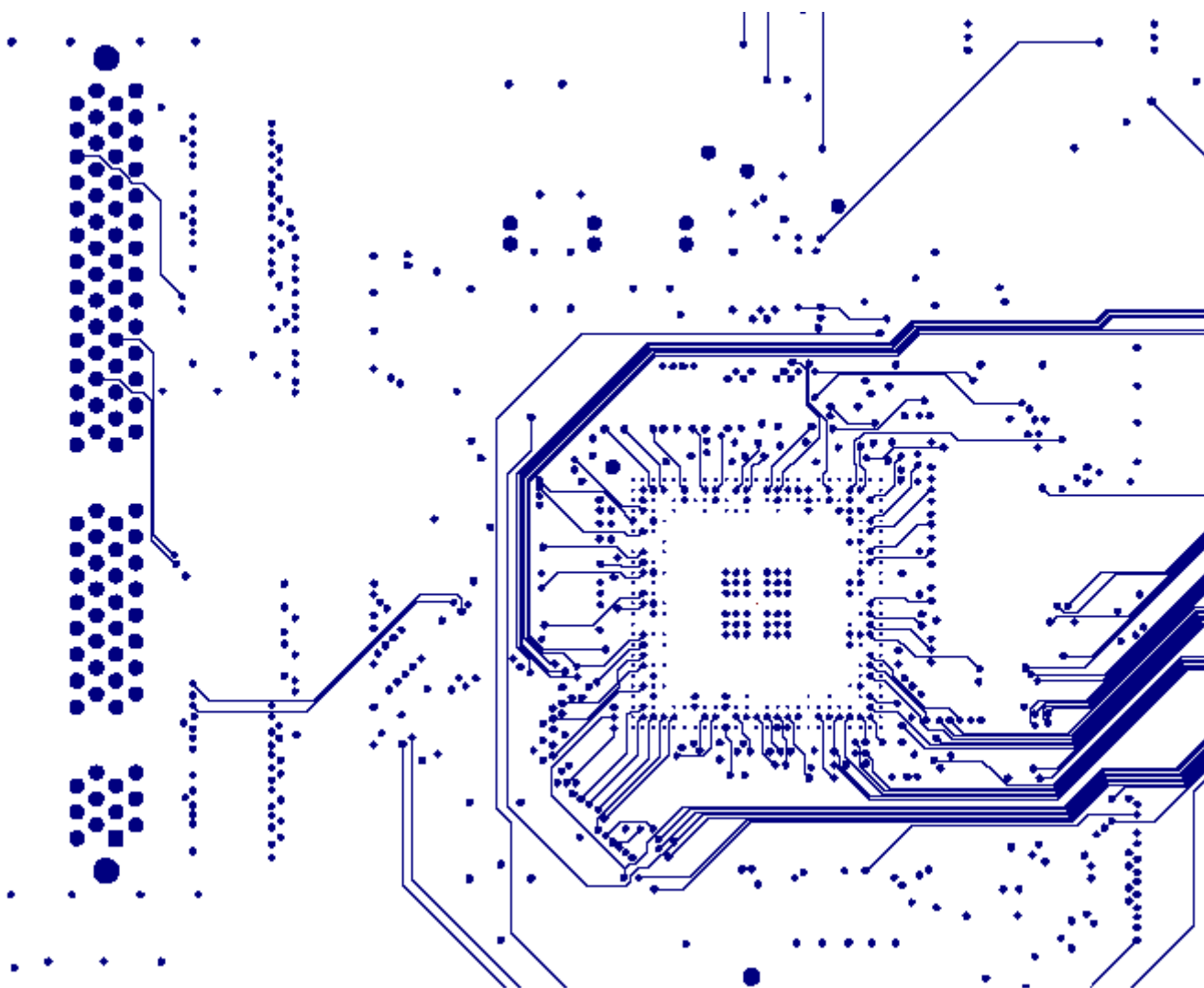
Figure 8. MCF547x/8x Validation Board Inner1 Layer

Figure 8 shows the first of the inner routing layers. The number of tracks on this layer is deliberately kept to a minimum, as any modifications to this layer would mean drilling the printed circuit board. On all layers tracks always use 45 degree angles, never 90 degree, to minimize noise in the form of reflections. Similarly the maximum distance tracks will run in parallel in close proximity is usually less then 2.5 cm (~1000 mil) if the signals are continuously switching to minimize cross talk noise between tracks.
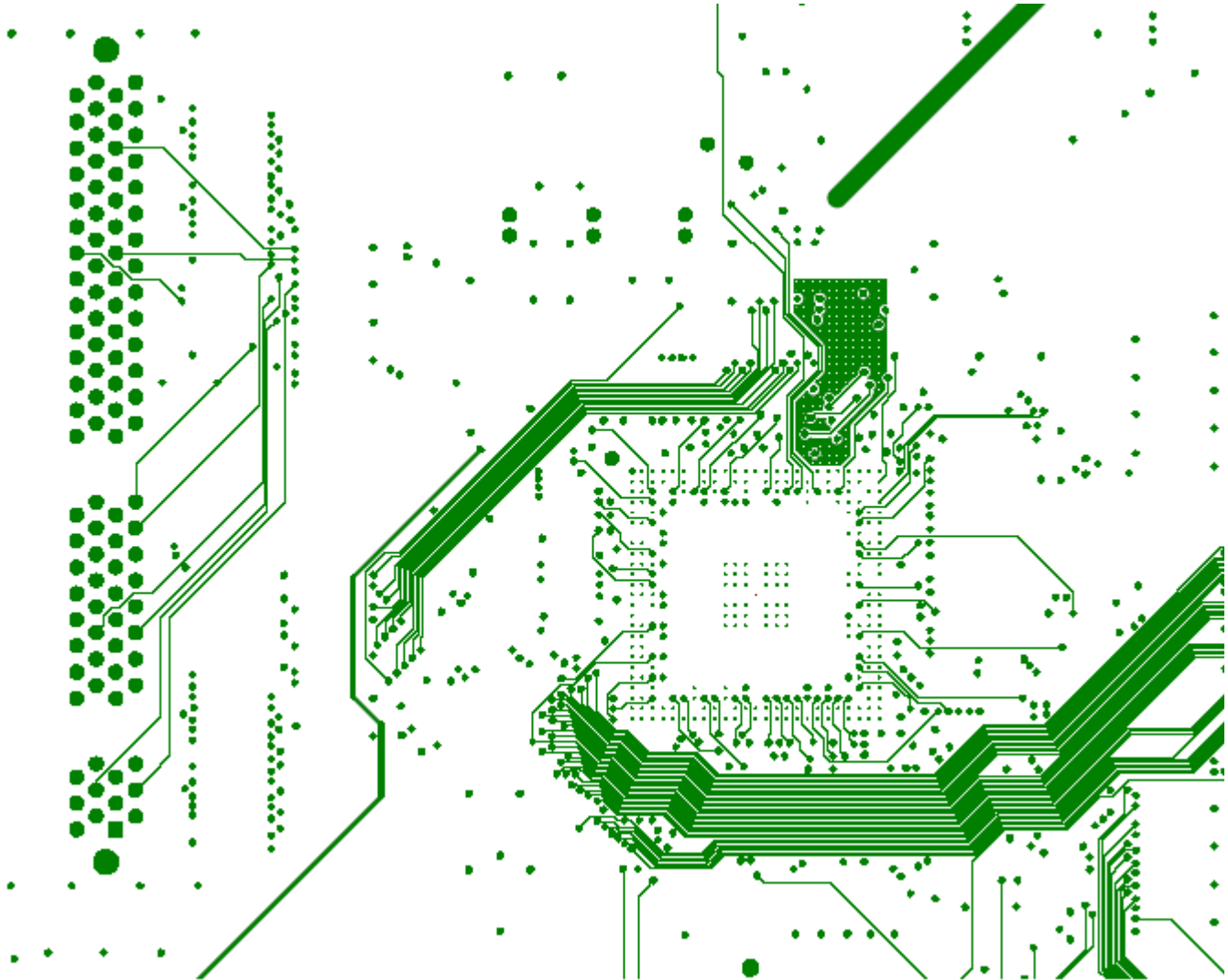
Figure 9. MCF547x/8x Validation Board Inner2 Layer

Figure 9 shows the second inner routing layer. This second layer shows tracking for the MPU Flexbus interface (below the MPU), as well as some DDR SDRAM interface routing from above the MPU, towards some vias which will then route on to the DDR SDRAM DIMM on another layer. For every track between the MPU and the DDR SDRAM DIMM, the layout tool was used to calculate the point to point distance of the track. It added the combined track lengths over the various layers on which it is routed. This ensures signal integrity in terms of skew, as well as the meeting of the target +/- 1.25cm (500mil) on all DDR SDRAM signal track lengths. Please note the flood-filled area above the MPU; this is a separate power

plane for the PLL supply on the MCF57x/548x MPU, which has a dedicated and heavily filtered supply to ensure there is a minimum of spurious noise that the PLL might incorrectly lock to.
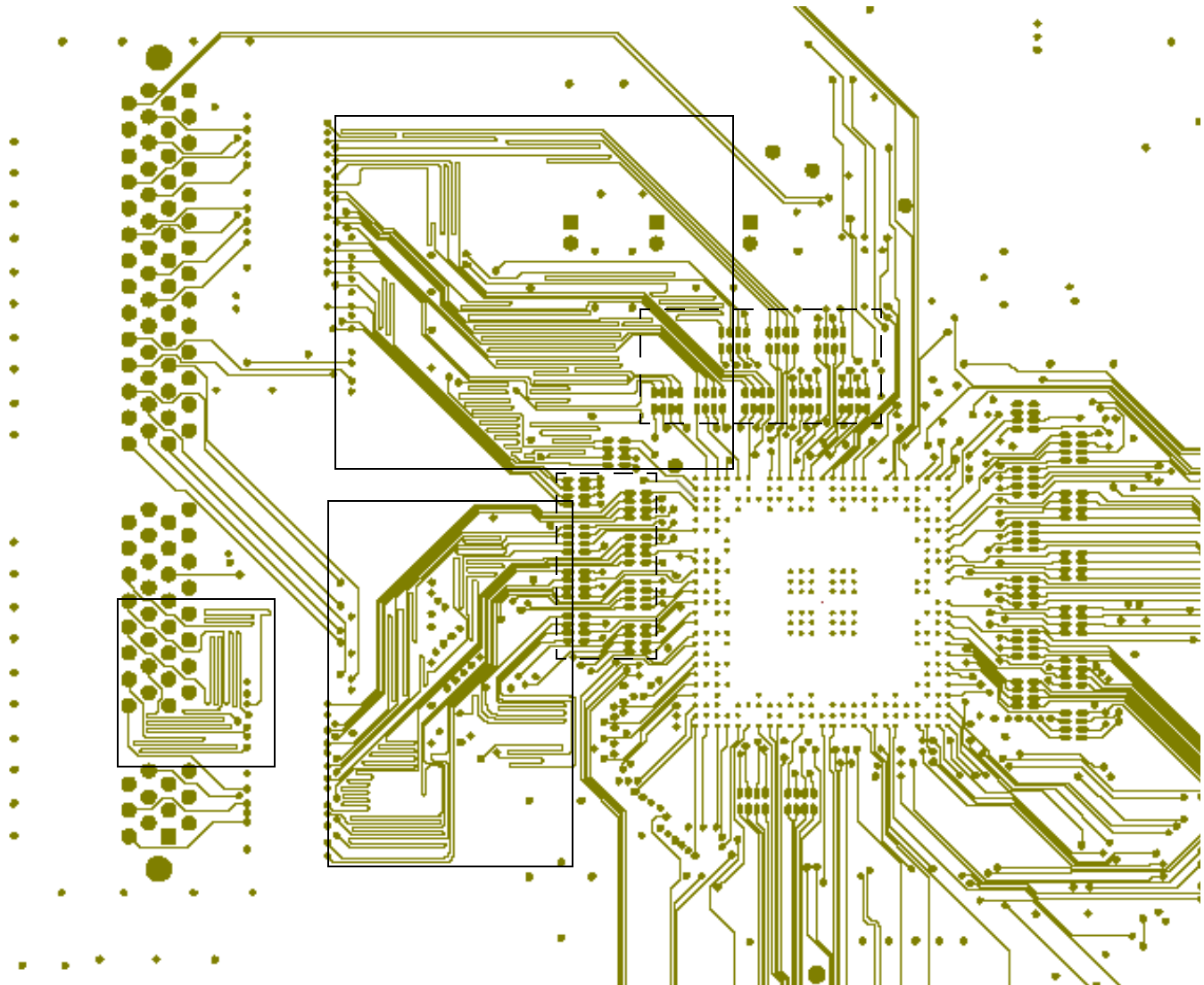
Figure 10. MCF547x/8x Validation Board Bottom Layer

Figure 10 shows the bottom routing layer of the validation board. Here again much of the DDR SDRAM tracking can be seen, as with the top layer, to allow modifications to be made more easily if need be. On this layer in particular the looping of various track signals can clearly be seen, as with the top layer. Again, the more obvious examples have been highlighted by the solid bounding boxes, to ensure a similar routing delay on the critical DDR SDRAM control signals. This layer clearly shows the 22 ohm series termination resistor pack footprints just to the left and above the MPU bounded by the rectangles made up of broken lines. These resistors need to be close to the source of the signal, so they are placed on the underside of the board as close as possible to the DDR SDRAM address bus, data bus, and control signals from the MPU. This layer also clearly shows the routing via the logic analyzer connectors to the left of the MPU (please see Figure 6, the silkscreen layer where J11, J12, J13 and J16 show their location). Most customers can avoid this to have the DDR SDRAM physically as close as possible to the MPU, which is recommended.
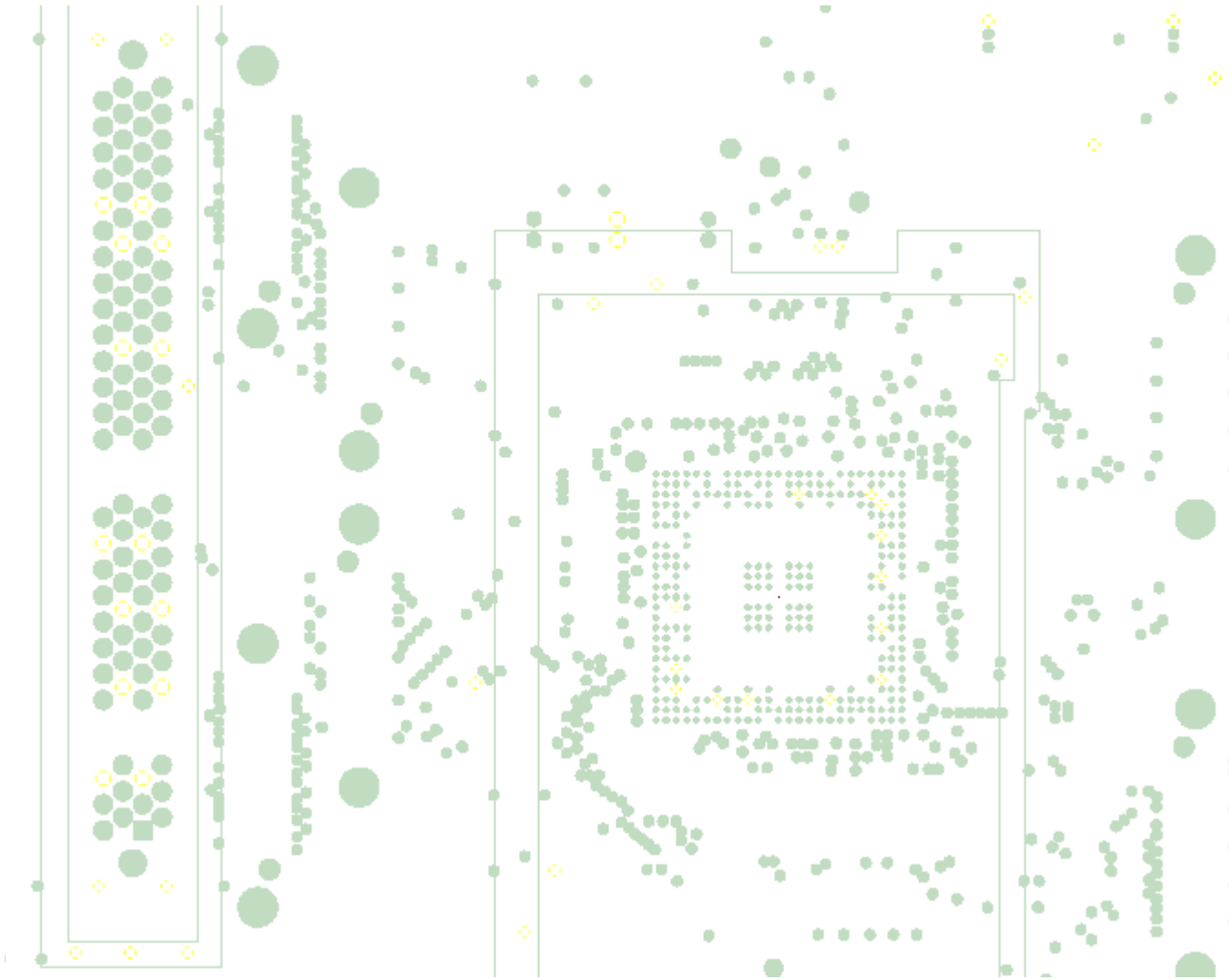
Figure 11. MCF547x/8x Validation Board Power Plane

Figure 11 shows one of the power planes (+3.3V) on the validation PCB. The other power planes (+1.5V & +2.5V) are not shown in this document because they are almost identical to the one shown above. Most importantly the plot above is a negative; white represents flood filled with copper. The holes shown in the copper are to accommodate through board components and thermal relief. The most critical thing to notice on this plot are the "boxes" around the footprint for the MPU and the DDR SDRAM DIMM. These areas of copper are created to force the supply to the MPU and DDR SDRAM DIMM through the de-coupling/bypass capacitors, thus increasing their effectiveness. If the reader refers back to the first diagram, the top silkscreen for the PCB (Figure 6), they will see that the decoupling capacitors for both the MPU and the DDR SDRAM are positioned along the edges of these boxes.
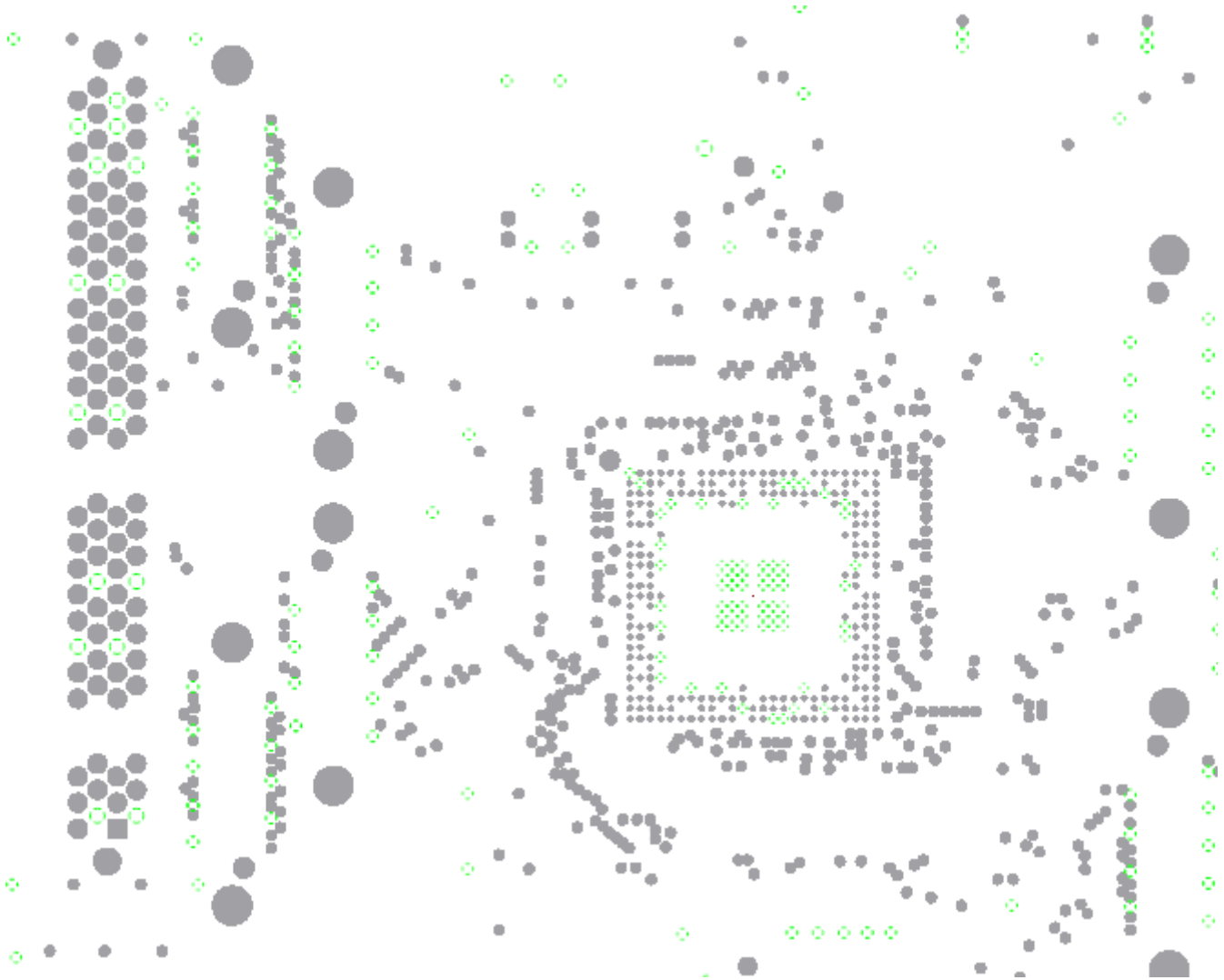
Figure 12. MCF547x/8x Validation Board Ground Plane

As with the previous diagram, Figure 12 is an inverse plot and white represents filled copper. This diagram shows the ground plane for the validation board. By flood filling the ground plane under the MPU and with the various power planes (+3.3V, +2.5V & +1.5V) above it, the PCB itself creates a by-pass/decoupling capacitor that will remove lower frequency noise (<1 MHz). The effectiveness of this will vary depending on the material used to manufacture the PCB, but FR4 (fiberglass) has proved quite effective on our evaluation and validation boards. As much of this layer is filled with copper as possible to minimize noise on the ground plane.

4 Summary

This application note has outlined the considerations that must be made when designing with DDR SDRAM and the MCF547x/548x family of processors. The major advantage of DDR SDRAM over SDR SDRAM is the data bandwidth available, theoretically a doubling of bandwidth. This increase in

performance, however, does mean that the system designer must pay particular attention to their PCB layout, as detailed above.

The overall gains made by using DDR SDRAM far outweigh the extra care that needs to be taken during PCB design. DRAM memory, in various modes of operation, will continue to lead the memory price/performance roadmap driven by the PC market. The embedded system designer can currently take advantage of this by utilizing DDR SDRAM memory in their embedded system design.

5   References

Table 2 provides a list of Freescale references used throughout this application note.

Table 2. References

Freescale Document Number	Title	Revision
MCF5475RM/D	MCF5475/4/3/2/1/0 Reference Manual	1.2
MCF5485RM/D	MCF5585/4/3/2/1/0 Reference Manual	1.1
CFPRM/D	ColdFire Family Programmer's Reference Manual	2

Table 3 provides a non-Freescale set of references used throughout this application note.

Table 3. Non-Freescale References

Document Number	Title	Revision
JESD79C	JEDEC DDR SDRAM spec. EIA/JESD8-9	March 2003

6   Document Revision History

Table 4 provides a document revision history for this application note.

Table 4. Document Revision History

Rev. No.	Substantive Change(s)	Date of Release
0	Initial Release	June 2004

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