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Application Note

Migrating from the MPC859T to the MPC885

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This document contains summary information that is useful when migrating from the MPC859T to the MPC885. For more detailed information, refer to the *MPC885 PowerQUICC Family Reference Manual* and *MPC880/MPC885 Hardware Specifications (*for the MPC885*)* and to the *MPC866 PowerQUICC Family Users Manual* and *MPC866859T/859DSL Hardware Specifications (*for the MPC859T*)*.

Contents

1   Overview

The need for embedded security and an additional Fast Ethernet channel makes the transition from an MPC859T to an MPC885 a logical progression. Both processors contain the same embedded architecture-based core and system integration unit (SIU) to ease software migration.

The MPC885 has twice the internal L1 cache as the MPC859T for a total of 8 Kbytes for data and 8 Kbytes for instructions. The MPC885 has a faster bus speed than the MPC859T. The MPC885 incorporates four 16-bit timers that can be cascaded into two 32-bit timers.

The MPC885 incorporates two Fast Ethernet channels, instead of one, and has a similar CPM. However, the variety of serial channels has changed. While both the MPC859T and the MPC885 feature UTOPIA, the MPC885 can support full duplex UTOPIA

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and Fast Ethernet simultaneously. The MPC885 also has a USB 1.1 controller and an on-chip security processor that can perform encryption on the serial channels and TDM interface.

Figure 1 and Figure 2 show block diagrams for MPC885 and MPC859T, respectively.

2 Feature Comparison

The MPC859T and the MPC885 communications microprocessors incorporate many types of communications engines to accommodate different system requirements. The following sections discuss hardware and protocol features of both microprocessors.

2.1 Hardware Features

Table 1 compares the MPC859T and the MPC885 hardware features.

Table 1. Hardware Features Comparison

Feature	MPC859T	MPC885
Core frequency (max)	133 MHz	133 MHz
Bus frequency (max)	66 MHz	80 MHz
I and D cache	4K	8K
FEC	1	2
Security	No	Yes
USB 1.1	No	Yes
Time slot assigner (TSA)	Yes	Yes
SPI	1	1
SMC	2	2
SCC	1	3
PCMCIA	Yes	Yes

2.2 Protocol Features

Table 2 compares the MPC859T and the MPC885 protocol features.

Table 2. Protocol Feature Comparison

Protocol	MPC859T	MPC885
10/100 Fast Ethernet	1	2
10BT Ethernet	Yes	Yes
HDLC/SDLC	Yes	Yes
UART	Yes	Yes
Transparent	Yes	Yes

3 MPC885

The MPC885 PowerQUICC™ is a 0.18 µm version of the MPC860 PowerQUICC family of communications microprocessors. The MPC885 has a core voltage of 1.8 V and an I/O voltage of 3.3 V, with 5V-input compatibility (on some I/O pins). The MPC885 supports a maximum core speed of 133 MHz and a maximum external bus speed of 80 MHz (in 1:1 mode).

The MPC885 incorporates the same embedded MPC8XX processor core and similar CPM and SIU. The MPC885 also supports an on-chip security engine and two 10/100 Fast Ethernet controller modules. The CPM supports USB 1.1, three SCCs (SCC2, SCC3, and SCC4), two SMCs (SMC1 and SMC2), SPI, and I^{2}C. The SCCs can support 802.3 Ethernet, ATM, HDLC/SDLC, UART and transparent protocols.

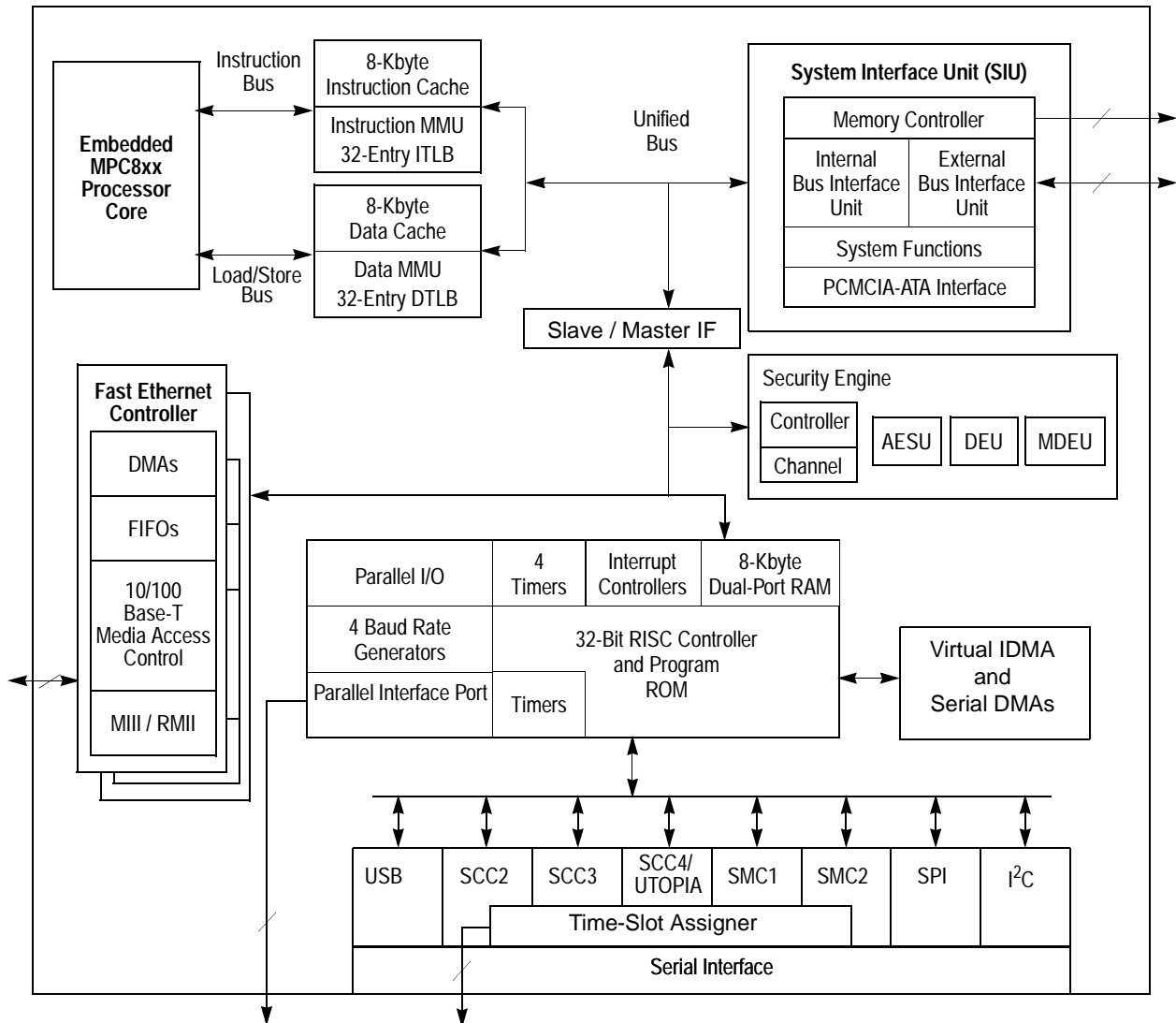Figure 1 shows the MPC885 block diagram.

Figure 1. MPC859T Block Diagram

4 MPC859T

The MPC859T PowerQUICC is a 0.18 μm version of the MPC862 PowerQUICC family of communications microprocessors. The MPC859T has a core voltage of 1.8 V and an I/O voltage of 3.3 V, with 5V-compatibility. The MPC859T supports a maximum core speed of 133 MHz and a maximum external bus speed of 66 MHz.

The MPC859T incorporates the same embedded MPC8XX processor core and similar CPM and SIU as the MPC8XX family. The MPC859T features one 10/100 Fast Ethernet controller module. The CPM supports one SCC (SCC1), two SMCs (SMC1 and SMC2), SPI and I^2C. The SCC can support 802.3 Ethernet, ATM, HDLC/SDLC, UART, and transparent protocols.
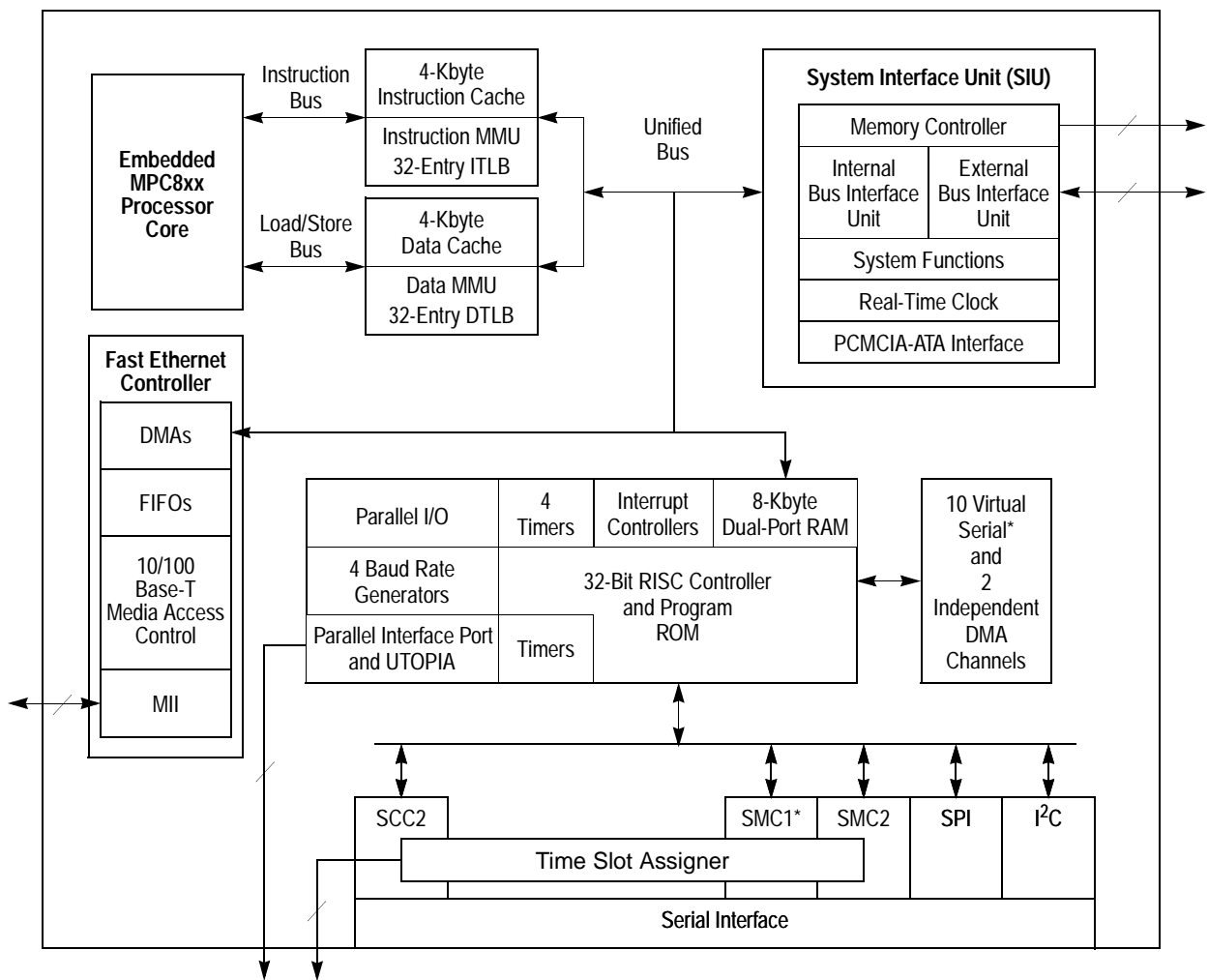
Figure 2. MPC859T Block Diagram

5 Similarities and Differences between the MPC859T and the MPC885

The following sections discuss pinout and memory mapping differences for the MPC859T and the MPC885.

5.1 Pinout

Both the MPC859T and the MPC885 use the 357 plastic ball grid array (PBGA) package. Buses and other functions were grouped in a logical order, but reuse of layout is not available. Parallel ports changed from four (Port A, B, C, and D) on the MPC859T to five (Port A, B, C, D, and E) on the MPC885. Each signal in the I/O ports can be configured as a general-purpose I/O signal or as a signal dedicated to supporting communications peripherals, such as Ethernet or USB. See the *MPC885 PowerQUICC Family Reference Manual* for more information.

Figure 3 shows the MPC885 pinout.
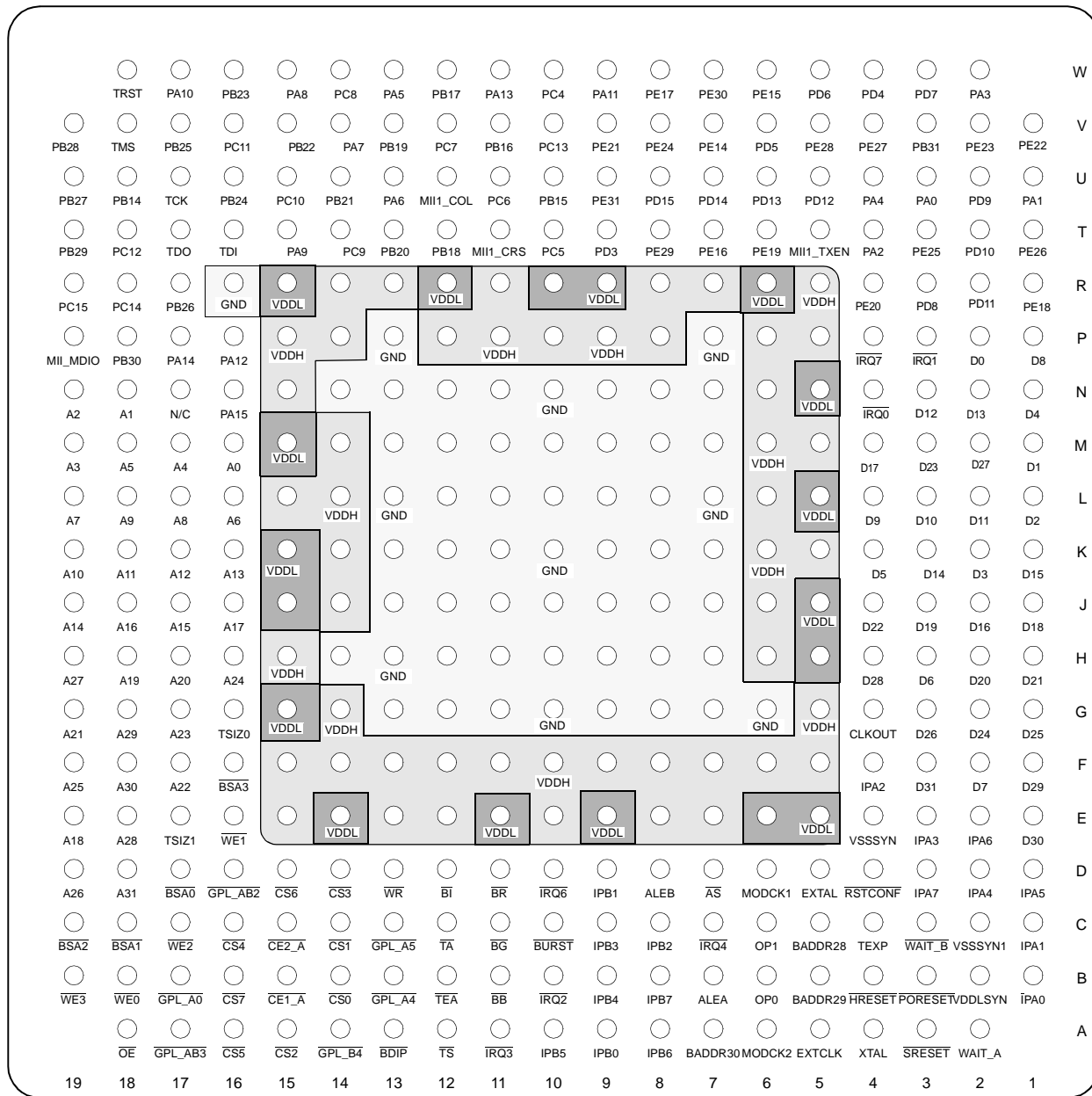
NOTE: This is the top view of the device.

Row	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
W		TRST	PA10	PB23	PA8	PC8	PA5	PB17	PA13	PC4	PA11	PE17	PE30	PE15	PD6	PD4	PD7	PA3	
V	PB28	TMS	PB25	PC11	PB22	PA7	PB19	PC7	PB16	PC13	PE21	PE24	PE14	PD5	PE28	PE27	PB31	PE23	PE22
U	PB27	PB14	TCK	PB24	PC10	PB21	PA6	MII1_COL	PC6	PB15	PE31	PD15	PD14	PD13	PD12	PA4	PA0	PD9	PA1
T	PB29	PC12	TDO	TDI	PA9	PC9	PB20	PB18	MII1_CRS	PC5	PD3	PE29	PE16	PE19	MII1_TXEN	PA2	PE25	PD10	PE26
R	PC15	PC14	PB26	GND	VDDL			VDDL		VDDL				VDDL	VDDH	PE20	PD8	PD11	PE18
P	MII_MDIO	PB30	PA14	PA12	VDDH		GND		VDDH		VDDH		GND			IRQ7	IRQ1	D0	D8
N	A2	A1	N/C	PA15						GND				VDDL		IRQ0	D12	D13	D4
M	A3	A5	A4	A0	VDDL									VDDH		D17	D23	D27	D1
L	A7	A9	A8	A6	VDDH	GND					GND			VDDL		D9	D10	D11	D2
K	A10	A11	A12	A13	VDDL					GND				VDDH		D5	D14	D3	D15
J	A14	A16	A15	A17										VDDL		D22	D19	D16	D18
H	A27	A19	A20	A24	VDDH		GND									D28	D6	D20	D21
G	A21	A29	A23	TSIZ0	VDDL	VDDH				GND				GND	VDDH	CLKOUT	D26	D24	D25
F	A25	A30	A22	BSA3						VDDH						IPA2	D31	D7	D29
E	A18	A28	TSIZ1	WE1		VDDL		VDDL		VDDL				VDDL		VSSSYN	IPA3	IPA6	D30
D	A26	A31	BSA0	GPL_AB2	CS6	CS3	WR	BI	BR	IRQ6	IPB1	ALEB	AS	MODCK1	EXTAL	RSTCONF	IPA7	IPA4	IPA5
C	BSA2	BSA1	WE2	CS4	CE2_A	CS1	GPL_A5	TA	BG	BURST	IPB3	IPB2	IRQ4	OP1	BADDR28	TEXP	WAIT_B	VSSSYN1	IPA1
B	WE3	WE0	GPL_A0	CS7	CE1_A	CS0	GPL_A4	TEA	BB	IRQ2	IPB4	IPB7	ALEA	OP0	BADDR29	HRESET	PORESET	VDDLSYN	IPA0
A		OE	GPL_AB3	CS5	CS2	GPL_B4	BDIP	TS	IRQ3	IPB5	IPB0	IPB6	BADDR30	MODCK2	EXTCLK	XTAL	SRESET	WAIT_A	

Figure 3. MPC885 Pinout

Figure 4 shows the MPC859T pinout.

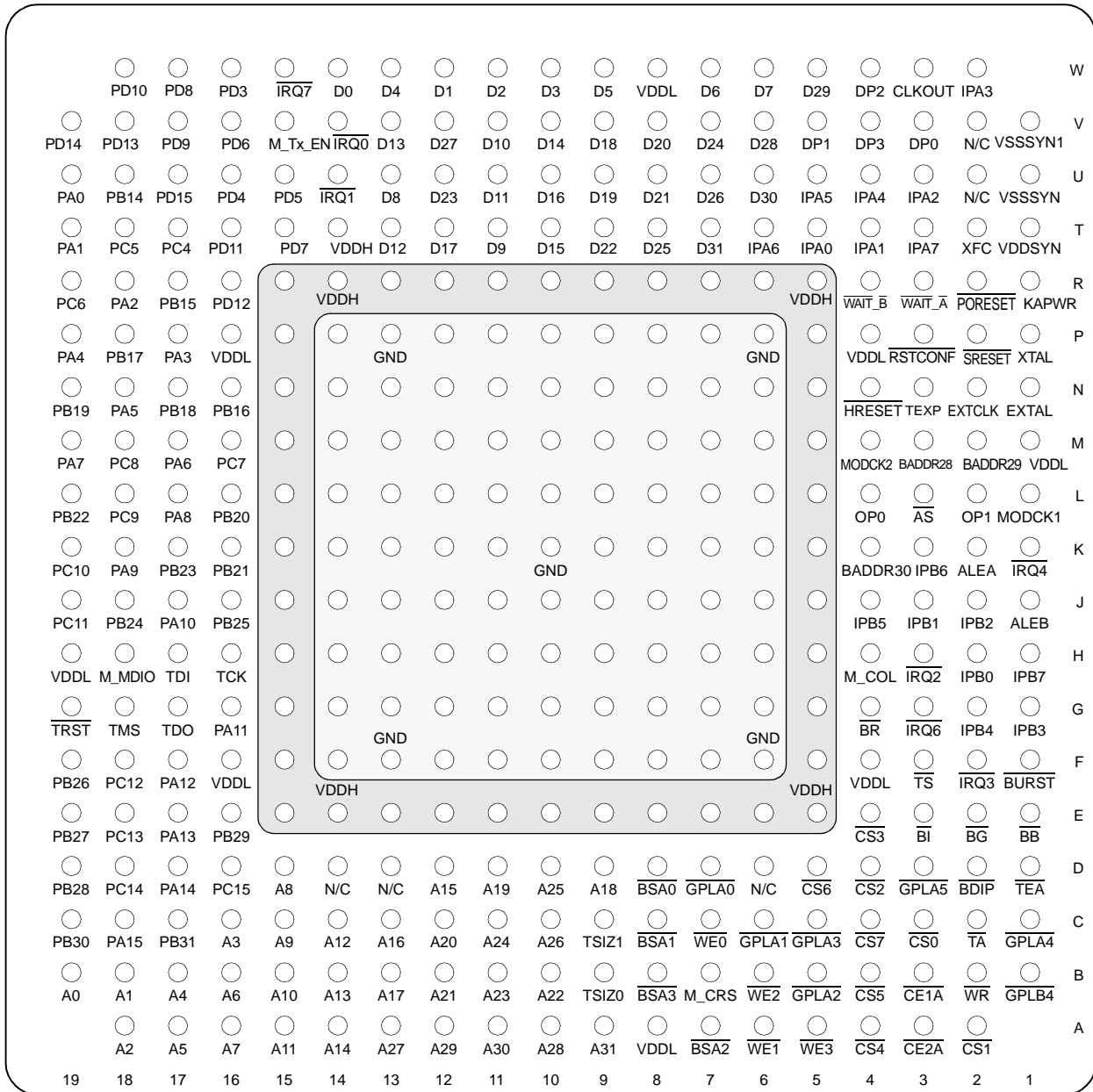**NOTE: This is the top view of the device.**

Figure 4. MPC859T Pinout

5.2 Memory Map

The memory maps for both the MPC859T and the MPC885 are very similar except for a few differences:

- The SCC1 in the MPC859T is replaced with a USB 1.1 controller.
- Reserved space (offset 0xA20-0xA77) in the MPC859T is now for SCC2 and SCC3 in the MPC885.

- Port E registers in the MPC885 reside in a previously reserved area of the Port B registers in the MPC859T (starting at offset 0xAC8).

- The registers mapped for the FEC registers in the MPC859T are now mapped for FEC1 for the MPC885. The immediate reserved space following the FEC registers in the MPC859T is the location for the FEC2 registers in the MPC885 (starting at offset 0x1E00). For ease of porting, FEC2 registers are located in the same order as FEC1, with offset for FEC2 equal to FEC1 plus 0x1000.

- Dual-port RAM for both processors is from IMMR + 0x2000-0x2FFF, with expanded dual-port RAM from 0x3000-0x3BFF.

- The MPC859T's memory resources are mapped to a contiguous 64 Kbyte block; the MPC885's memory resources are mapped to a contiguous 256 Kbyte block, as shown in Figure 5, that includes the security block in the upper 128 Kbytes.

- Bits 14–15 in the 16-bit field IMMR[ISB] have new meaning in the MPC885. When IMMR[ISB] bits 14–15 are cleared, the internal memory map is the same as in the MPC859T. When IMMR[14–15] = 10, an additional 128 Kbyte memory block becomes available for the security engine, as shown in Figure 5.
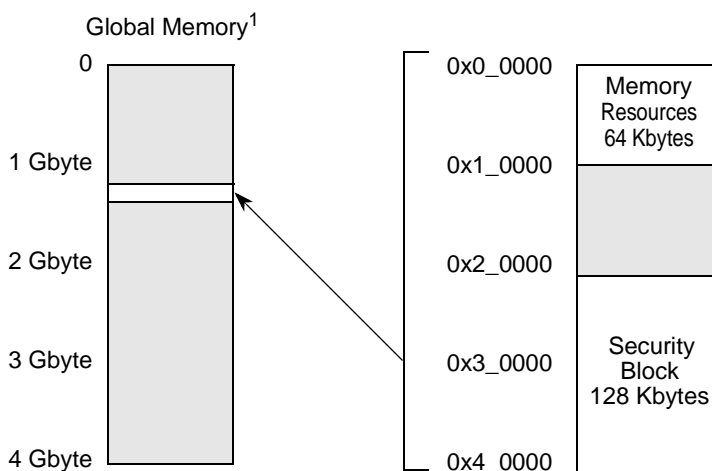
[1] Location of contiguous 256-Kbyte block of internal memory resources in this figure is for illustration only. The addresses shown are offsets from the IMMR.

Figure 5. MPC885 Memory Map

6 New Features for MPC885

The following sections discuss the new features for the MPC885.

6.1 Hardware Changes

The following are the hardware changes from the MPC859T to the MPC885:

- There is no data parity generation /checking.
- The MPC885 only supports normal high and normal low power modes.

6.2 Security Engine

The block diagram of the security engine's internal architecture is shown in Figure 6. The MPC8XX bus interface module is designed to transfer 32-bit words between the MPC8XX bus and any register inside the security engine core.
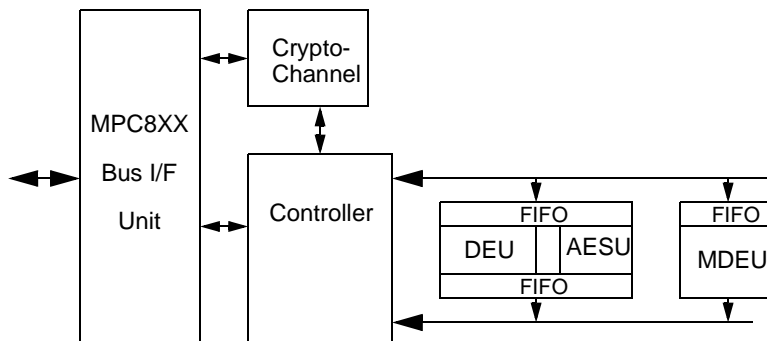
Figure 6. Security Engine Functional Blocks

An operation begins with a write of a pointer to the crypto-channel fetch register, which points to a data packet descriptor. The channel requests the descriptor and decodes the operation to be performed. The channel then asks the controller to assign crypto execution units and fetch the keys, IVs, and data needed to perform the specific operation. The controller assigns execution units to the channel and makes requests to the master interface to satisfy the requests. As data is processed, it is written to the individual executions unit's output buffer and then back to system memory by means of the MPC8XX I/F module.

The internal registers for the security engine can be accessed when IMMR [ISB]14–15 = 10. The *MPC885 PowerQUICC Family Reference Manual* lists details of the registers and their locations in the internal memory map.

7 Summary

Although the migration from the MPC859T to the MPC885 requires layout and software changes, the benefits of an additional Fast Ethernet controller, USB 1.1, and an internal security engine may warrant the migration, depending on system requirements.

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