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Implementing an Ethernet Interface with the MC9S12NE64

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Introduction

This application note provides recommendations for implementing an Ethernet interface with the MC9S12NE64 microcontroller unit (MCU). The discussion covers many topics including:

- Overview of the MC9S12NE64 including available packages
- Components required to add Ethernet functionality to the MC9S12NE64
- MC9S12NE64 schematics showing the minimum system design
- Circuit connections between the MC9S12NE64 and a high-speed LAN magnetics isolation module and RJ45 connector
- General printed circuit board (PCB) layout recommendations for 10 and 100 Mbps Ethernet design
- High-speed LAN magnetics isolation module requirements
- Crystal placement and circuitry recommendations
- MC9S12NE64 Ethernet design examples in both 112-pin and 80-pin packages

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Figure 1 shows a preview of the design examples:

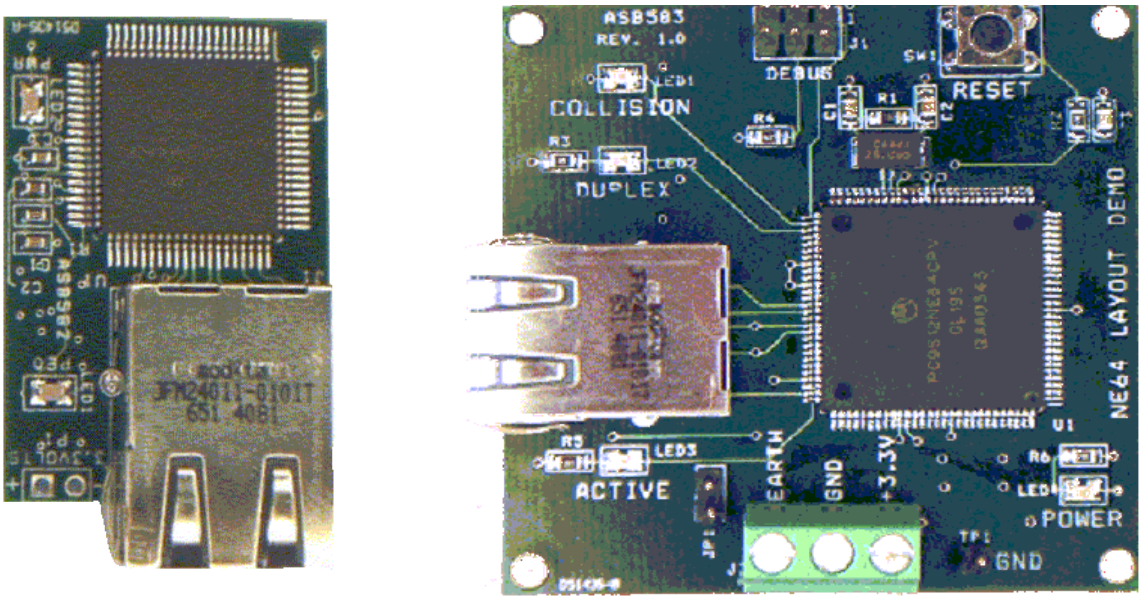


Figure 1. Design Examples

MC9S12NE64 Single-Chip Ethernet Solution

This section introduces the MC9S12NE64 and provides an overview of the MC9S12NE64 integrated Ethernet controller and MC9S12NE64 system design.

MC9S12NE64 Overview

The MC9S12NE64 is a 16-bit MCU based on Freescale Semiconductor's HCS12 CPU platform. It includes 8K bytes of RAM and 64K bytes of FLASH memory. In the 80-pin package, the MC9S12NE64 has other standard on-chip peripherals including two asynchronous serial communications interface modules (SCIs), one synchronous serial peripheral interface (SPI), an inter-integrated circuit bus (IIC), a 4-channel/16-bit timer module (TIM), an 8-channel/10-bit analog-to-digital converter (ADC), and up to 18 pins available as keypad wake-up inputs (KWUs) or general-purpose I/O pins. In addition, an expanded bus that can be operated at 16 MHz[1] is available on the 112-pin package.

The MC9S12NE64 introduces a new peripheral for the HCS12 CPU platform, an integrated Ethernet controller. The MC9S12NE64 integrates an Ethernet controller that includes a media access controller (MAC) and a physical transceiver (PHY) in one die with the CPU, memory, and other HCS12 standard on-chip peripherals. The MC9S12NE64 integrated Ethernet controller is compatible with IEEE 802.3 and 802.3u specifications for 10-Mbps or 100-Mbps operation, respectively.

1. At a 16-MHz internal bus speed, the MC9S12NE64 integrated Ethernet controller is limited to 10-Mbps operation. A 25-MHz internal bus speed is required for 100-Mbps operation.

The MC9S12NE64 can be targeted at low-throughput connectivity applications that require operation from a nominal 3.3-V power supply. With an on-chip bandgap-based voltage regulator (VREG), the internal digital supply voltage of 2.5 V (V_{DD}) will be generated internally. Figure 2 shows a block diagram of the MC9S12NE64. More information on the MC9S12NE64 is available from the Freescale Semiconductor website: http://freescale.com.

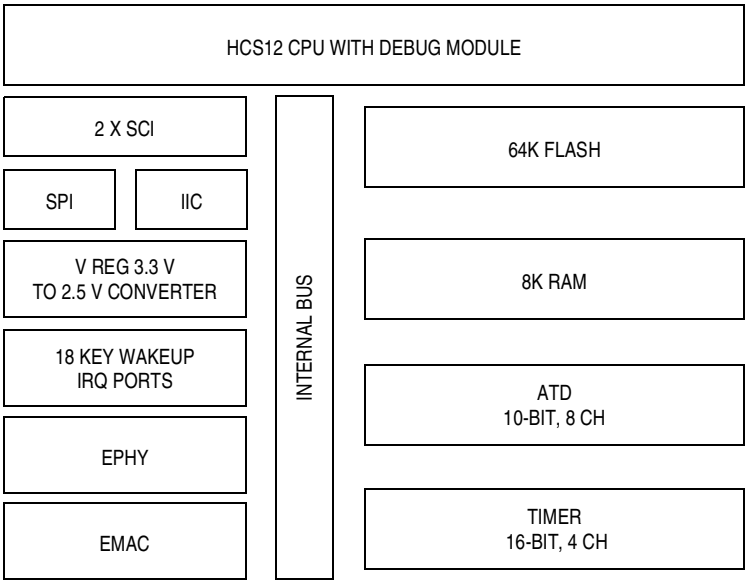


Figure 2. Block Diagram of the MC9S12NE64

MC9S12NE64 Packages

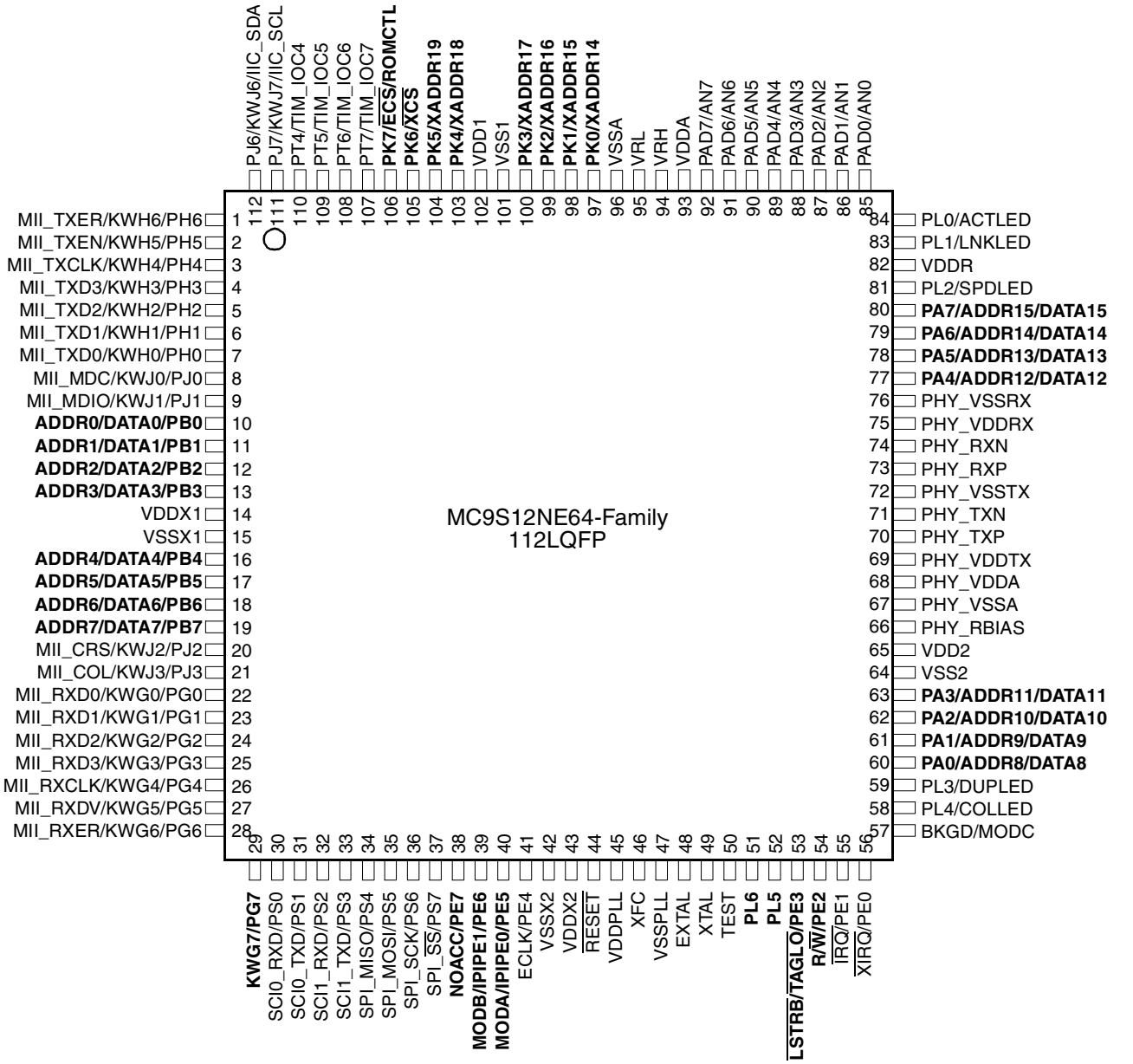
The MC9S12NE64 is available in two packages. Table 1 provides device numbers for each package Figure 3 shows the 112-pin LQFP package pin-out. Figure 4 shows the 80-pin TQFP-EP package pin out.

Table 1. MC68HCS908NE64 Package Options

Device Number	Mask Set	Temp	Package
MC9S12NE64CFU	0L19S	–40° C, 85° C	80TQFP-EP
MC9S12NE64CPV	0L19S	–40° C, 85° C	112LQFP

- 112-pin LQFP package — 70 I/O port pins and 10 input-only pins
- 80-pin TQFP-EP package — 38 I/O port pins and 10 input-only pins

The 80-pin TQFP-EP package does not have access to the multiplex address and data bus. It is designed for single-chip applications that use the internal FLASH and RAM memory. The 80-pin TQFP-EP package has an exposed flag for heat dissipation and requires special PCB layout to accommodate the flag. See the Exposed Flag section.



Signals shown in **Bold** are not available on the 80-pin package.

Figure 3. Pinout of MC9S12NE64 in 112-Pin LQFP Package

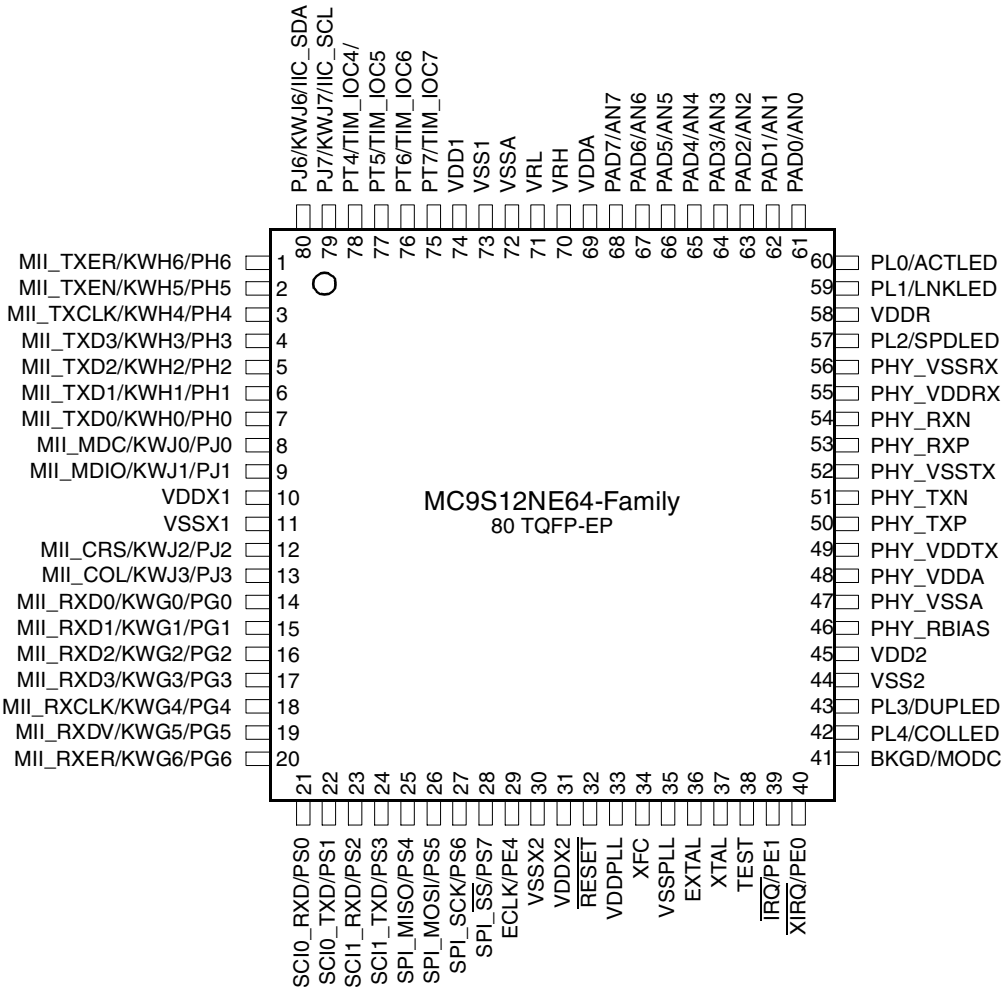


Figure 4. Pinout of MC9S12NE64 in 80-Pin TQFP-EP Package

Designing with the MC9S12NE64 and Adding an Ethernet Interface

The MC9S12NE64 is a single-chip Ethernet solution. Having built-in CPU, FLASH, RAM, MAC, and PHY reduces the cost of implementing an embedded device with Ethernet connectivity, because no active external components are required. The components required to enable the MC9S12NE64 Ethernet interface include the following:

- MC9S12NE64 MCU
- 25-MHz crystal
- 3.3-V power supply
- External resistor for PHY_RBIAS pin (see data sheet for value of R_{Bias})
- High-speed LAN magnetics isolation module
- RJ45 connector
- Miscellaneous capacitors and resistors
- Optional: PHY status LEDs (available in some integrated RJ45 connectors)
- Optional: Background debug (BDM) connector

Figure 5 is a schematic of a MC9S12NE64 minimum system circuit implementation using the MC9S12NE64 in an 80-pin package and the components described in this section. This circuit implementation shows an optional background debug connector (J1), and status LEDs (LED1 through LED5). The circuit also shows the required bias resistor (R5), high-speed LAN magnetics isolation module, and RJ45 Ethernet connector.

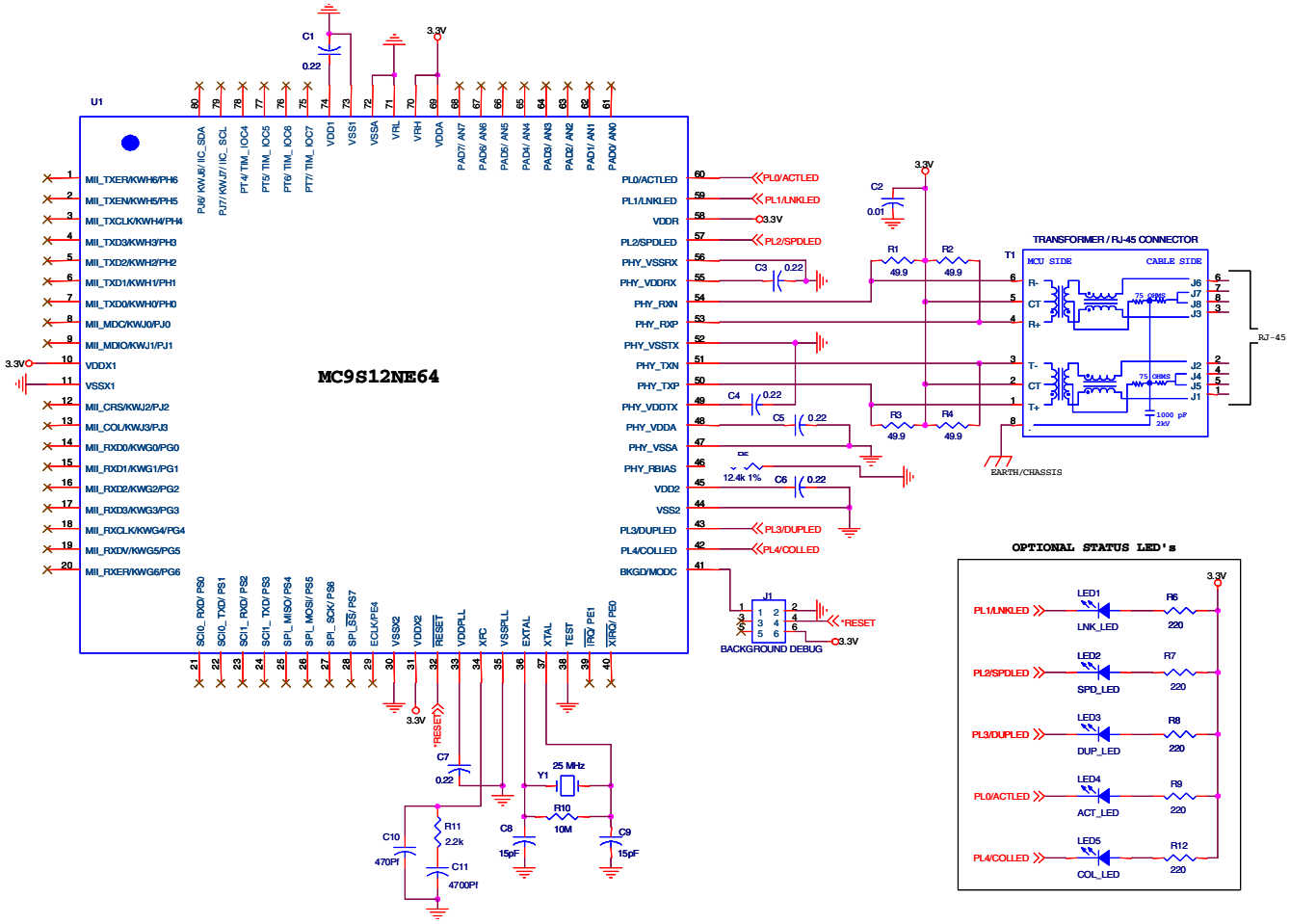


Figure 5. MC9S12NE64 Minimum System Circuit Implementation in the 80-Pin Package

In Figure 5, the MC9S12NE64 in the 80-pin package will operate in normal single-chip mode. Figure 5 shows that the design operates with the internal voltage regulator enabled. Using the internal voltage regulator is the recommended configuration for the MC9S12NE64. Figure 5 also illustrates the basic MC9S12NE64 power and clock input requirements, which are described in following sections.

To configure the MC9S12NE64 (in a 112-pin package) in normal single-chip mode, the MODC, MODB, and MODA pins may need to be pulled up or down. The operating mode of the MC9S12NE64, as well as other HCS12 MCUs, out of reset is determined by the states of MODC, MODB, and MODA during reset. MODC, MODB, and MODA can alternatively be configured by software. Table 2 describes the available modes on the 112-pin package.

Table 2. Mode Selection

BKGD = MODC	PE6 = MODB	PE5 = MODA	PP6 = ROMCTL	ROMON Bit	Mode Description
0	0	0	X	1	Special single chip, BDM allowed and active. BDM is allowed in all other modes, but a serial command is required to make BDM active.
0	0	1	0	1	Emulation expanded narrow, BDM allowed
			1	0	
0	1	0	X	0	Special test (expanded wide), BDM allowed
0	1	1	0	1	Emulation expanded wide, BDM allowed
			1	0	
1	0	0	X	1	Normal single chip, BDM allowed
1	0	1	0	0	Normal expanded narrow, BDM allowed
			1	1	
1	1	0	X	1	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	0	0	Normal expanded wide, BDM allowed
			1	1	

For details about modes, refer to the MC9S12NE64 device user guide.

Connecting a Power Supply to the MC9S12NE64

Using the internal voltage regulator can simplify power supply requirements for the design because (with the internal voltage regulator enabled) only a 3.3-V power supply that can handle the current load of the MC9S12NE64 is required. The power supply must be connected to VDDX1, VDDX2, and VDDR.

The internal voltage regulator is a five-stage regulator that provides 2.5 V to the MC9S12NE64, including:

- CPU
- PLL
- PHY analog
- PHY transmitter
- PHY receiver

Alternatively, depending on the embedded design requirements, the MC9S12NE64 can be set up with the internal voltage regulator disabled, which would require a 2.5-V external power supply for the logic plus a 3.3-V supply for the PHY I/O. This application note describes MC9S12NE64 configuration with the internal 2.5-V voltage regulator enabled. For configurations with the internal voltage regulator is disabled, see the MC9S12NE64 data sheet for special circuitry requirements. Disabling the voltage regulator is not recommended.

Connecting a Crystal to the MC9S12NE64

For basic operation of the MC9S12NE64 Ethernet controller, a 25-MHz crystal input with a tolerance of 25 ppm is required per IEEE 802.3 specification. The 25-MHz crystal input is required to provide the clock input to the integrated PHY for basic operation at 10 Mbps and/or 100 Mbps. The crystal must connect to the MC9S12NE64 in a Pierce configuration by the XTAL and EXTAL pins as shown on Table 5 with related cap and resistors.

In addition to providing a 25-MHz crystal input, to operate at 100 Mbps, the internal bus clock must be configured to 25 MHz. With the 25-MHz crystal, the CRG must be configured so the PLL is enabled and multiplies the crystal oscillator clock to achieve the internal bus clock 25 MHz operational setting.

For 10 Mbps, an internal bus clock setting of 2.5 MHz minimum is acceptable, but a 25-MHz crystal input is still required.

For details about the CRG and configuring the PLL, see Freescale Semiconductor document AN2692/D: *MC9S12NE64 Integrated Ethernet Controller*.

MC9S12NE64 PHY External Pins

Table 3 describes the pins related to the MC9S12NE64 PHY, their operation, and their circuitry design. The PHY pins in Table 3 serve several possible functions including power, signaling, component, and indicators for the EPHY.

Table 3. MC9S12NE64 PHY External Pins

Pin Function	Pin Label(s)	Pin Overview	Description
Power	PHY_VDDA, PHY_VSSA	Power supply pins for EPHY analog power	This 2.5-V supply is derived from the internal voltage regulator. No static load is allowed on these pins. The internal voltage regulator is turned off if VDDR is tied to ground.
	PHY_VDDRX, PHY_VSSRX	Power supply pins for EPHY receiver power	
	PHY_VDDTX, PHY_VSSTX	Power supply pins for EPHY transmitter	
Signaling	PHY_TXP	EPHY twisted pair output +	Ethernet twisted pair output pin. These pins are Hi-Z out of reset.
	PHY_TXN	EPHY twisted pair output –	
	PHY_RXP	EPHY twisted pair input +	
	PHY_RXN	EPHY twisted pair input –	
Circuit (EPHY bias pin)	PHY_RBIAS	EPHY bias control resistor	Connect an external bias resistor(1), (R5), between the PHY_RBIAS pin and analog ground. This resistor should be placed as near a possible to the MCU pin. Stray capacitance must be less than 10 pF (greater than 50 pF may cause instability). No high-speed signals should go in the region of the bias resistor.
Indicator	COLLED	Collision LED	Flashes in half-duplex mode when a collision occurs on the network.
	DUPLED	Duplex LED	Indicates the duplex of the link, which can be full-duplex or half-duplex.
	SPDLED	Speed LED	Indicates the speed of a link, which can be 10 Mbps or 100 Mbps.
	LNKLED	Link LED	Indicates whether a link is established with another network device.
	ACTLED	Activity LED	Flashes when data is received by the device.

NOTES:
1. See the MC9S12NE64 data sheet for the value of the bias resistor

LED Indicator Pins

The power, signaling, and EPHY bias pins are required for basic operation of the EPHY; indicator pins (PL0:5) are optional. The EPHY can be configuring by software to drive indicator pins (PL0:5) automatically by setting the LEDEN bit of the EPHY EPHYCTL0 register. When LEDEN = 1, PL0:5 pins are dedicated to the EPHY. Alternatively, the system can be designed such that user software drives LEDs on any port pin to show EPHY status. For instance, the user may desire to show only link status. In this case, the user can manually drive an LED with software to show link status (with LEDEN bit = 0), which would allow the other four pins to be used for other purposes.

MC9S12NE64 low-level Ethernet drivers are available to handle software-driven LEDs.

Adding an RJ45 Connector to the MC9S12NE64

Because the MC9S12NE64 has an integrated MAC and PHY, connecting an RJ45 Ethernet connector and transformer is easy. A high-speed LAN magnetics isolation module must be used between the MC9S12NE64 and the RJ45 Ethernet connector. This high-speed LAN magnetics isolation module can be discrete or integrated within a RJ45 Ethernet connector. Figure 6 shows the required circuitry configuration.

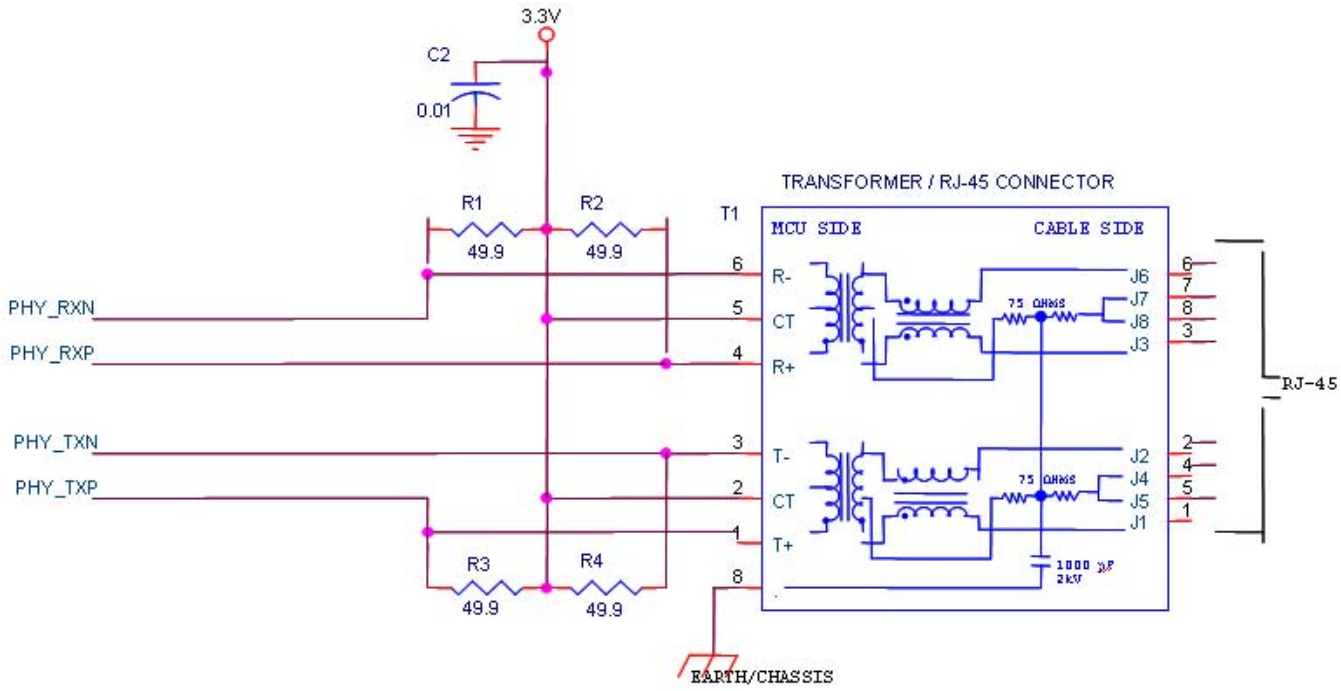


Figure 6. Ethernet Interface Circuitry

Table 4 describes the signal wiring for the MCU side.

Table 4. High-Speed LAN Magnetics Isolation Module Circuit Connections

High-Speed LAN Magnetics Isolation Module	MC9S12NE64 pins
TX CT	3.3 V
T+	PHY_TXP
T-	PHY_TXN
RX CT	3.3 V
R+	PHY_RXP
R-	PHY_RXN

PCB Design Recommendation

The section provides recommendations for PCB design and high-speed LAN magnetics isolation module selection.

General PCB Design Recommendations

The PCB layout must be designed to ensure proper operation of the voltage regulator and the MCU. The following recommendations are provided to ensure a robust PCB design:

- Every supply pair must be decoupled by a low-ESR (equivalent series resistance) ceramic capacitor connected as near as possible to the corresponding pins.
- Central point of the ground star should be the VSSX1 and VSSX2 pins.
- Use low-ohmic, low-inductance connections with VSS1, VSS2, VSSX1, and VSSX2 pins.
- VSSPLL must be directly connected to VSSX.
- Keep traces of VSSPLL, EXTAL, and XTAL as short as possible and their occupied board area as small as possible.

Ethernet PCB Design Recommendations

When designing a PCB that uses the MC9S12NE64 Ethernet module, several design considerations must be made to ensure that Ethernet operation conforms to the IEEE 802.3 physical interface specification. Use the following recommendations for PCB design between the high-speed LAN magnetics isolation module and:

- MC9S12NE64 EPHY external pins (most critical)
- RJ45 connector

Ethernet PCB design recommendations:

- The distance between the magnetic module and the RJ-45 jack is the most critical and must always be as short as possible (must be less than one inch).
- Never use 90° traces. Use 45° angles or radius curves in traces.
- Trace widths of 0.010” are recommended. Wider is better. Trace widths should not vary.
- Route differential Tx and Rx pairs near together (max 0.010” separation with 0.010” traces).
- Trace lengths must always be as short as possible (must be less than one inch).
- Make trace lengths as equal as possible.
- Keep TX and RX differential pairs routes separated (at least 0.020” separation). Better to separate with a ground plane.
- Avoid routing Tx and Rx traces over or under a plane. Areas under the Tx and Rx traces should be open, See Figures 9, 10, 11, 17 and 18.
- Use precision components in the line termination circuitry with 1% tolerance.
- Ensure that the power supply is rated for a load of 300 mA minimum.
- Avoid vias and layer changes.

In addition, all termination resistors should be near to the driving source. The MCU is the driving source for PHY_TXP and PHY_TXN pins. The high-speed LAN magnetics isolation module is the driving source for PHY_RXP and PHY_RXN pins.

High-Speed LAN Magnetics Isolation Module Requirements

The MC9S12NE64 requires a 1:1 ratio transformer for the high-speed LAN magnetics isolation module for both the receive and the transmit signals. The basic high-speed LAN magnetics isolation module specification requirements are provided in Table 5. High-speed LAN magnetics isolation modules that meet these requirements are available from a variety of manufacturers.

Table 5. High-Speed LAN Magnetics Isolation Module Specification Requirements

Parameter	Value	Units	Test Condition
Tx/Rx turns ratio	1:1 CT / 1:1	—	—
Inductance	350	mH (min)	—
Insertion loss	1.1	dB (max)	1 to 100 MHz
Return loss	–18	dB (min)	1 to 30 MHz
	–14	dB (min)	30 to 60 MHz
	–12	dB (min)	60 to 80 MHz
Differential to common mode rejection	–40	dB (min)	1 to 60 MHz
	–30	dB (min)	60 to 100 MHz
Transformer	1500	V	—

The MC9S12NE64 can be used with high-speed LAN magnetics isolation modules that are either discrete or integrated into a RJ45 connector. Some of these integrated connectors have built-in LEDs as well. For the MC9S12NE64, an RJ45 connector with an integrated high-speed LAN magnetics isolation module is recommended because it reduces component count and simplifies PCB layout.

Because the MC9S12NE64 does not implement Auto-MDIX, an Auto-MDIX capable high-speed LAN magnetics isolation module is not required. A high-speed LAN magnetics isolation module with improved return loss characteristics is recommended to avoid Ethernet return loss issues.

Table 6 provides discrete and integrated high-speed LAN magnetics isolation modules that have been found in testing to satisfy the requirements necessary to establish an IEEE-compliant Ethernet interface with the MC9S12NE64. Other models can be used as long as the high-speed LAN magnetics isolation module specifications satisfy the requirements.

Although specific hardware is discussed in this section, Freescale Semiconductor does not recommend or endorse any particular product or vendor. This data is provided only to describe the specification requirements.

Table 6. Discrete High-Speed LAN Magnetics Isolation Module

Type	Manufacturer	Model
Discrete	Pulse	H1102
	Midcom	000-6241-37R
Integrated	Pulse	J10-0026
	Midcom	JFM25xxx-0510, JFM24xxx-1010
	Bel Fuse	0810-1X1T-06
	Halo	HFJ11-2450E

Design Examples

This section shows two MC9S12NE64 design examples of Ethernet interface implementations with the MC9S12NE64 in a minimum system. These minimum system examples are provided only to demonstrate recommended MC9S12NE64 PCB design. These MC9S12NE64 design examples are test boards, and they are not available for purchase.

The first design shows a minimum system using the MC9S12NE64 in a 112-pin package. The second design is an example of a system using the 80-pin MC9S12NE64 with a very compact PCB footprint.

Schematics and all artwork layer views for both designs will be shown in this section. Both designs are implemented on 4-layer PCBs to provide better heat dissipation. Both boards are minimum system designs that use the internal voltage regulator.

MC9S12NE64 112-Pin Package Design Example

A photo of the MC9S12NE64 112-pin package design example is provided in Figure 7. The PCB, which is approximately 6.3 cm x 6.3 cm, was designed using the recommendations discussed in the PCB Design Recommendation section. This design and PCB layout are discussed in detail in following sections.

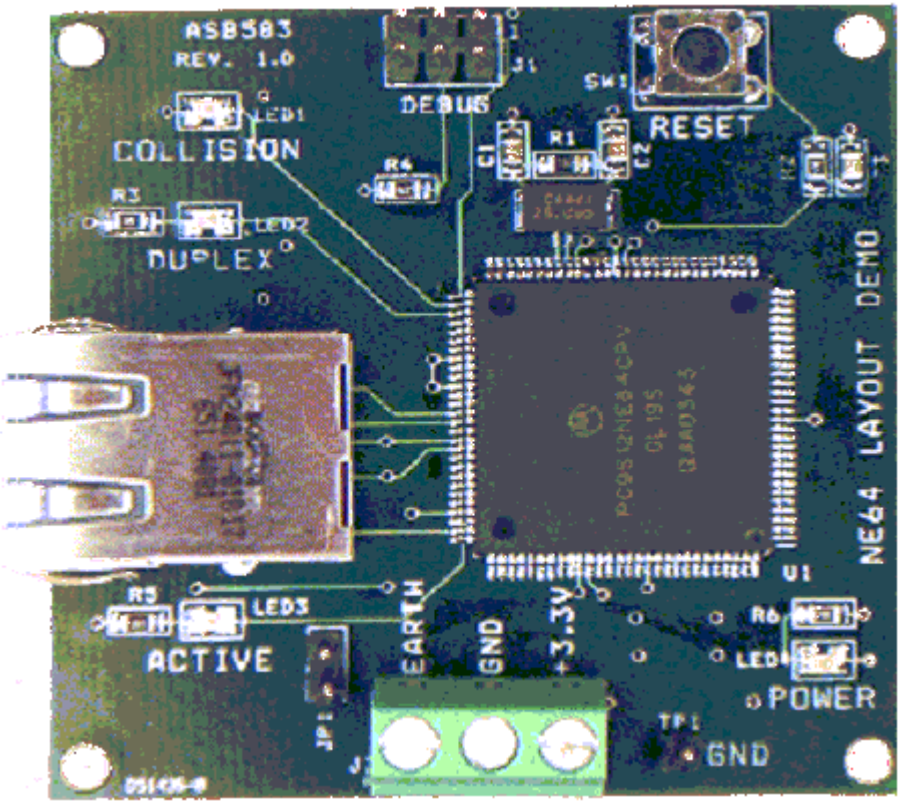


Figure 7. 112-Pin Package Design Example

A schematic of this design example is provided in Figure 8.

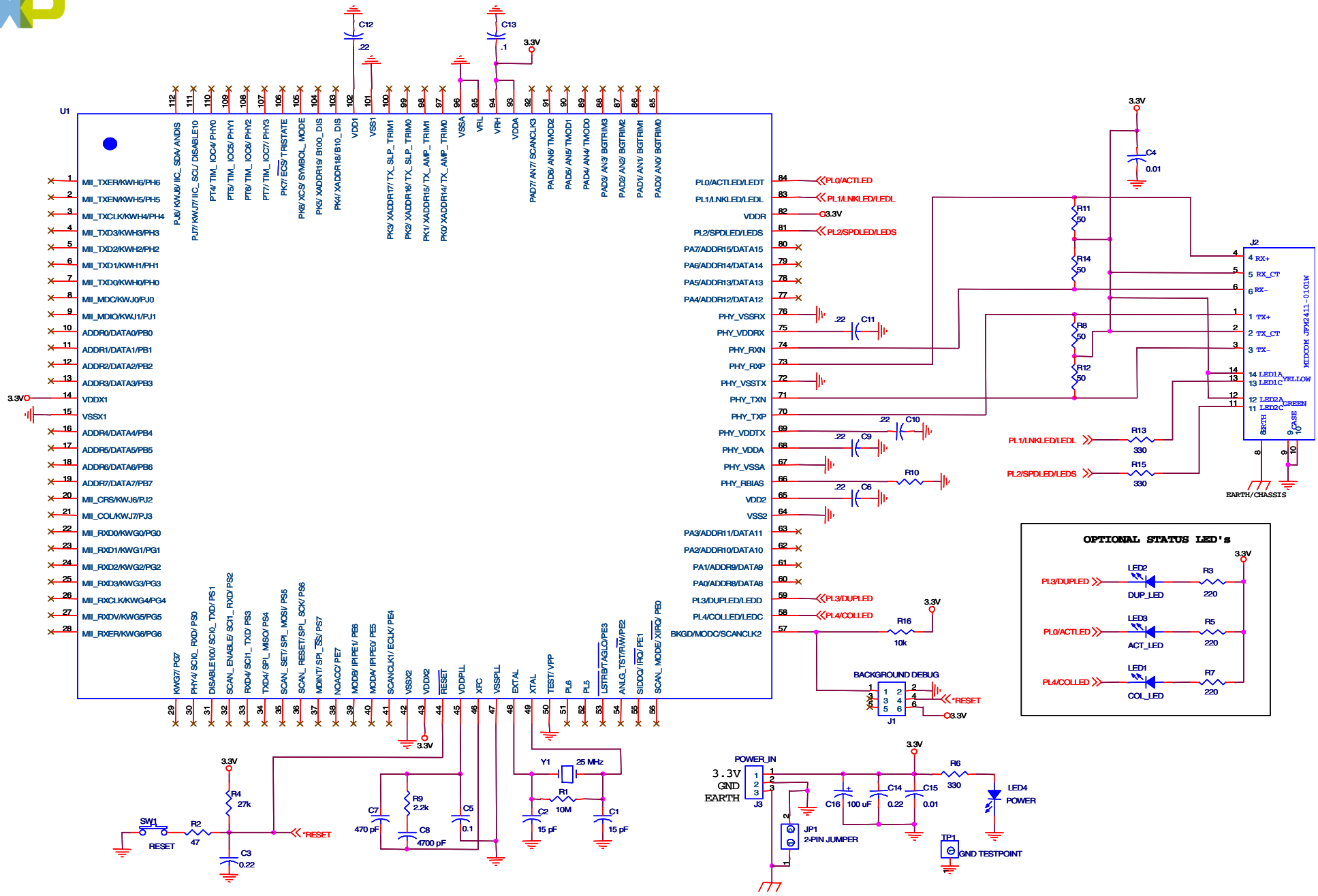


Figure 8. Minimum 112-Pin Package System Schematic

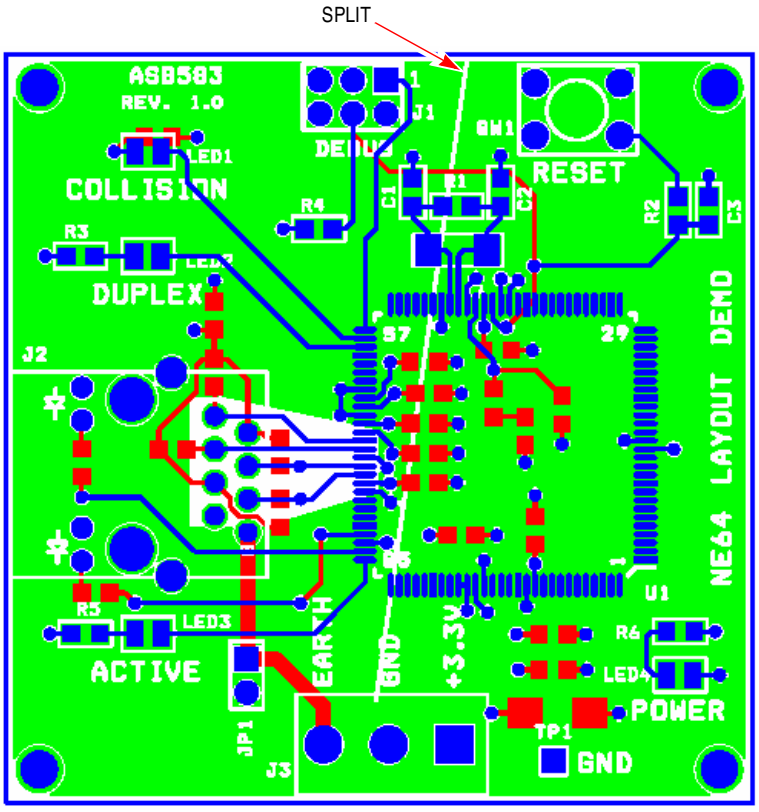


Figure 9. Minimum 112-pin Package Artwork All Layers

Ground planes and how grounds are tied together affect noise immunity. To maximize noise immunity, it is important to get a good ground plane under the MCU. It is also a good practice to have the ground plane under the crystal components. Note, on the layout, Figure 10, there is a white area to the left of the MCU. That area is directly under the Ethernet transmit and receive traces from the MCU to the high-speed LAN magnetics isolation module. That area under those traces must be devoid of any ground plane to reduce capacitance.

As shown in Figure 9 and Figure 10, there is a split in the ground plane. It starts just to the right of the top center of the PC board and continues down to just above the center of connector J3. The center pin of J3 is the system ground connection. This split in the ground plane forces the system's ground currents to flow to a common point, the ground connection for the PC board. This technique helps increase noise immunity in the system.

As shown in Figure 11, attention was given to the length of the Ethernet transmit and receive pairs that go between the MCU and the Ethernet integrated magnetics/RJ45 connector. They were made as short as possible for this mechanical layout. The PC board tracks in the Ethernet portion of this design are 0.010" and the maximum conductor length is just under 0.5". The PC board traces bend on 45° angles, with no 90° angles. Figure 11 demonstrates these design practices.

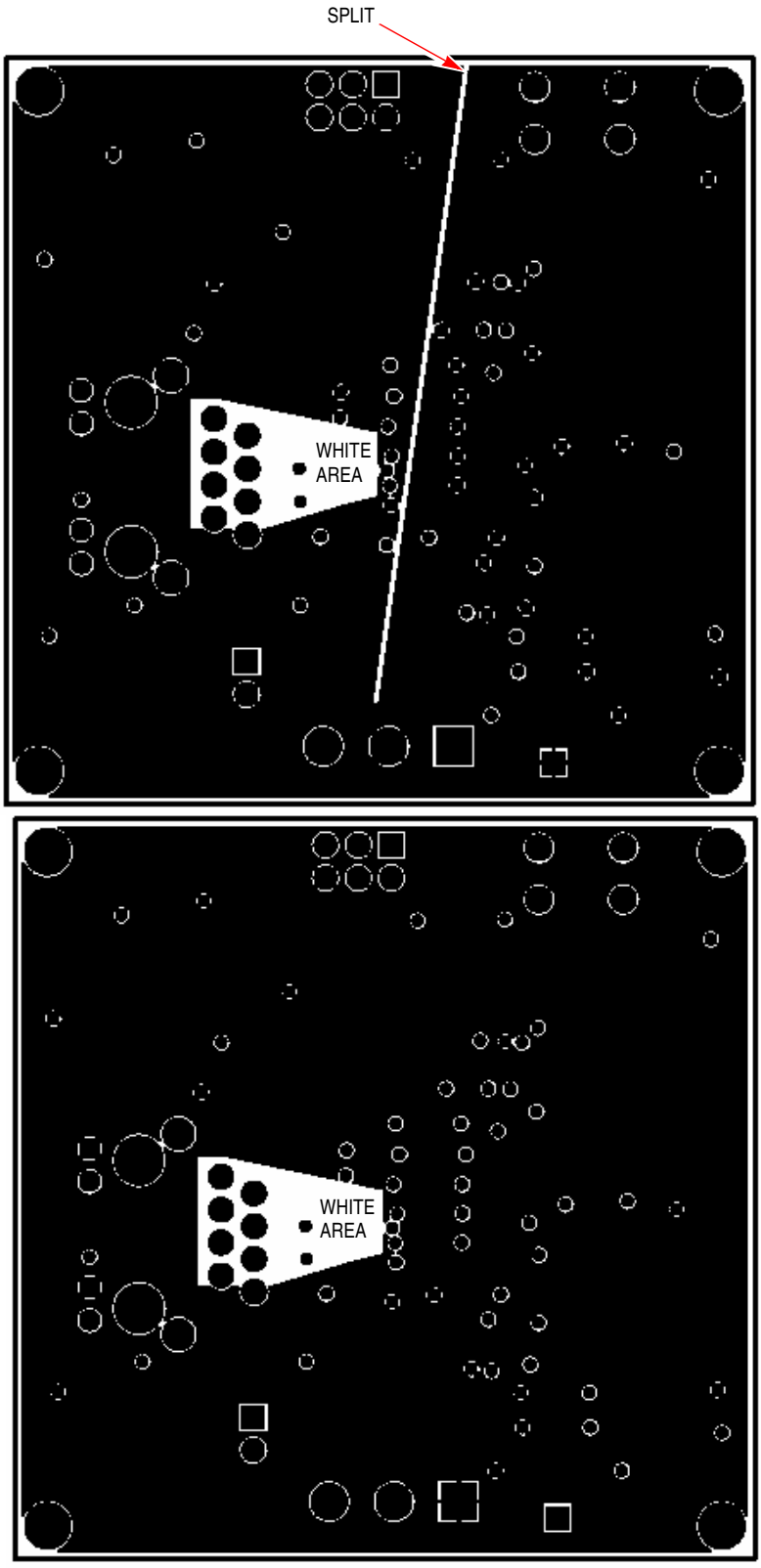


Figure 10. Minimum 112-Pin Package Artwork

Top Layer

Bottom Layer

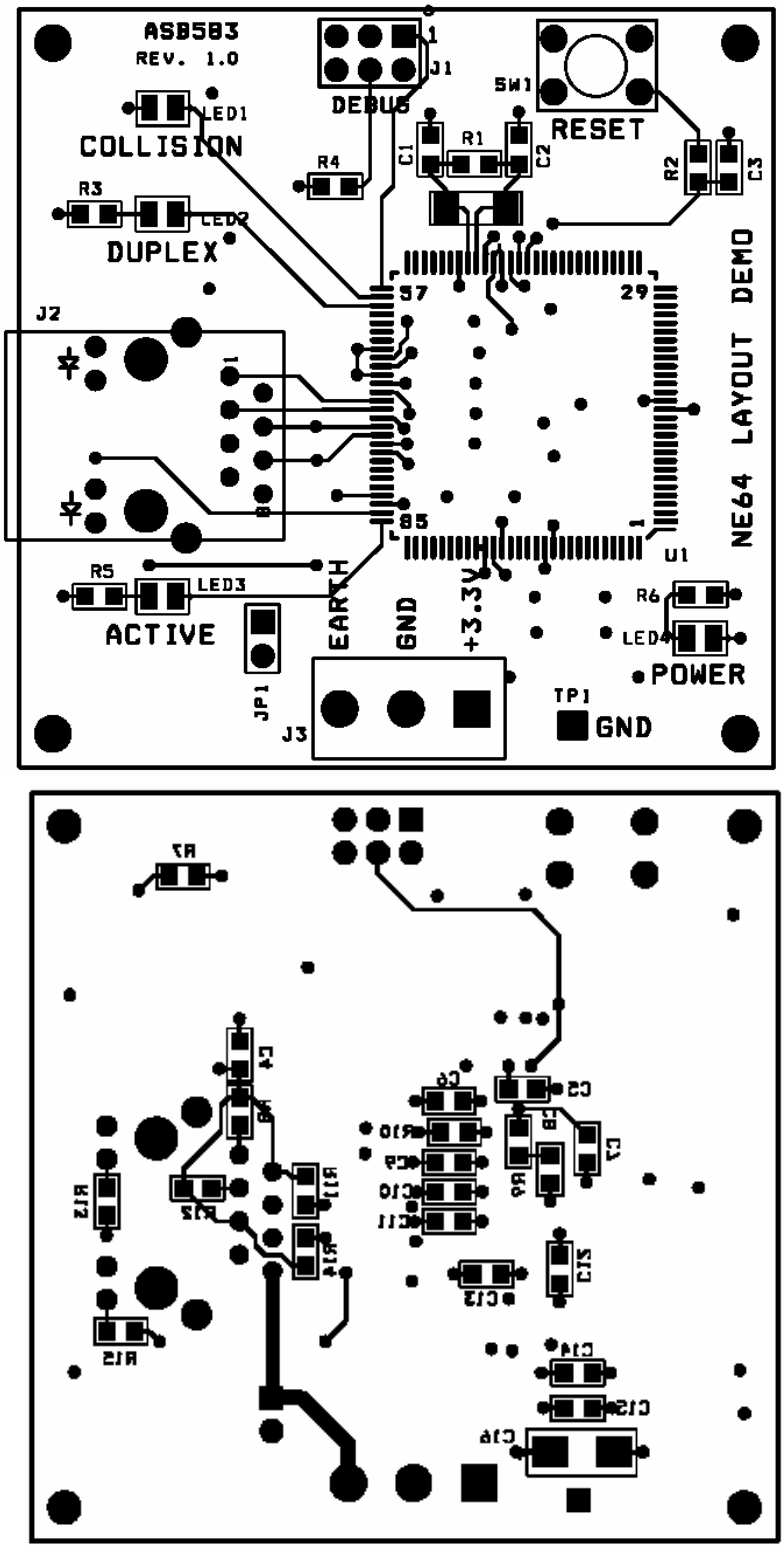


Figure 11. Minimum 112-pin Package Artwork

As with all designs, place the crystal and its associated components as near to their MCU pins as possible and use minimum trace lengths. This is also true with the XFC connections (PLL components).

There are a number of power supply decoupling capacitors necessary to decouple the MCU and its various internal power supplies. These pins are VDD1, VDD2, VDDA, VDDPLL, PHY_VDDRX, and PHY_VDDTX. These capacitors should be good quality, low ESR type ceramic components.

MC9S12NE64 80-Pin Package Design Example

The second design example uses the 80-pin MC9S12NE64 and uses the PCB design recommendations discussed for the 112-pin design example. A photo is provided in Figure 12.

This example demonstrates that the MC9S12NE64 can implement Ethernet capability in a very small package footprint. This 80-pin design example resides on a very small 1” x 1.5” PCB and shows a complete Ethernet PCB system implementation. The design example uses the PCB recommendations described in this application note. A schematic of this design example is provided in Figure 13.

Figure 12. 80-Pin Package Design Example

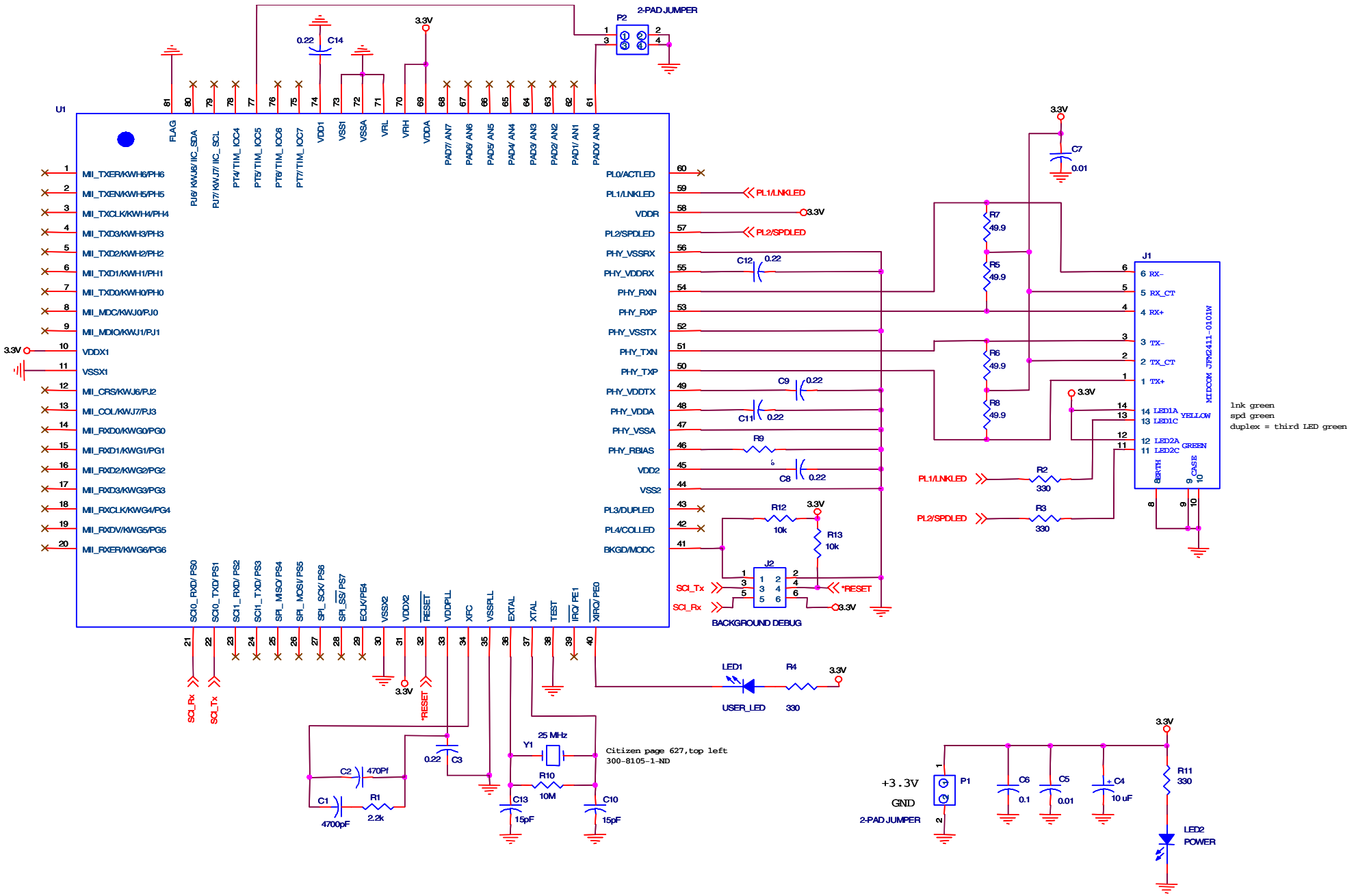


Figure 13. 80-Pin Package System Schematic

Figure 14 provides all artwork for the MC9S12NE64 80-pin package design example.

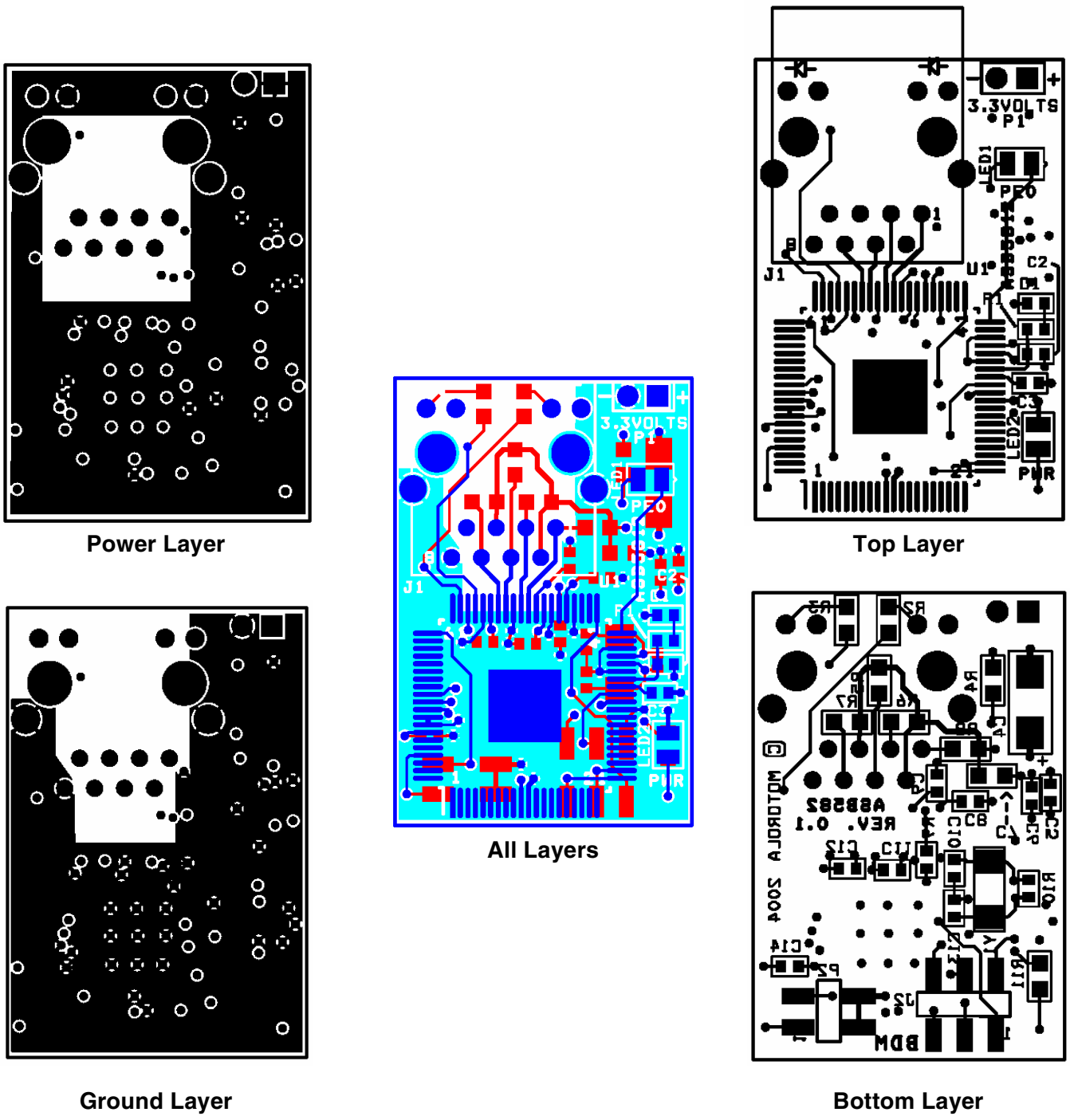


Figure 14. 80-Pin Package Artwork

Exposed Flag

Because the 80-pin TQFP-EP package has an exposed flag, which provides additional heat dissipation for the MC9S12NE64, the artwork shows special PCB design to accommodate the exposed flag. There are two ways to accommodate the flag:

- Have a hatched pattern in the solder mask
- Use small copper areas under the flag

The concept is to have about 50% of the flag soldered to the PC board.

Conclusion

The MC9S12NE64 is a highly integrated, flexible and easy-to-use Ethernet-capable microcontroller with an integrated MAC and PHY. No external active components are needed to implement an Ethernet interface. The schematics in this document illustrate the simplicity of implementing such a system.

Interfacing the device to an Ethernet trunk is accomplished with the addition of only four resistors, a decoupling capacitor and an integrated transformer/RJ45 connector. PCB layout around the high-speed LAN magnetics isolation module is critical, as with any high frequency design. Using techniques discussed in this document makes that task easier.

NOTE

With the exception of mask set errata documents, if any other Freescale Semiconductor document contains information that conflicts with the information in the device user guide, the user guide should be considered to have the most current and correct data.

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