

# Interfacing SDRAM Devices to the PowerQUICC™ MPC8280 at 100 MHz

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This application note discusses the interface of SDRAM memory devices using the internal MPC8280 SDRAM controller operating at a bus frequency of 100 MHz. We examine solutions for example load and fanout designs to give the designer practical techniques for ensuring that the timing parameters of the SDRAM manufacturer are satisfied.

The MPC8280 device is similar to the earlier MPC826x devices except that it operates at higher clock frequencies. The main differences between the MPC8280 family devices and the earlier devices are as follows:

- System core microprocessor supporting frequencies of 150–450 MHz
- CPM has 32-Kbytes of dual-port RAM instead of the 24-Kbytes in the original MPC8260
- Inverse multiplexing for ATM capabilities (IMA)
- Transmission Convergence layer (TC)
- Reduced core supply voltage of 1.425–1.575 V
- Bus Frequency of 100 MHz.

The increased bus frequency of 100 MHz leads to restrictions on the interface bus due to the shorter cycle time. These restrictions require the use of faster memory devices with reduced setup and hold time requirements.

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# 1 Bus Interface Timing Specifications

Figure 1 shows the interaction of several 60x bus interface signals. Table 1 and Table 2 list the timing parameters for the 60x bus interface operating at 100 MHz.

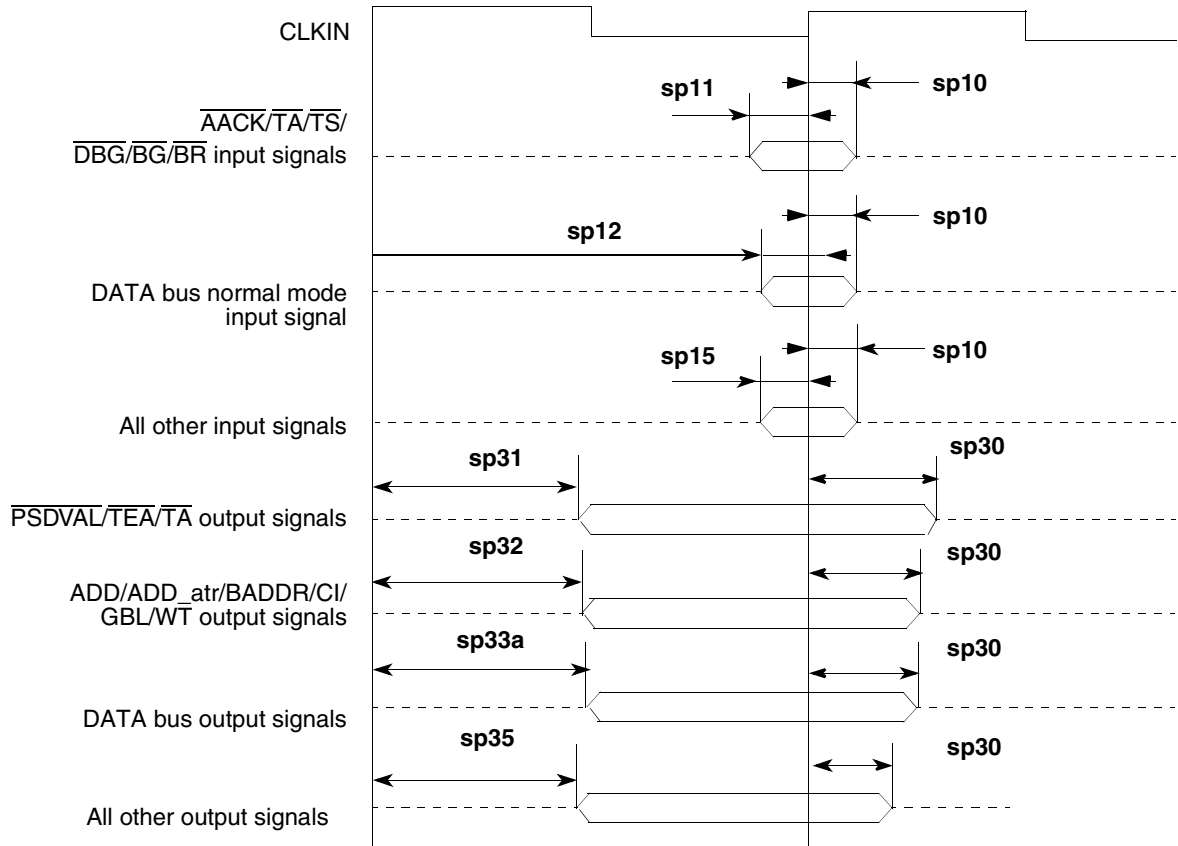


Figure 1. 60x Bus Signals

Table 1. AC Characteristics for SIU Inputs <sup>1</sup>

Spec_num (Max/Min)	Characteristics	Maximum Delay (ns)	Minimum Delay (ns)
		100 MHz	100 MHz
sp11/sp10	$\overline{AACK}/\overline{ARTRY}/\overline{TA}/\overline{TS}/\overline{DBG}/\overline{BG}/\overline{BR}$	3.5	0.5
sp12/sp10	Data bus in normal mode	3.5	0.5
sp13/sp10	Data bus in ECC and PARITY modes	3.5	0.5
sp13a/sp10	Pipeline mode—Data bus in ECC and PARITY modes	2.5	0.5
sp14/sp10	DP pins	3.5	0.5
sp14a/sp10	Pipeline mode—DP pins	2.5	0.5
sp15/sp10	All other pins	3.5	0.5

<sup>1</sup> Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

**Table 2. AC Characteristics for SIU Outputs <sup>1</sup>**

Spec_num (Max/Min)	Characteristics	Maximum Delay (ns)	Minimum Delay (ns)
		100 MHz	100 MHz
sp31/sp30	$\overline{\text{PSDVAL}}/\overline{\text{TEA}}/\overline{\text{TA}}$	5.5	1
sp32/sp30	ADD/ADD_atr/DADDR/CI/GBL/WT	5.5	1
sp33a/sp30	Data bus <sup>2</sup>	5.5	0.7
sp33b/sp30	DP	6.5	1
sp34/sp30	memc signals/ALE	5.5	1
sp35/sp30	All other signals	5.5	1
sp35a/sp30	AP	7	1

<sup>1</sup> Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

<sup>2</sup> To achieve 1 ns of hold time at 66.67/83.33/100 MHz, a minimum loading of 20 pF is required.

Activating the data pipeline mode by setting BRx[DR] in the memory controller improves the AC timing because data beat accesses to memory controller address spaces are delayed by one cycle. With this mode enabled, the output timing for the data bus and DP pins is the same as the timing for a normal bus.

## 2 Interface to SDRAM at 100 MHz

The internal MPC8280 SDRAM controller provides a glueless interface to standard SDRAM devices and DIMM modules. The electrical specification for standard SDRAM devices shows the following timings:

- For inputs, the setup time for address, data,  $\overline{\text{CS}}$ ,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{DQM}}$  is 1.5 ns minimum.
- Hold time for all signals is 0.8 ns.
- For outputs, the data output hold time is a minimum of 3 ns for normal loads and 1.8 ns for low loads.

### 2.1 MPC8280 Writing to SDRAM

At a bus frequency of 100 MHz, the cycle time is 10 ns. When the MPC8280 writes to the SDRAM, the address and address attributes are valid at a maximum 5.5 ns (sp32/sp30) after a rising clock edge. The SDRAM requires a minimum 1.5 ns of setup time before the next rising edge. Therefore, this allows  $10 - 5.5 - 1.5 = 3$  ns for clock skew and track delay in the interface. The MPC8280 outputs the data at a maximum of 5.5 ns (sp33a/sp30) after a rising clock edge, and the SDRAM requires a minimum setup time of only 1.5 ns for data. This allows  $10 - 5.5 - 1.5 = 3$  ns for clock skew and track delay. The MPC8280 maintains the data for 0.7 ns after the clock edge or for 1 ns after the clock edge if the load is greater than 20 pF. The SDRAM device requires a hold time of 0.8 ns, so if the load on the data bus is greater than 20 pF, there is a margin of 0.2 ns. The MPC8280 control signals are held for 1 ns. The SDRAM device requires only 0.8 ns, so there is a margin of 0.2 ns.

## 2.2 MPC8280 Reading from SDRAM

During a read cycle from the MPC8280 to the SDRAM, the address and address attributes are valid at a maximum of 5.5 ns (sp32/sp30) after a rising clock edge. The SDRAM requires a minimum of 1.5 ns of setup time before the next rising edge. This allows  $10 - 5.5 - 1.5 = 3$  ns for clock skew and track delay. The SDRAM outputs the required data at a maximum of 5.4 ns after the rising clock edge for a PC133 SDRAM with a  $\overline{\text{CAS}}$  latency of 3. The MPC8280 requires 3.5 ns (sp12/sp10) for setup time. Therefore, this leaves  $10 - 5.4 - 3.5 = 1.1$  ns for clock skew and track delay. The SDRAM maintains the data for 3 ns for normal load but only 1.8 ns for low loads. The MPC8280 requires a hold time of only 0.5 ns. Therefore even with a low load there is a margin of  $1.8 - 0.5 = 1.3$  ns. The MPC8280 control signals are held for 1 ns. The SDRAM device requires only 0.8 ns. Therefore, there is a margin of 0.2 ns for track delay and clock skew.

## 2.3 Restriction on the Interface to SDRAM

The preceding timing analysis shows that for an ideal situation with zero clock skew between the MPC8280 and the SDRAM, the timing requirements are all met if the load on the signals is greater than 20pF. The margin is small at 0.2 ns but assumes a PCB track delay of approx 0.1 ns per inch, allowing for for track lengths of up to two inches (5 cm). In a real design, clock skew is present between the MPC8280 and the SDRAM, which negatively affects the margins. However, there are longer track lengths, which have a positive effect by increasing the signal delay.

For a system with a clock driver with a 0.1 ns skew between the SDRAM clock and the MPC8280 clock and an equal track length between the clock driver and the MPC8280 and the clock driver and the SDRAM, there is still a margin of 0.1 ns in the interface. The longer tracks between the MPC8280 and the SDRAM add more margin to both the read and write cycles. For details on implementing clock skew and track delay into a design, refer to the Freescale white paper entitled *Timing Considerations when Interfacing the PowerQUICC II to SDRAM* (MPC826XSDRAMWP).

## 3 Capacitive Loading

Because the MPC8280 can have a glueless interface to SDRAM at 100 MHz if the loading on the SDRAM interface signals is greater than 20pF, it is important to consider the total load on each signal:

- Address, data, and DQM. These signals are shared between the SDRAM and flash memory, so the load of both devices must be included. The flash memory may not use all the address, data, and DQM signals
- $\overline{\text{RAS}}$ . This signal is multiplexed with the output enable signal for flash memory, so the load of both types of device must be added.
- $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ . These signals are used only by the SDRAM devices, so only the load of these devices must be considered.
- $\overline{\text{CS}}$ . This signal can be unique for each device, so additional capacitive load or buffer delay may be required on this signal

## 4 Load analysis Example

To achieve the 1 ns hold time specification on the MPC8280, it must have a minimum of a 20 pF load on the interface signals. If we consider a typical SDRAM DIMM module of 32 Mbyte, 64 Mbyte, or 128 Mbyte, the published capacitive loading for this module is as follows:

- A[0:11], control signals MIN 10pF
- $\overline{DQ}$  MIN 8pF
- $\overline{CS}$  MIN 5pF
- $\overline{DQM}$  MIN 10pF

A typical DIMM socket has a capacitive load of around 2 pF. PCB trace capacitance is typically around 1.2 pF per inch with a transmission line propagation delay of 0.1 ns per inch. Therefore, with this module (apart from the  $\overline{CS}$  line), there is a minimum load of 10 pF before any trace capacitance is included. Large boards can have PCB traces of 10–12 inches (25–30 cm), which can add at least another 10 pF load to each signal, thus ensuring that the 20 pF load requirement is met.

## 5 Fanout Buffer Example

Figure 2 shows an example of an SDRAM configuration consisting of a 100 MHz oscillator input into a fanout buffer that fans the clock into four discrete SDRAM devices as well as the MPC8280.

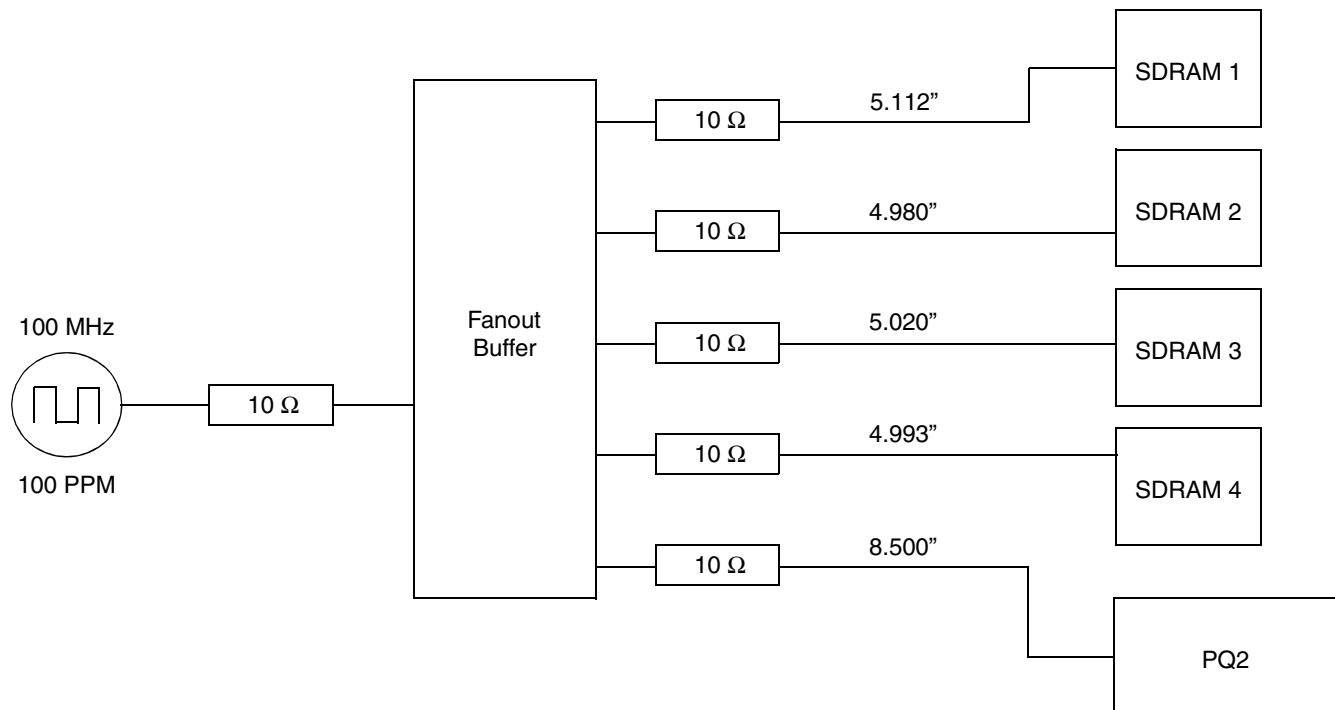


Figure 2. Example Fanout Buffer

## Fanout Buffer Example

This example uses a Pericom PI49FCT32805Q fanout buffer and Micron MT48LC32M16A2 SDRAMs. The Pericom data sheet states that skew between outputs is 270 ps. Here, the maximum trace length from the fanout buffer to a device is 5.116 inches, and minimum trace length is 4.014 inches (1.102 inches difference). We calculate propagation delays based upon the estimate that on an FR4 PCB the flight time is a minimum 140 ps per inch and maximum of 192 ps per inch. See Table 3.

**Table 3. Trace Lengths and Propagation Delays**

	Length (Inches)	Min (ns)	Max (ns)
SDRAM 1	5.112	0.716	0.982
SDRAM 2	4.980	0.697	0.956
SDRAM 3	5.020	0.703	0.964
SDRAM 4	4.993	0.699	0.959
PowerQUICC II	8.500	1.190	1.632

Using the SDRAM and fanout buffer data sheets, timing analysis for setting up SDRAM for a write produces the results shown in Table 4 (in nanoseconds).

**Table 4. SDRAM Write Setup**

9.990	Clock period (100 MHz + 100 ppm)
(0.150)	Jitter
(0.270)	Fanout buffer clock skew
(5.500)	PQ2 max clock to out
(1.500)	SDRAM setup
0.697	Min trace propagation CLK to SDRAM
(1.632)	Max trace propagation CLK to PQ2
<b>1.635</b>	

Assuming 20pF of loading on the data bus, we achieve 1 ns of MPC8280 hold (sp30 in the MPC8280 hardware specification). The SDRAM data sheet specifies SDRAM hold at 0.8 ns and SDRAM max clock-to-out at 5.4 ns. See Table 5.

**Table 5. SDRAM Write Hold**

1.000	PQ2 min output hold (sp30)
(0.270)	Fanout buffer clock skew
(0.982)	Max trace propagation CLK to SDRAM
1.190	Min trace propagation CLK to PQ2
(0.800)	SDRAM hold
<b>0.138</b>	

For an SDRAM read, Table 6 and Table 7 show the resulting margins for SDRAM setup and hold.

**Table 6. SDRAM Read Setup**

9.990	Clock period (100 MHz + 100 ppm)
(0.150)	Jitter
(0.270)	Fanout buffer clock skew
(5.400)	SDRAM max clock to out
(3.500)	PQ2 setup
(0.982)	Max trace propagation CLK to SDRAM
1.190	Min trace propagation CLK to PQ2
<b>0.878</b>	

**Table 7. SDRAM Read Hold**

1.800	SDRAM min clock-to-out
(0.270)	Fanout buffer clock skew
0.956	Min trace propagation CLK to SDRAM
(1.632)	Max trace propagation CLK to PQ2
(0.800)	PQ2 hold
<b>0.054</b>	

This example shows a positive timing margin for both setup and hold in all test cases. Additionally, depending upon the amount of detail desired, we can also account for slicing skew (that is, ViH and ViL differences on the SDRAM and MPC8280). To meet SDRAM write hold timing requirements, the trace to the processor must be approximately two inches longer than the average trace length to the SDRAM devices. We can estimate the maximum possible trace length for the preceding example in order to meet timing requirements. A clock length of 8.5 inches to SDRAM gives us the propagation delays and timing shown in Table 8 through Table 12.

**Table 8. Maximum Trace Lengths and Propagation Delays**

	Length (Inches)	Min (ns)	Max (ns)
SDRAM 1	8.500	1.190	1.632
SDRAM 2	8.500	1.190	1.632
SDRAM 3	8.500	1.190	1.632
SDRAM 4	8.500	1.190	1.632
PQ2	12.302	1.722	2.362

**Table 9. Maximum Trace Write Setup**

9.990	Clock period (100 MHz + 100 ppm)
(0.150)	Jitter
(0.270)	Fanout buffer clock skew
(5.500)	PQ2 max clock to out
(1.500)	SDRAM setup
1.190	Min trace propagation CLK to SDRAM
(2.362)	Max trace propagation CLK to PQ2
<b>1.398</b>	

**Table 10. Maximum Trace Write Hold**

1.000	PQ2 min output hold (sp30)
(0.270)	Fanout buffer clock skew
(1.632)	Max trace propagation CLK to SDRAM
1.722	Min trace propagation CLK to PQ2
(0.800)	SDRAM hold
<b>0.020</b>	

**Table 11. Maximum Trace Read Setup**

9.990	Clock period (100 MHz + 100 ppm)
(0.150)	Jitter
(0.270)	Fanout buffer clock skew
(5.400)	SDRAM max clock to out
(3.500)	PQ2 setup
(1.632)	Max trace propagation CLK to SDRAM
1.722	Min trace propagation CLK to PQ2
<b>0.760</b>	

**Table 12. Maximum Trace Read Hold**

1.800	SDRAM min clock-to-out
(0.270)	Fanout buffer clock skew
1.632	Min trace propagation CLK to SDRAM
(2.362)	Max trace propagation CLK to PQ2
(0.800)	PQ2 hold
<b>0.000</b>	



As this example shows, it is the hold time that gives the most difficulty. Although 8.5 inches is the maximum length with which we can easily meet timing, longer lengths may be possible with attention to buffer skew, jitter, clock accuracy, and flight times through the actual laid out/routed PCB.

## 6 Further Reading

The following documents are all available at the Freescale web site listed on the back cover of this document:

- *MPC8260 PowerQUICC™ II Family Reference Manual (MPC8260UM)*
- *MPC8260 PowerQUICC™ II Design Checklist (AN2290)*
- *MPC8260 SDRAM Timing Diagram (AN2178)*
- *MPC826x Timing When Interfacing PQII to SDRAM (MPC826XSDRAMWP)*
- *MPC8260 PowerQUICC™ II Family Device Errata (MPC8260CE)*
- *MPC8260A HiP4 Family Hardware Specifications (MPC8260AEC)*

## 7 Conclusion

The analysis in this document demonstrates that with careful design practice the MPC8280 has a glueless interface to standard SDRAM memory devices operating with bus frequencies up to and including 100 MHz. The main design consideration is to ensure that the MPC8280 data bus is loaded with a minimum of 20 pF on all signals. With this loading, the interface meets the min/max specification for both the MPC8280 and typical SDRAM devices, with an additional timing margin for clock skew and track delay.

## 8 Revision History

Table 13 provides a revision history for this application note.

**Table 13. Document Revision History**

Rev. Number	Date	Substantive Change(s)
0	2/2004	Initial release.
1	12/2006	<ul style="list-style-type: none"> <li>• Updated Figure 1.</li> <li>• Updated and extended the fanout buffer example, adding Tables 3 through 12.</li> </ul>





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