Freescale Semiconductor
Application Note

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MPC82xx PowerQUICC™ II Reset Sources and Effects

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Each device in the Freescale PowerQUICC™ II family of communications processors contains several system blocks on a single silicon die (see Table 1). These blocks include a PowerPC™ 603e core, a RISC communications processor module (CPM) and peripherals, and a system integration unit (SIU). Because the PowerQUICC II has three main sources of system reset, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, and $\overline{\text{SRESET}}$, the designer must understand which system blocks are affected by each reset source. This application note describes how the individual system blocks are affected by the individual reset sources and addresses other common questions when dealing with PowerQUICC II reset sources.

Contents

Table 1. PowerQUICC II Devices and Silicon

Device	Process	Silicon [1]			
		0.29 µm (HiP3)	0.25 µm (HiP4)	0.13 µm (HiP7)	
		MPC8260 Family		MPC8280 Family	MPC8272 Family
MPC8260(A) [2]		√	√		
MPC8250			√		
MPC8255(A)[2]		√	√		
MPC8264			√		
MPC8265			√		
MPC8266			√		
MPC8270				√	
MPC8275				√	
MPC8280				√	
MPC8272					√
MPC8271					√
MPC8248					√
MPC8247					√

1 For a complete list of silicon revisions within each PowerQUICC II family, refer to application note AN2291, *Differences Among PowerQUICC™ II Devices and Revisions*.

2 "A" designates HiP4 revisions of a device originally available in a HiP3 version.

1 Reset Sources

Many events, such as input pin assertion, software watchdogs, and timers, can drive a reset to the PowerQUICC II. All of these events use three main reset sources into the PowerQUICC II. These sources are documented in the *MPC8260 PowerQUICC II Family Reference Manual*. The reset sources are as follows:

- $\overline{\text{PORESET}}$. External assertion of $\overline{\text{PORESET}}$ initiates the power-on reset flow so that such operational features as master/slave operation, clock modes, and so on can be selected through the hard reset configuration word (HRCW).
- $\overline{\text{HRESET}}$. Can be initiated externally or internally and begins with the hard reset configuration process. Because the $\overline{\text{HRESET}}$ flow does not sample $\overline{\text{RSTCONF}}$, it cannot be used to configure processor operation as a master or slave. The $\overline{\text{HRESET}}$ flow continues for 1024 input clock cycles, after which the $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ signals are negated. These two signals should be tied with a 1- to 10-KΩ external resistor.
- $\overline{\text{SRESET}}$. Can be initiated externally or internally. The $\overline{\text{SRESET}}$ flow continues for 512 input clock cycles, after which the $\overline{\text{SRESET}}$ signal is negated. The $\overline{\text{SRESET}}$ signal should be tied with a 1- to 10-KΩ external resistor.

2 Reset Effects

Depending on which reset source is asserted, separate PowerQUICC II system blocks undergo reset (that is, the registers associated with the system block are returned to their default settings). Table 2 shows the three reset sources and details the effect of each source on each PowerQUICC II system block. For default (reset) register settings, see the individual register description in the reference manual.

Table 2. Reset Sources and Affected System Blocks

Reset Source	Reset Logic and PLL	Clock Module Reset	Internal Logic [1]	603e Core
PORESET	Y	Y	Y	Y
HRESET	N	N	Y	Y
SRESET	N	N	N	Y

1 Internal logic includes a memory controller, system protection logic, an interrupt controller, and parallel I/O ports.

3 Reset Comments

This section collates and discusses information from frequently asked questions (FAQs) regarding the PowerQUICC II reset sequences. It covers the reset sequence from the assertion of $\overline{\text{HRESET}}$ to the point at which the HRCW has been read.

When $\overline{\text{HRESET}}$ is asserted, any transactions on the bus are aborted (if $\overline{\text{SRESET}}$ is asserted, the bus cycle in progress completes but the data is discarded). At $\overline{\text{HRESET}}$ the device pins take the following states:

- Bidirectional. Set to input.
- Tri-State. Set to Hi-Z.
- Output. Negated

When $\overline{\text{HRESET}}$ is issued, the SDRAM machine returns to its reset state and any SDRAM in the system controlled by the SDRAM machine does not retain its data. However, the SDRAM machine remains active when an $\overline{\text{SRESET}}$ is issued. The time counter (TMCNT) within the PowerQUICC II is affected (that is, reset to zero) when $\overline{\text{PORESET}}$ or $\overline{\text{HRESET}}$ is asserted but not when $\overline{\text{SRESET}}$ is asserted, allowing the user software to track when a soft reset occurred.

If a $\overline{\text{PORESET}}$ flow is initiated, the MODCK[1–3] pins are sampled along with MODCK[4–7] (from the HRCW) to ascertain the PowerQUICC II operating frequencies. It is sufficient for the MODCK[1–3] pins to be tied to the design requirements (that is, they do not need to be actively driven). From a test and debug point of view it should be noted that the JTAG[$\overline{\text{TRST}}$] is internally connected to $\overline{\text{PORESET}}$. This arrangement ensures that the JTAG TAP is in reset state after each power up. The JTAG is available after the PowerQUICC II has negated $\overline{\text{HRESET}}$.

Upon exit of the $\overline{\text{HRESET}}$/$\overline{\text{SRESET}}$ flow, the x$\overline{\text{RESET}}$ signal is negated (through an external pull-up). The processor then waits 16 cycles before testing for an external reset. The 16-cycle wait period ensures that reset pins were adequately pulled up. The processor does nothing else during this period.

It is important to understand the PowerQUICC II bus activity and configuration during the HRCW fetch. The HRCW is fetched a byte at a time from address 0x00 (and increases 0x08 bytes for each byte read). The address is mapped to $\overline{CS0}$. For each bus access during the HRCW read, the $\overline{CS0}$ (chip select 0), $\overline{POE}$ (60x bus output enable) and BCTL0/1 (buffer control 0/1) signals are asserted. During the reset phase, the PowerQUICC II internal reset configuration block controls $\overline{CS0}$. Therefore the configuration of OR0 (or its default configuration) has no effect. The hard reset configuration period always takes 1024-16 CLOCKIN cycles to configure the master and slaves (even if slave devices do not exist in the system). When the HRCW has been read, the external bus mode (HRCW[EBM]) and $\overline{CS10}$ configuration (HRCW[CS10PC]) fields are used to configure which pins are driven during external bus accesses, for example, whether address latch enable (ALE) is active (60x compatible bus mode) and whether $\overline{CS10}$ acts as $\overline{CS10}$ or $\overline{BCTL1}$.

In some cases, the HRCW may be required to be read from a flash memory device, which requires a reset when the entire system is reset. Often these flash memory devices cannot be accessed for a fixed period of time afterward. Delivering the flash reset by the PowerQUICC II (through $\overline{HRESET}$) can cause problems because the PowerQUICC II begins to read the HRCW immediately after the $\overline{HRESET}$ flow ends, which may be a shorter time period than the flash memory allows. It may be necessary to introduce delay logic between the PowerQUICC II reset sources (PO/HRESET) and the flash memory. Two possible implementations for this delay (typically 2–5 ms) are the following:

1. $\overline{HRESET}$ to flash memory. To enable a flash that requires a minimum reset time to be interfaced to the PowerQUICC II $\overline{HRESET}$, interface logic can be used as shown in Figure 1. In this example, the interface logic is used to interpret a $\overline{HRESET}$ assertion by the PowerQUICC II as a reset assertion to the Flash device. From $\overline{HRESET}$ being internally activated, the PowerQUICC II takes 1024 CLOCKIN cycles before $\overline{HRESET}$ is negated. At this point the interface logic can be used to assert $\overline{HRESET}$ into the PowerQUICC II for a combined time period greater than the minimum reset time required by the flash memory. This approach allows the designer to implement the minimum flash reset time while using a PowerQUICC II internal $\overline{HRESET}$ (which can come from sources such as the bus monitor or software watchdog timeout).

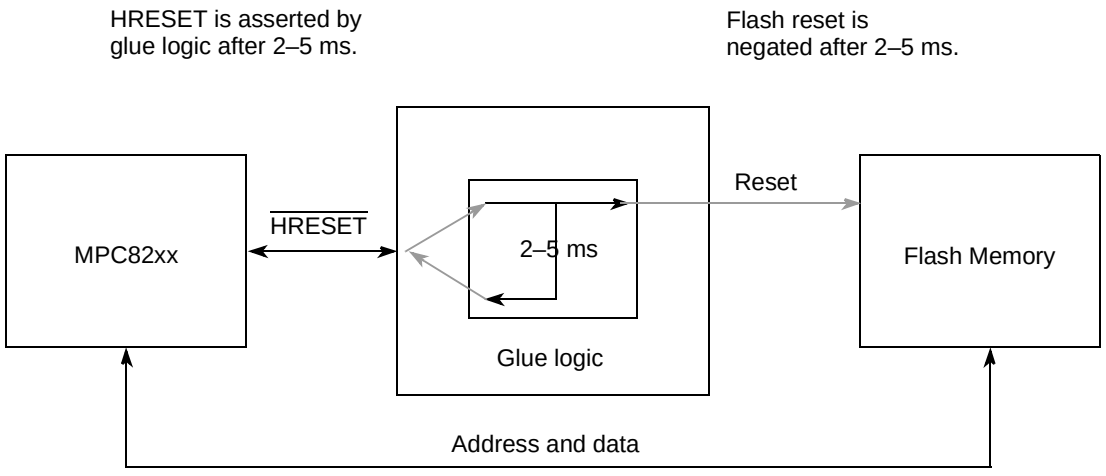

Figure 1. PowerQUICC II $\overline{HRESET}$ to Flash implementation

2. $\overline{\text{PORESET}}$ to flash memory. To enable a flash memory device that requires a minimum reset time to be interfaced to the PowerQUICC II $\overline{\text{PORESET}}$, the designer can implement a logic delay after the flash reset assertion and before $\overline{\text{PORESET}}$ assertion to the PowerQUICC II. If the logic delay is long enough to cover the required flash reset time (typically 2–5 ms), the PowerQUICC II can safely fetch the HRCW data from flash memory.

4 References

For additional information, consult the reference documentation shown in Table 3.

Table 3. References

Document Category	Document Title	Document ID
Hardware Specifications	MPC8260 (0.29-µm HiP3) Hardware Specifications	MPC8260EC
	MPC8260 (0.25-µm HiP4) Hardware Specifications	MPC8260AEC
	MPC8280 (0.13-µm HiP7) Hardware Specifications	MPC8280AEC
Reference Manual	*MPC8260 PowerQUICC II Reference Manual* (Rev. 1)	MPC8260UM
	MPC8280 Addendum to the MPC8260 Reference Manual	MPC8280UMAD

5 Document Revision History

Table 4. Document Revision History

Revision	Date	Substantive Changes
0	12/2003	Original release of document
0.1	2/2004	Section 3: Addition of implementation descriptions at the end of the section
1	1/2007	Non-substantive formatting.

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