Application Note

AN2521/D
Rev.0 , 5/2003

BLDC Motor version II TPU Function Set (BLDC)

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Functional Overview

BLDC Motor version II (BLDC) is an alternative realization of the algorithm provided by BLDC Motor version I (BLDCm). This realization presents some advantages and some disadvantages when compared with the BLDC Motor version I (BLDCm). This version commutates the PWM phases immediately after the Hall sensor signals indicate a new sector (see **Figure 2**). This is an advantage for high speed motion systems. The disadvantage of this version is a lower maximum motor voltage amplitude (see **Minimum Pulse Width**). The function set consists of 6 TPU functions:

- 3-phase Hall Sensor Decoder for BLDC Motor (BLDC_3HD)
- BLDC Motor – Top (BLDC_top)
- BLDC Motor – Bottom (BLDC_bottom)
- Synchronization Signal for BLDC Motor (BLDC_sync)
- Resolver Reference Signal for BLDC Motor (BLDC_res)
- Fault Input for BLDC Motor (BLDC_fault)

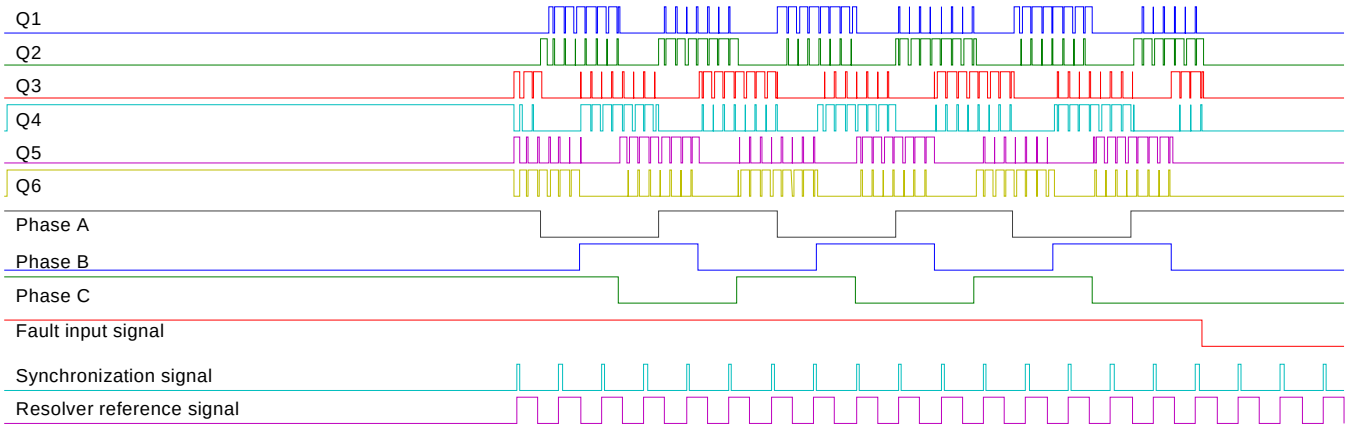

Figure 1. Signals processed by BLDC TPU function set

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The BLDC_3HD function receives the Hall Sensor signals and controls the commutation of 3 PWM phases. The BLDC_top and BLDC_bottom TPU functions work together to generate a 6-channel 3-phase center-aligned PWM signal with dead-time between the top and bottom channels. One of the phases is always switched off while the other two generate the PWM signal. The Synchronization Signal for the BLDC function can be used to generate one or more adjustable signals for a wide range of uses, which are synchronized to the PWM, and track changes in the PWM period. The Resolver Reference Signal for the BLDC function can be used to generate one or more 50% duty-cycle adjustable signals that are also synchronized to the PWM.The Fault Input for BLDC function is a TPU input function that sets all PWM outputs low when the input signal goes low. See **Figure 1**.

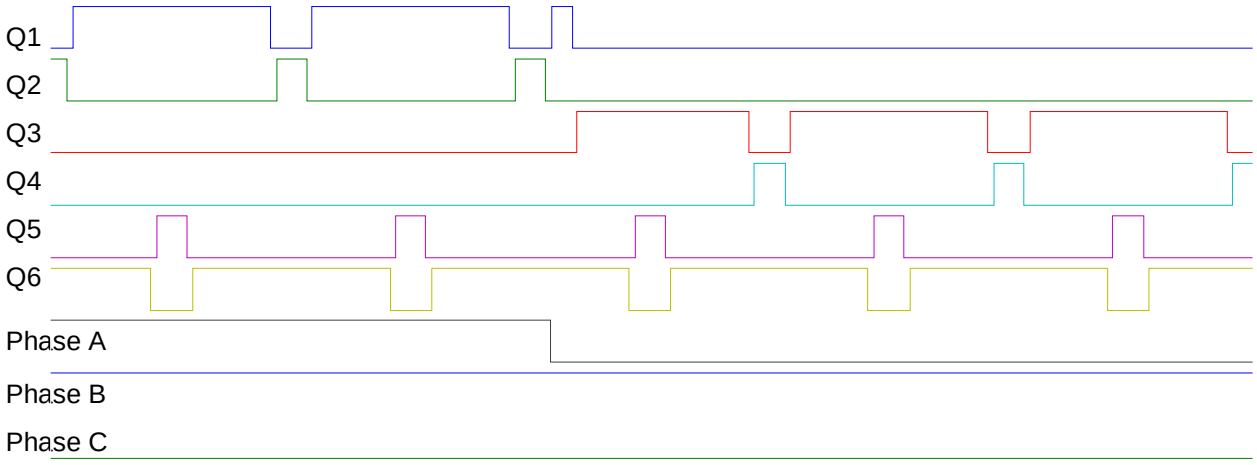

Figure 2. Example of commutation

NOTE: *Q1 and Q2 channels are switched off and Q3 Q4 channels are switched on immediately after the change on Phase A Hall sensor signal.*

Function Set Configuration

None of the TPU functions in the BLDC Motor TPU function set can be used separately. The BLDC_3HD, BLDC_top and BLDC_bottom functions have to be used together. The BLDC_3HD is used on 3 input channels while the BLDC_top is used on 3 output channels and the BLDC_bottom is used on other 3 output channels, with higher numbers then the BLDC_top channels. One or more channels running Synchronization Signal for BLDC as well as Resolver Reference Signal for BLDC functions can be added. They can run with different settings on each channel. The function Fault Input for BLDC can also be added. It is recommended to use it on channel 15, and to set the hardware option that

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disables all TPU output pins when the channel 15 input signal is low (DTPU bit = 1). This ensures that the hardware reacts quickly to a pin fault state. Note that it is not only the PWM channels, but all TPU output channels, including the synchronization signals, that are disabled in this configuration.

Table 1 shows the configuration options and restrictions.

Table 1. BLDC TPU function set configuration options and restrictions

TPU function	Optional/ Mandatory	How many channels	Assignable channels
BLDC_3HD	mandatory	3	any 3 channels
BLDC_top	mandatory	3	any 3 channels, lower than BLDC_bottom channels
BLDC_bottom	mandatory	3	any 3 channels, higher thea BLDC_top channels
BLDC_sync	optional	1 or more	any channels
BLDC_res	optional	1 or more	any channels
BLDC_fault	optional	1	any, recommended is 15 and DTPU bit set

Table 2 and Table 3 show two examples of configuration.

Table 2. Example of configuration

Channel	TPU function	Priority
0	BLDC_top	high
1	BLDC_top	high
2	BLDC_top	high
3	BLDC_bottom	high
4	BLDC_bottom	high
5	BLDC_bottom	high
6	BLDC_3HD	high
7	BLDC_3HD	high
8	BLDC_3HD	high
10	BLDC_sync	low
15	BLDC_fault	high

Table 3. Example of configuration

Channel	TPU function	Priority
0	BLDC_top	high
1	BLDC_top	high
2	BLDC_top	high

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Table 3. Example of configuration

Channel	TPU function	Priority
3	BLDC_bottom	high
4	BLDC_bottom	high
5	BLDC_bottom	high
10	BLDC_sync	low
11	BLDC_res	low
12	BLDC_3HD	high
13	BLDC_3HD	high
14	BLDC_3HD	high
15	BLDC_fault	high

Table 4 shows the TPU function code sizes.

Table 4. TPU function code sizes

TPU function	Code size
BLDC_3HD	69 µ instructions + 8 entries = 77 long words
BLDC_top	57 µ instructions + 8 entries = 65 long words
BLDC_bottom	171 µ instructions + 8 entries = 179 long words
BLDC_sync	26 µ instructions + 8 entries = 34 long words
BLDC_res	38 µ instructions + 8 entries = 46 long words
BLDC_fault	9 µ instructions + 8 entries = 17 long words

Configuration Order

The CPU configures the TPU as follows.

1. Disables the channels by clearing the two channel priority bits on each channel used (not necessary after reset).
2. Selects the channel functions on all used channels by writing the function numbers to the channel function select bits.
3. Initializes function parameters. The parameters *PinAddr_A*, *PinAddr_B*, *T*, *DT*, *MPW* and *sync_presc_addr* must be set before initialization. If a BLDC_sync channel or a BLDC_res channel is used, then also its parameters must be set before initialization.
4. Issues an HSR (Host Service Request) type %10 to all BLDC_3HD channels, to initialize them, and to one of the BLDC_bottom channels to initialize all PWM channels. Issues an HSR type %10 to the BLDC_sync channels, BLDC_res channels and BLDC_fault channel, if used.
5. Enables servicing by assigning a high, middle or low priority to the channel priority bits. All Hall sensor channels, as well as all PWM channels, must be assigned the same priority to ensure correct operation. The CPU must ensure that BLDC_bottom (which actually initializes all PWM channels) is initialized after the initialization of

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BLDC_3HD, and that the BLDC_sync or BLDC_res function is initialized even after the initialization of BLDC_bottom:

- assign a priority to the Phase A, Phase B and Phase C Hall sensor channels to enable their initialization
- wait until the HSR bits are cleared to indicate that initialization of these channels has completed
- assign a priority to the PWM channels to enable their initialization
- if a Synchronization Signal or a Resolver Reference Signal channel is used, wait until the HSR bits are cleared to indicate that initialization of the PWM channels has completed and
- assign a priority to the BLDC_sync or BLDC_res channel to enable its initialization

NOTE: *A CPU routine that configures the TPU can be generated automatically using the MPC500_Quick_Start Graphical Configuration Tool.*

Detailed Function Description

3-phase Hall Sensor Decoder for BLDC Motor (BLDC_3HD)

The BLDC_3HD operates on three channels and processes the incoming Hall sensor signals. On each detected transition that marks a change of position in one of six sectors, a link is sent to two pairs of PWM channels to force them to commutate. One pair of PWM channels is switched ON by the link while the other pair is switched OFF.

Furthermore, as a result of this processing, the Sector parameter gets a value that reflects the position of a motion system in one of six sectors. The state of the Hall sensor signals and the corresponding Sector value is listed in **Table 5**.

Table 5. Hall sensor signal states and corresponding Sector value

Phase A	Phase B	Phase C	Sector
1	0	0	4
1	1	0	6
0	1	0	2
0	1	1	3
0	0	1	1
1	0	1	5
0	0	0	0
1	1	1	7

A Sector value of 0 or 7 indicates an illegal state of the Hall sensor signals.

The Sector value history determines the direction of the motion system. The Direction parameter can be assigned a value of 0 or 1. See **Table 6**.

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Table 6. Sector value sequence and corresponding Direction value

Sector value sequence	Direction
4, 6, 2, 3, 1, 5, 4, ...	0
4, 5, 1, 3, 2, 6, 4, ...	1

The Period value is calculated each time the sector is changed. The Period value is the TCR time of last revolution. It is measured from the last edge of similar type (low-high / high-low), on the same channel, to the current edge – see **Figure 3**. This method eliminates inaccuracies in the Hall sensor signals. The Period parameter does not contain a valid value during the first revolution after initialization, or after a change of direction.

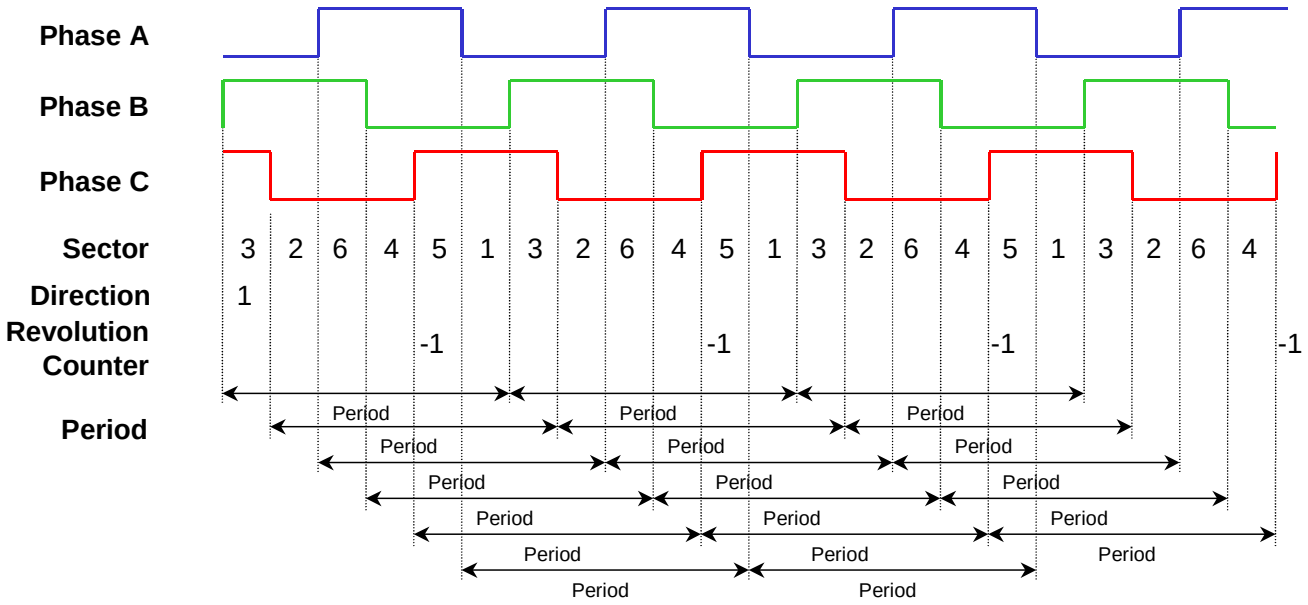

Figure 3. Hall sensor signals and corresponding values

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Two function modes are provided:

- TCR1 clock selected
- TCR2 clock selected

The selected mode is determined by the HSQ bit 1. The user has to select the same mode on all channels.

The function provides interpolation support. The parameters LastEdgeT and ActualT are updated on a Host Service Request HSR = 11. LastEdgeT then has the value of the last incoming edge time in TCR clocks and ActualT has the current value of the TCR clock.

The CPU program should use 32-bit reads to ensure coherency of the two parameters. This applies to coherent reads of LastEdgeT and ActualT as well as the Sector and TCR_VALUE, which is necessary for interpolation calculations.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 7. BLDC_3HD Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_3HD function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Get LastEdgeT and ActualT
1 0 Host Sequence Bits (HSQ)	x0 – Phase A or Phase B x1 – Phase C 0x –TCR1 clock selected 1x – TCR2 clock selected
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

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TPU function BLDC_3HD generates an interrupt each time the Sector is changed.

Table 8. BLDC_3HD Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Phase A	0	TCR_VALUE															
	1	Sector															
	2	PinAdr_A															
	3	ON_chans_A															
	4	OFF_chans_A															
	5	PINSTATE_A															
	6	EdgeT_LH_A															
	7	EdgeT_HL_A															
Phase B	0	LastEdgeT															
	1	ActualT															
	2	PinAdr_B															
	3	ON_chans_B															
	4	OFF_chans_B															
	5	PINSTATE_B															
	6	EdgeT_LH_B															
	7	EdgeT_HL_B															
Phase C	0	Direction															
	1	RC															
	2	Period															
	3	ON_chans_C															
	4	OFF_chans_C															
	5	PINSTATE_C															
	6	EdgeT_LH_C															
	7	EdgeT_HL_C															

Table 9. BLDC_3HD parameter description

Parameter	Format	Description
Parameters written by CPU		
PinAdr_A	16-bit unsigned integer	$YAZA, where Y is a number of Phase B channel and Z is a number of Phase C channel

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Table 9. BLDC_3HD parameter description

Parameter	Format	Description
PinAdr_B	16-bit unsigned integer	$ZAXA, where Z is a number of Phase C channel and X is a number of Phase A channel
Parameters written by both TPU and CPU		
RC	16-bit signed integer	Revolution Counter value
Parameters written by TPU		
LastEdgeT	16-bit unsigned integer	TCR time of last transition *
ActualT	16-bit unsigned integer	Actual TCR time *
Direction	0 or 1	Direction 0 – Sector sequence 4, 6, 2, 3, 1, 5, 4, ... 1 – Sector sequence 4, 5, 1, 3, 2, 6, 4, ...
TCR_VALUE	16-bit unsigned integer	TCR time of last transition
Sector	4, 6, 2, 3, 1 or 5	Sector: position in one of six sectors
Period	16-bit unsigned integer	Period: time of last revolution in TCR clocks.
PINSTATE_A PINSTATE_B PINSTATE_C	$0000 or $0001	The actual state of the pin is $0001 – high, $0000 – low
EdgeT_LH_A EdgeT_LH_B EdgeT_LH_C	16-bit unsigned integer	TCR time of last low-high transition
EdgeT_HL_A EdgeT_HL_B EdgeT_HL_C	16-bit unsigned integer	TCR time of last high-low transition
* The parameter values are entered by TPU on Host Service Request 11 (Get LastEdgeT and ActualT).		
Other parameters are just for TPU function inner use.		

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Table 10. BLDC_3HD State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	22	5
GET_TIME	8	3
LH1	36	14
HL1	36	14
LH2	40	15
HL2	40	15

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

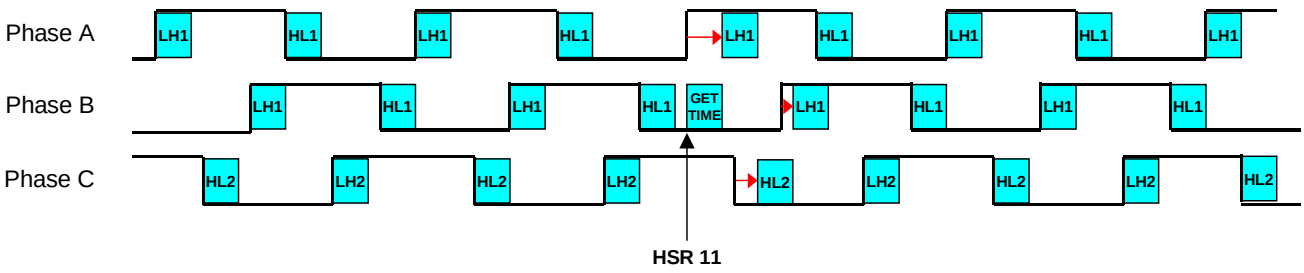

Figure 4. BLDC_3HD timing

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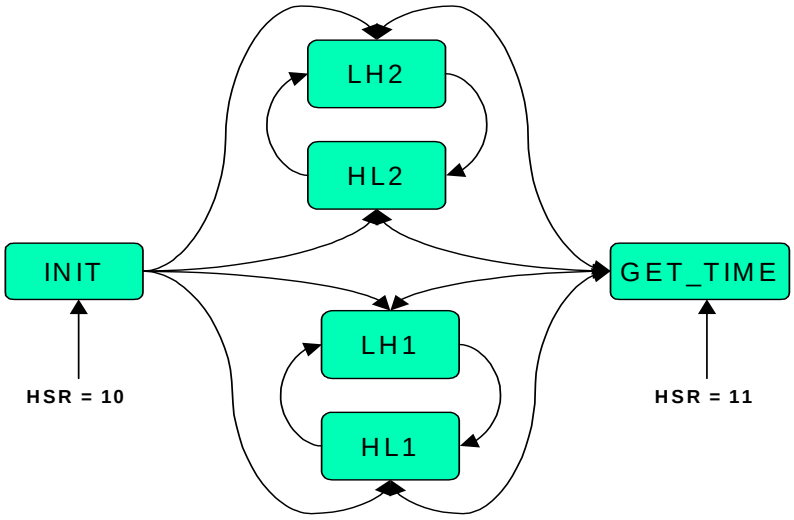

Figure 5. BLDC_3HD state diagram

Noise Immunity

The input signals can be disturbed by an impulse noise. The TPU hardware rejects short input pulses of less than a configurable number of IMB clocks. Longer pulses are processed by the TPU. Furthermore the function itself uses a pin history to reject short error pulses that are long enough to get through the hardware filter, but not long enough to last from the actual transition time to the time that the TPU services the channel. Even longer error pulses are counted on both edges, resulting in a short-time error of the Sector value.

BLDC Motor – Top (BLDC_top) and BLDC Motor – Bottom (BLDC_bottom)

The BLDC_top and BLDC_bottom TPU functions work together to generate a 6-channel, 3-phase PWM signal, with dead-time between the top and bottom channels. In order to charge the bootstrap transistors, the PWM signals start to run 1.6ms after their initialization (at 20MHz TCR1 clock). The functions generate signals corresponding to value of 0 for duty-cycle ratio *dc* until the first *dc* value is processed. This accures for at least one PWM period.

One of the phases is always switched off while the other two generate the PWM signal. Which phase is switched off, depends on which one of the six sectors the rotor is positioned in. The position is decoded from the Hall sensor signals.

The CPU controls the PWM output by setting the TPU parameters. The duty-cycle ratio *dc* and PWM period *T* can be adjusted during run time. Conversely, dead-time (*DT*) and minimum pulse width (*MPW*) are not supposed to be changed during run time. The duty-cycle ratio *dc* can gain a value in the range (–1, 1). The sign controls the motion system direction, while the absolute value controls the amplitude of the applied voltage.

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The following figures show the input *dc* value and corresponding output PWM signals (valid for sector 4, direction 0):

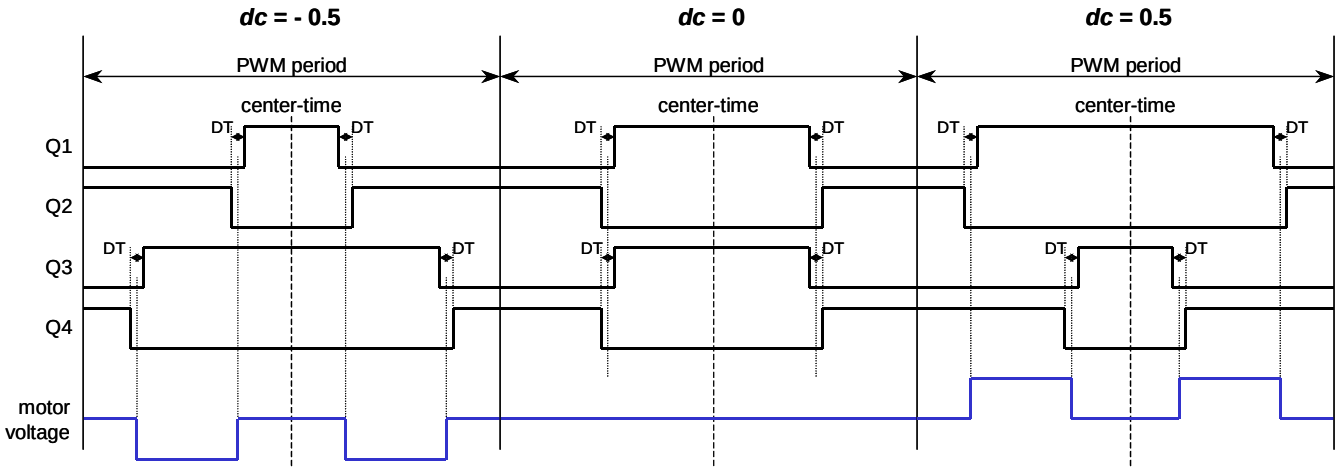

Figure 6. Unipolar switching

The following equations describe how the PWM signal transition times *T1p*, *T2p*, *B1p*, *B2p*, *T1m*, *T2m*, *B1m*, *B2m* are calculated, and how they are assigned to each channel transition time t_{LH} and t_{HL} based on BLDCm commutation rules:

$$Tdc_{\alpha} = T \cdot dc$$

$$X = \frac{T + Tdc}{2}$$

$$Y = \frac{T - Tdc}{2}$$

$$A = \frac{X - DT}{2} \qquad C = \frac{Y - DT}{2}$$

$$B = \frac{X + DT}{2} \qquad D = \frac{Y + DT}{2}$$

$$T1p = center\_time - A \qquad T2p = center\_time + A$$

$$B1p = center\_time - B \qquad B2p = center\_time + B$$

$$T1m = center\_time - C \qquad T2m = center\_time + C$$

$$B1m = center\_time - D \qquad B2m = center\_time + D$$

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Table 11. Assigment of the calculated transition times to each channel transition times t_{LH} and t_{HL} based on the BLDC comutation rules

Channel	Sector					
	4	6	2	3	1	5
Q1	$t_{LH} = T1p$ $t_{HL} = T2p$	$t_{LH} = T1p$ $t_{HL} = T2p$	OFF	$t_{LH} = T1m$ $t_{HL} = T2m$	$t_{LH} = T1m$ $t_{HL} = T2m$	OFF
Q2	$t_{LH} = B2p$ $t_{HL} = B1p$	$t_{LH} = B2p$ $t_{HL} = B1p$	OFF	$t_{LH} = B2p$ $t_{HL} = B1p$	$t_{LH} = B2p$ $t_{HL} = B1p$	OFF
Q3	$t_{LH} = T1m$ $t_{HL} = T2m$	OFF	$t_{LH} = T1p$ $t_{HL} = T2p$	$t_{LH} = T1p$ $t_{HL} = T2p$	OFF	$t_{LH} = T1m$ $t_{HL} = T2m$
Q4	$t_{LH} = B2p$ $t_{HL} = B1p$	OFF	$t_{LH} = B2p$ $t_{HL} = B1p$	$t_{LH} = B2p$ $t_{HL} = B1p$	OFF	$t_{LH} = B2p$ $t_{HL} = B1p$
Q5	OFF	$t_{LH} = T1m$ $t_{HL} = T2m$	$t_{LH} = T1m$ $t_{HL} = T2m$	OFF	$t_{LH} = T1p$ $t_{HL} = T2p$	$t_{LH} = T1p$ $t_{HL} = T2p$
Q6	OFF	$t_{LH} = B2p$ $t_{HL} = B1p$	$t_{LH} = B2p$ $t_{HL} = B1p$	OFF	$t_{LH} = B2p$ $t_{HL} = B1p$	$t_{LH} = B2p$ $t_{HL} = B1p$

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 12. BLDC_top Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_top function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Not used 11 – Not used

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Table 12. BLDC_top Control Bits

Name	Options
1 0 Host Sequence Bits (HSQ)	x – Not used
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

Table 13. BLDC_bottom Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_bottom function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Stop
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

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Table 14. BLDC_top and BLDC_bottom Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q1	0	pinst_addr_Q1															
	1	other_ch_Q1															
	2	C															
	3	T1p															
	4	T2p															
	5	dc															
	6																
	7	fault_pinstate															
Q2	0	pinst_addr_Q2															
	1	other_ch_Q2															
	2	Tdc															
	3	B1p															
	4	B2p															
	5	DT															
	6																
	7																
Q3	0	pinst_addr_Q3															
	1	other_ch_Q3															
	2	D															
	3	T1m															
	4	T2m															
	5	T															
	6																
	7																
Q4	0	pinst_addr_Q4															
	1	other_ch_Q4															
	2	T_copy															
	3	B1m															
	4	B2m															
	5	MPW															
	6																
	7																
Q5	0	pinst_addr_Q5															
	1	other_ch_Q5															
	2	center_time															
	3																
	4																
	5	sync_presc_addr															
	6																
	7																

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Table 14. BLDC_top and BLDC_bottom Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Q6	0	pinst_addr_Q6															
	1	other_ch_Q6															
	2	L															
	3																
	4																
	5																
	6																
	7																

Table 15. BLDC_top and BLDC_bottom parameter description

Parameter	Format	Description
Parameters written by CPU		
dc	16-bit fractional	duty-cycle ratio in the range <–1,1)
T	16-bit unsigned integer	PWM period in number of TCR1 TPU cycles
DT	16-bit unsigned integer	Dead-time in number of TCR1 TPU cycles
MPW	16-bit unsigned integer	Minimum pulse width in number of TCR1 TPU cycles. See **Performance** for details.
sync_presc_addr	8-bit unsigned integer	address of synchronization channel *prescaler* parameter: $X4, where X is synchronization channel number. $0 if no synchronization channel is used.
Parameters written by TPU		
fault_pinstate	0 or 1	If fault channel is used, state of fault pin: 0 ... low 1 ... high
Other parameters are just for TPU function inner use.		

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Table 16. BLDC_top State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
T	24	5
TC2	42	18
$ONOFF_{ON}$	14	0
$ONOFF_{OFF}$	6	0

Table 17. BLDC_bottom State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	178	47
STOP	38	0
T	24	5
TC1	82	12
$ONOFF_{ON}$	14	0
$ONOFF_{OFF}$	6	0

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

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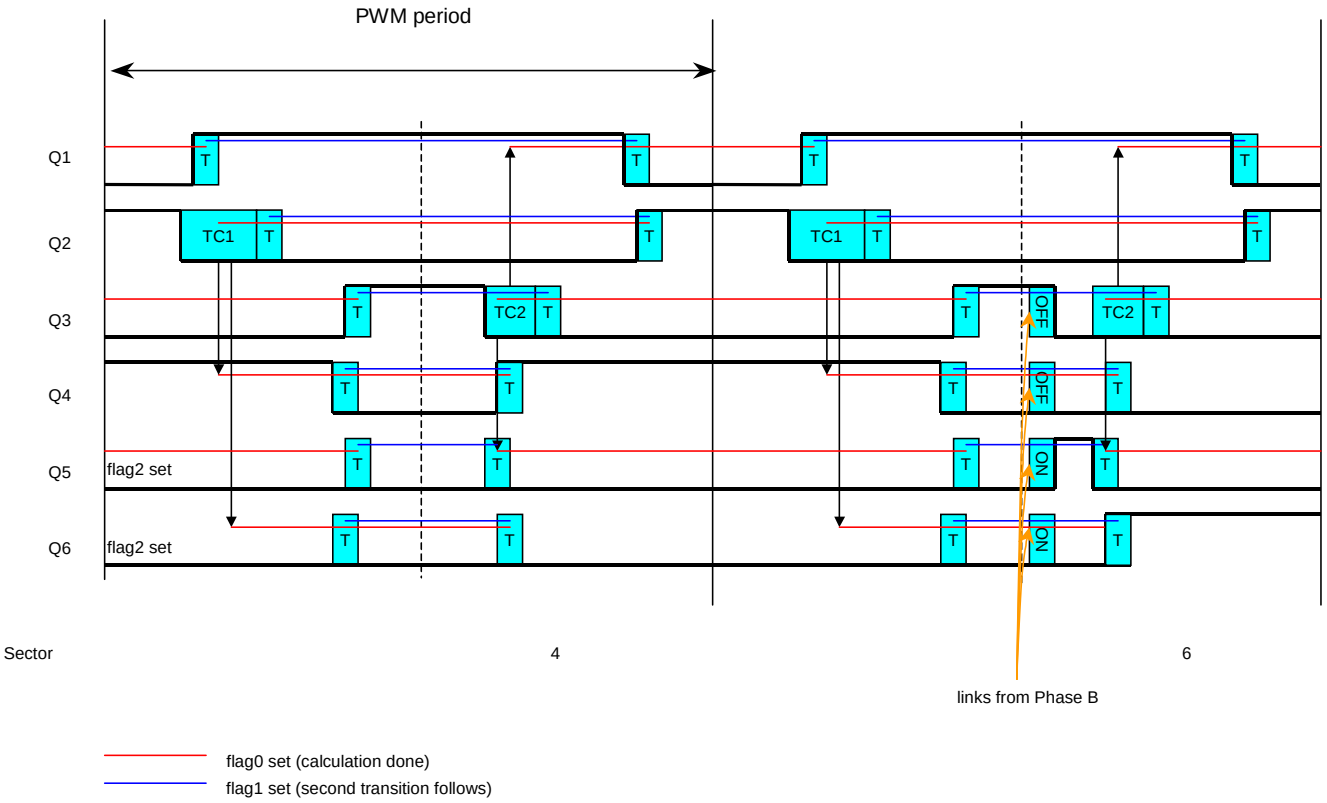

Figure 7. BLDC_top and BLDC_bottom timing

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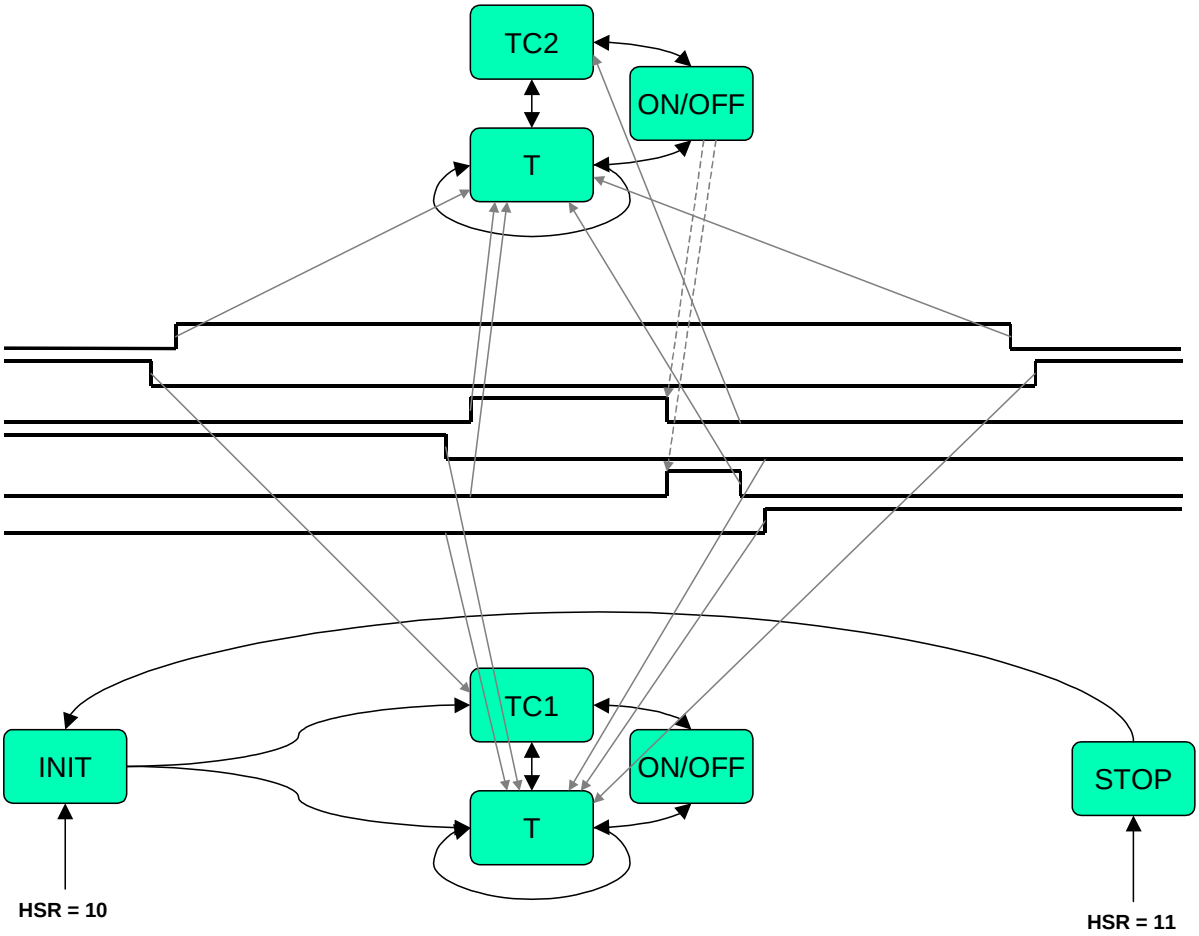

Figure 8. BLDC_top and BLDC_bottom state diagram

Minimum Pulse Width

The TPU cannot generate PWM signals with duty cycle ratios very close to 0% or 100%. It is the case when the dc value is close to 1 or –1. The minimum pulse width that the TPU can be guaranteed to correctly generate is determined by the TPU function itself and by the activity on the other channels. When the TPU function is requested to generate a narrower pulse a collision can occur. To prevent this, the parameter *MPW* (minimum pulse width) is introduced. The TPU function BLDCm limits the narrowest generated pulse widths to *MPW*. The CPU program should check the maximum absolute value of *dc* to avoid this limitation, or take account of the non-linear performance when *dc* moves towards the boundary values and the limitation is exhibited by the TPU. The maximum absolute value of *dc* should satisfy:

$$|dc| \leq 1 - \frac{2(MPW + DT)}{T}$$

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The *MPW* is written by the CPU. The *MPW* depends on the whole TPU unit configuration, especially the lengths of the longest states of other functions, and their priorities, running on the same TPU. The *MPW* has to be correctly calculated at the time the whole TPU unit is configured.

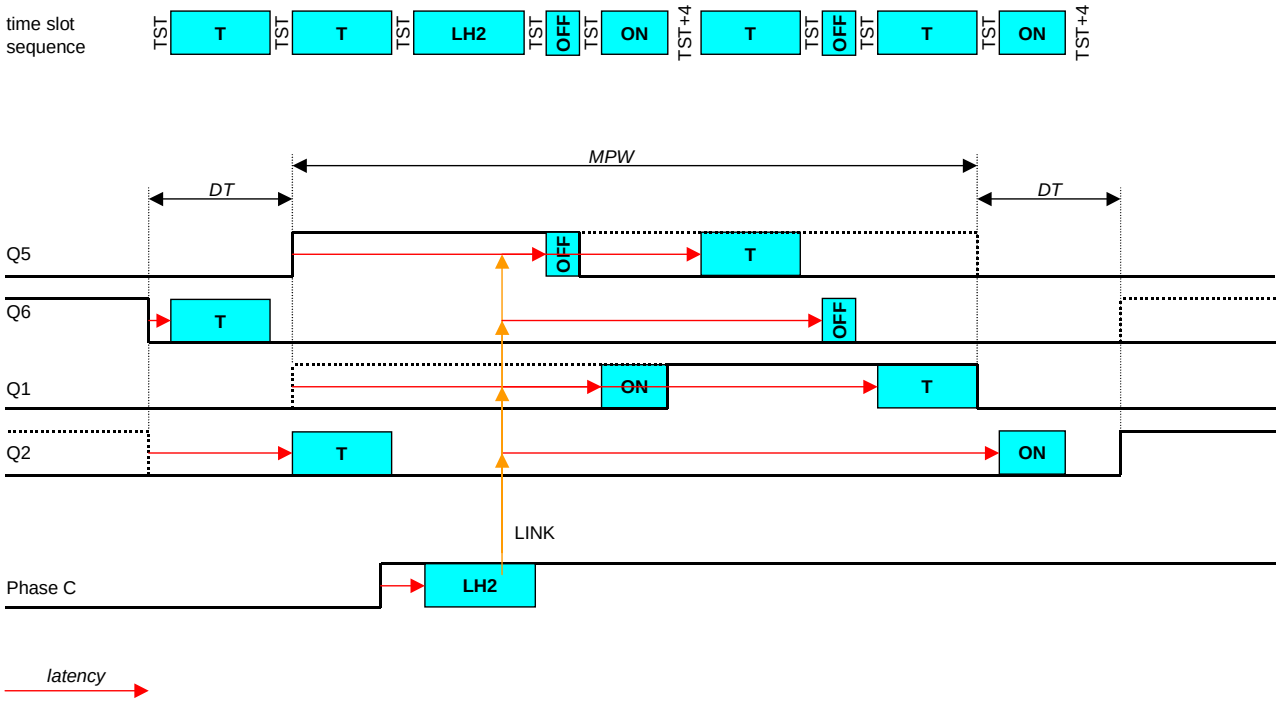

Figure 9. Worst case timing – case one

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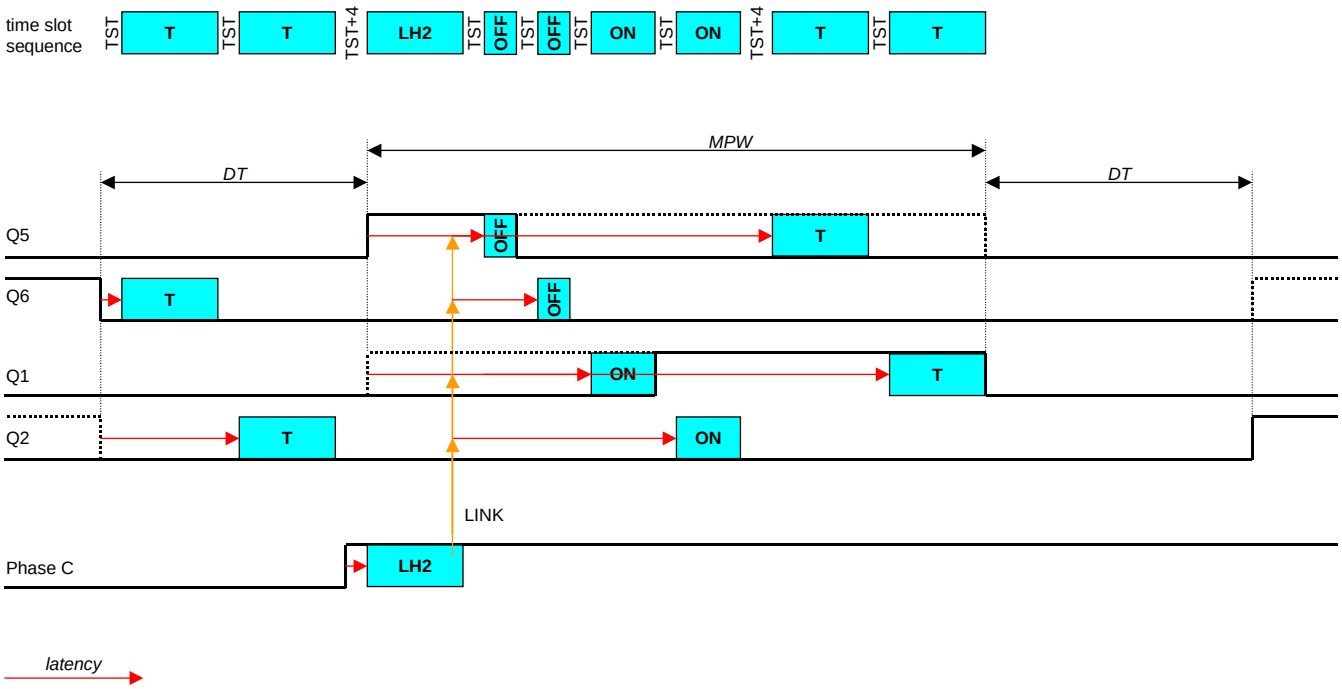

Figure 10. Worst case timing – case two

When BLDC_top and BLDC_bottom are running alone on one TPU, the minimum pulse width can be calculated according to **Figure 9** or **Figure 10**. These illustrate two possible worst cases of timing, when only compulsory BLDC functions are running on one TPU (BLDC_top, BLDC_bottom and BLDC_3HD). The worst case happens when a transition on one of the Hall sensor signals is detected and processed during the shortest pulse on a PWM channel. The processing send links to four PWM channels to switch them on or off. Processing of the detected transition (state LH2), all the ON/OFF states and the transition states T, therefore has to be done within *MPW*. Each state is preceded by the Time Slot Transition (TST), which takes 10 or 14 IMB clock cycles.

According to the **Figure 9** the *MPW* is 246 IMB clock cycles – *DT*. According to **Figure 10** the *MPW* is 192 IMB clock cycles. In summary the MPW parameter value is equal to 246 IMB clock cycles – *DT*, and has a minimum value of 192 IMB clock cycles.

Note that the *MPW*, as well as the *DT*, are not entered into the parameter RAM in IMB clock cycles, but in TCR1 clock cycles. It is recommended for the BLDC function that the TCR1 clock is configured for its maximum speed, which is the IMB clock divided by 2. In this case the *MPW* = 123 – *DT*, with a minimum value of 96.

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When other functions are running concurrently on the same TPU, the longest state of each function with its time-slot transition can increase the calculated *MPW* value. The BLDC_fault function does not affect the *MPW*. The BLDC_sync, if used, increase the *MPW* value by 22 (44 IMB clock cycles). The BLDC_res, if used, increase the *MPW* value by 20 (40 IMB clock cycles).

If a lower value than the one calculated, is set for the *MPW* parameter, the motion system can run with a higher motor voltage amplitude, but with a risk, that the dead-time is not maintained.

It is also possible to use the Worst-Case Latency (WCL), which is automatically calculated by the MPC500_Quick_Start Graphical Configuration Tool. It can serve as a good approximation of *MPW*. The calculated WCL is always longer than the real-case is. Let the WCL be calculated after the configuration of TPU channels and then find the longest WCL value within all BLDC PWM channels. Convert the number, from IMB clock cycles to TCR1 clock cycles, to get the *MPW*.

Synchronization signal for BLDC Motor (BLDC_sync)

The BLDC_sync TPU function uses information obtained from BLDC PWM functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, which tracks the changes in the PWM period and is always synchronized with the PWM. The synchronization signal is a positive pulse generated repeatedly after the *prescaler* or *presc_copy* PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go a number of TCR1 TPU cycles before or after the PWM period center time. The pulse width *pw* is another synchronization signal parameter.

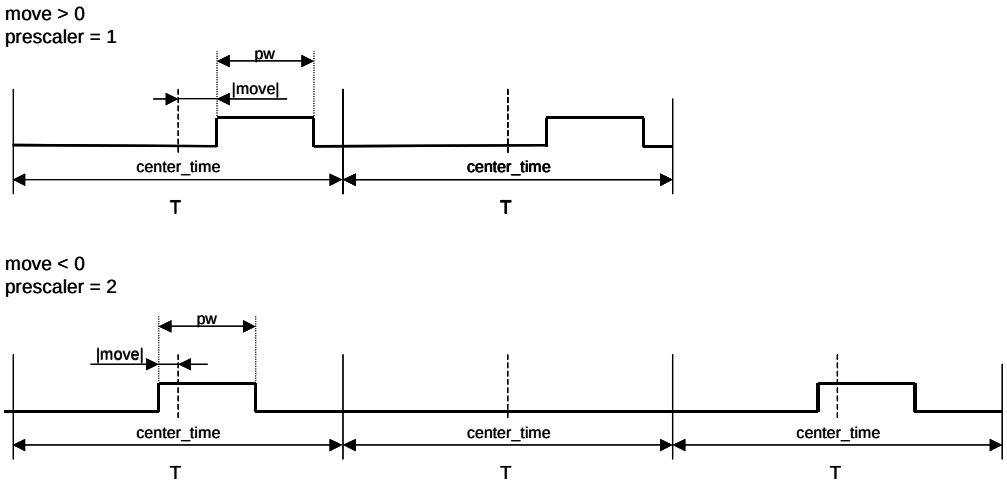

Figure 11. Synchronization signal adjustment examples

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Synchronized Change of PWM Prescaler And Synchronization Signal Prescaler

The BLDC_sync TPU function actually uses the *presc_copy* parameter instead of the *prescaler* parameter. The *prescaler* parameter holds the prescaler value that is copied to the *presc_copy* by the BLDC_bottom function at the time the PWM parameters are reloaded. This ensures that new prescaler values for the PWM signals, as well as the synchronization signal, are applied at the same time. Write the synchronization signal *prescaler* parameter address to the *sync_presc_addr* parameter to enable this mechanism. Write 0 to disable it, and remember to set the synchronization signal *presc_copy* parameter instead of the *prescaler* parameter in this case.

Host Interface

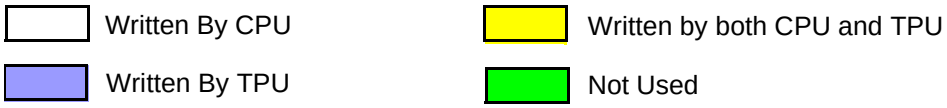

Table 18. BLDC_sync Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_sync function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function BLDC_sync generates an interrupt after each low to high transition.

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Table 19. BLDC_sync Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Synchronization channel	0	move															
	1	pw															
	2	prescaler															
	3	presc_copy															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 20. BLDC_sync parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time
pw	16-bit unsigned integer	Synchronization pulse width in number of TCR1 TPU cycles.
prescaler	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of synchronized prescalers change
presc_copy	16-bit unsigned integer	The number of PWM periods per synchronization pulse – use in case of asynchronized prescalers change
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less than a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

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Table 21. BLDC_sync State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	12	6
S2	8	3
S3	16	7

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

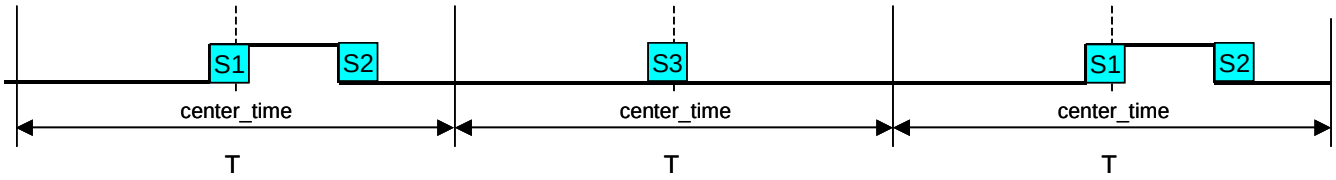

Figure 12. BLDC_sync timing

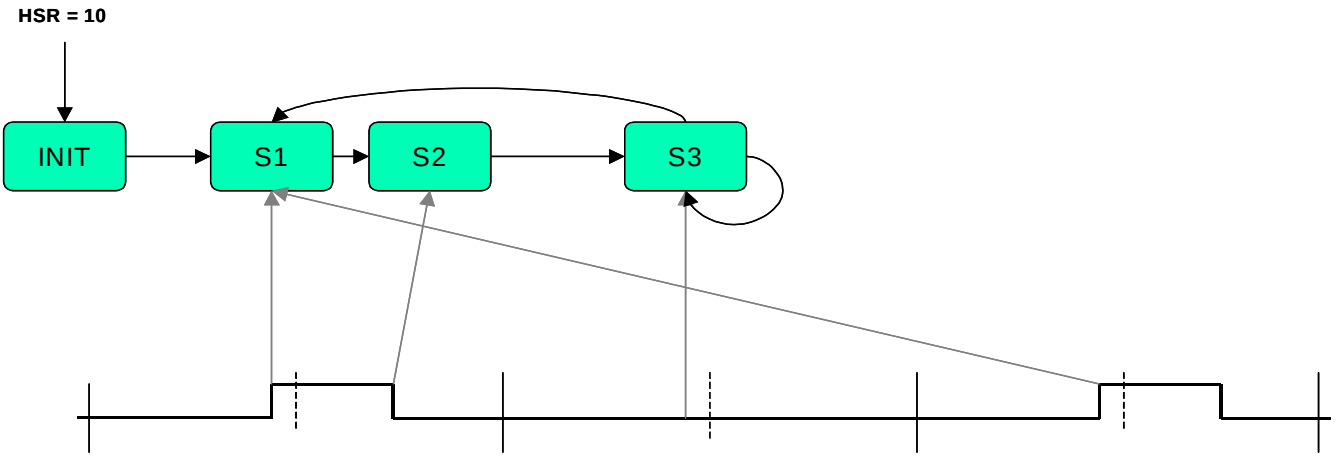

Figure 13. BLDC_sync state diagram

Resolver Reference Signal for BLDC Motor (BLDC_res)

The BLDC_res TPU function uses information read from the BLDC PWM functions, the actual PWM center times and the PWM periods. This allows a signal to be generated, which tracks the changes of the PWM period and is always synchronized with the PWM. The resolver reference signal is a 50% duty-cycle signal with a period equal to *prescaler* or synchronization channel

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presc_copy PWM periods (see next paragraph). The low to high transition of the pulse can be adjusted by a parameter, either negative or positive, to go a number of TCR1 TPU cycles before or after the PWM period center time.

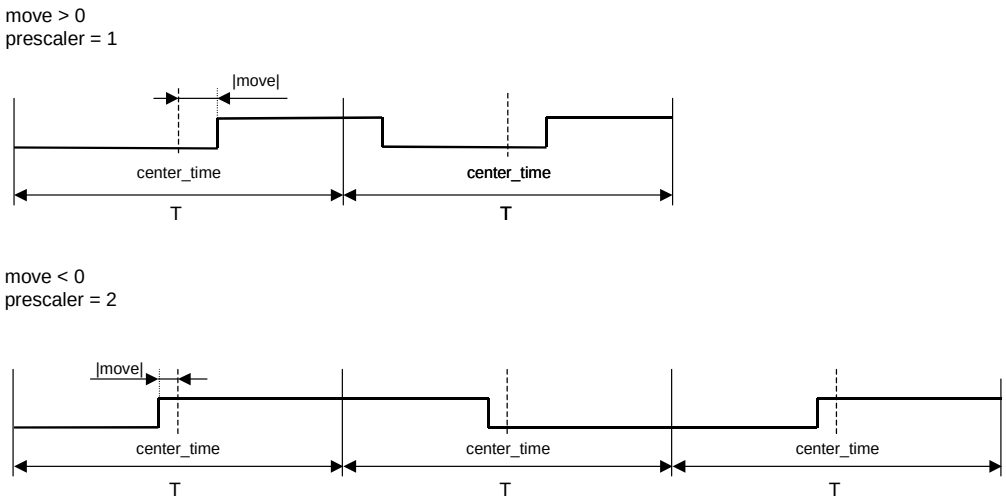

Figure 14. Resolver reference signal adjustment examples

Synchronized Change of PWM Prescaler And Resolver Reference Signals Prescaler

The BLDC_res TPU function can inherit the Synchronization Signal prescaler that is synchronously changed with the PWM prescaler. Write the synchronization signals *presc_copy* parameter address to the *presc_addr* parameter to enable this mechanism. Write 0 to disable it, and in this case set the *prescaler* parameter to directly specify prescaler value.

Host Interface

Written By CPU

Written by both CPU and TPU

Written By TPU

Not Used

Table 22. BLDC_res Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_res function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority

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Table 22. BLDC_res Control Bits

Name	Options
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	x – Not used
0 Channel Interrupt Status	x – Not used

Table 23. BLDC_res Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Resolver	0	move															
	1																
	2	presc_addr															
	3	prescaler															
	4	time															
	5	dec															
	6	T_copy															
	7																

Table 24. BLDC_res parameter description

Parameter	Format	Description
Parameters written by CPU		
move	16-bit signed integer	The number of TCR1 TPU cycles to forego (negative) or come after (positive) the PWM period center time

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Table 24. BLDC_res parameter description

Parameter	Format	Description
presc_addr	16-bit unsigned integer	$00X6, where X is a number of Synchronization Signal channel, to inherit Sync. channel prescaler or $0000 to enable direct specification of prescaler value in prescaler parameter
prescaler	1, 2, 4, 6, 8, 10, 12, 14, ...	The number of PWM periods per synchronization pulse – use when apresc_addr = 0
Parameters written by TPU		
Other parameters are just for TPU function inner use.		

Performance

There is one limitation. The absolute value of parameter *move* has to be less than a quarter of the PWM period *T*.

$$|move| < \frac{T}{4}$$

Table 25. BLDC_res State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	12	5
S1	26	9
S3	18	7

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

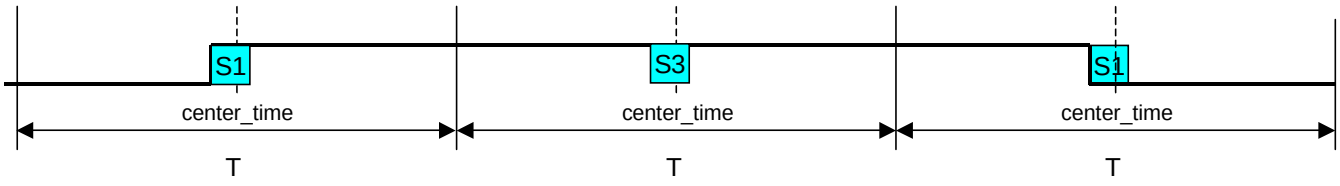

Figure 15. BLDC_res timing

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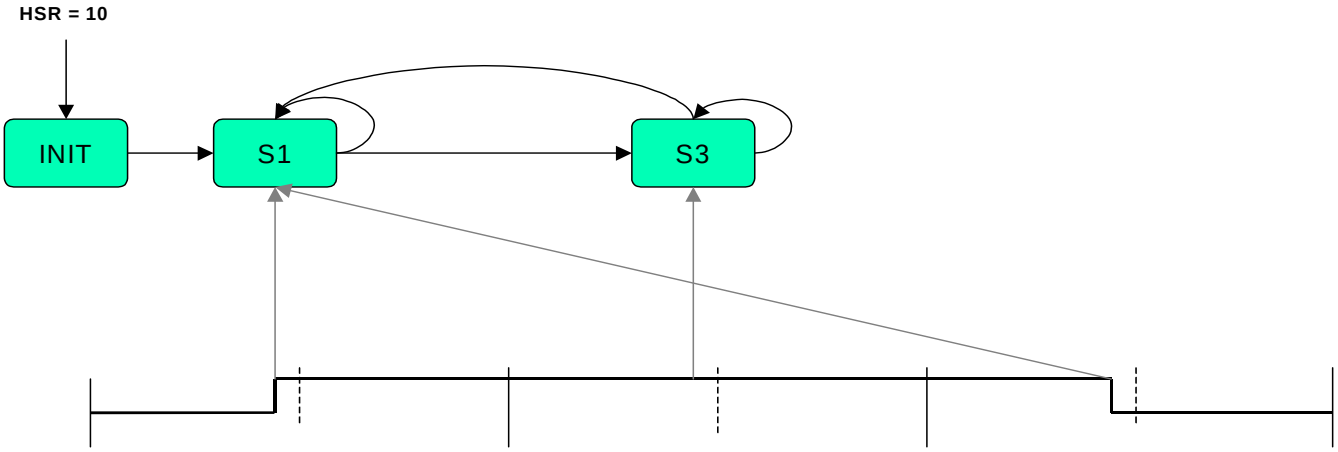

Figure 16. BLDC_res state diagram

Fault Input for BLDC Motor (BLDC_fault)

The BLDC_fault is an input TPU function that monitors the pin, and if a high to low transition occurs, immediately sets all PWM channels low and cancels all further transitions on them. The PWM channels, as well as the synchronization and resolver reference signal channels (if used), have to be initialized again to start them running.

The function returns the actual pinstate as a value of 0 (low) or 1 (high) in the parameter *fault_pinstate*. The parameter is placed on the Q1 PWM channel to keep the fault channel parameter space free.

Host Interface

Written By CPU
Written by both CPU and TPU
Written By TPU
Not Used

Table 26. BLDC_fault Control Bits

Name	Options
3 2 1 0 Channel Function Select	BLDC_fault function number (Assigned during assembly the DPTRAM code from library TPU functions)
1 0 Channel Priority	00 – Channel Disabled 01 – Low Priority 10 – Middle Priority 11 – High Priority

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Table 26. BLDC_fault Control Bits

Name	Options
1 0 Host Service Bits (HSR)	00 – No Host Service Request 01 – Not used 10 – Initialization 11 – Not used
1 0 Host Sequence Bits (HSQ)	xx – Not used
0 Channel Interrupt Enable	0 – Channel Interrupt Disabled 1 – Channel Interrupt Enabled
0 Channel Interrupt Status	0 – Interrupt Not Asserted 1 – Interrupt Asserted

TPU function BLDC_fault generates an interrupt when a high to low transition appears.

Table 27. BLDC_fault Parameter RAM

Channel	Parameter	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fault input	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7																

Table 28. BLDC_fault parameter description

Parameter	Format	Description
Parameters written by TPU		
fault_pinstate	0 or 1	State of fault pin: 0 ... low 1 ... high

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Performance

Table 29. BLDC_fault State Statistics

State	Max IMB Clock Cycles	RAM Accesses by TPU
INIT	8	2
FAULT	44	1
NO_FAULT	4	1

NOTE: *Execution times do not include the time slot transition time (TST = 10 or 14 IMB clocks)*

Figure 17. BLDC_fault timing

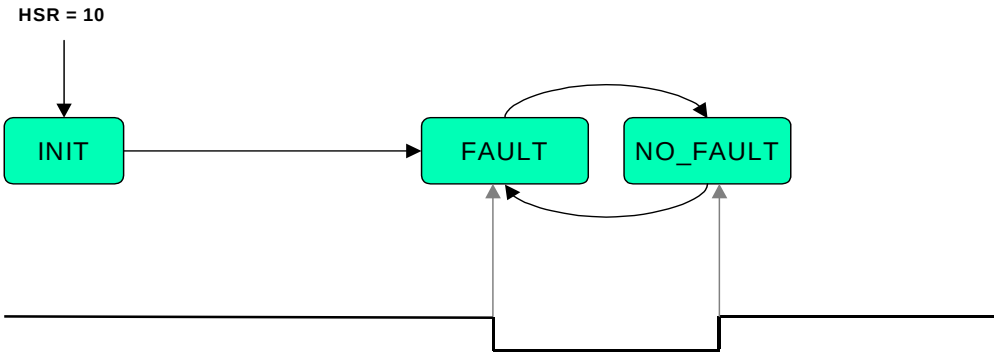

Figure 18. BLDC_fault state diagram

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