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Migrating from the M•CORE MMC2107 to the MMC2114

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This document describes design and programming considerations to address when migrating from the MMC2107 to the MMC2114. There are a number of advantages for current MMC2107 customers to make the move to the MMC2114. This document highlights these advantages and provides a checklist for those differences, both in hardware and in code, that the user needs to be aware of when substituting the MMC2114 for the MMC2107. Because the MMC2107 and MMC2114 are members of the same family of M•CORE microcontrollers, the CPU and all on-chip modules are nearly identical on the two devices.

Table 1 summarizes the design considerations when migrating from the MMC2107 to the MMC2114.

Table 1. MMC2107 to MMC2114 Migration Issue Summary

Device Feature	Device Implementation		Impact		Migration Criticality	Section/Page
	MMC2107	MMC2114	Hardware	Code		
Flash Type	CMFR	SGFM		√	Medium	1.1.1/p. 2
Flash Size	128K	256K		√	Low	1.1.2/p. 3
Flash Enable during Chip Configuration	Yes	No	√		Low	1.2.1.3/p. 4
Flash Security	No	Yes		√	Low	1.2.1.4/p. 5
Flash Interrupts	0	2		√	Low	1.3.1.3/p. 8
Flash Access Time	1-2 cycles	1 cycle		√	Low	1.3.2.2/p. 12
SRAM Size	8K	32K		√	Low	1.1.3/p. 3
LVD Interrupt/Reset	No	Yes	√	√	Low	1.3.1.2/p. 6
5V-tolerant Inputs	No	Yes	√		Medium	1.2.1.5/p. 5
Package Types	100- & 144-pin LQFP	100- & 144-pin, 196-ball MAPBGA	√		Low	1.1.6/p. 3
V_{PP} pin/supply	Yes	No	√		Medium	1.2.1.1/p. 4
V_{DDSYN} pin/supply	Yes	No (PLLEN input)	√		Medium	1.2.1.2/p. 4
QADC Port QB	Input Only	I/O	√	√	Medium	1.2.1.6/p. 5
QADC Prescalar	Complicated	Simplified		√	Medium	1.3.1.8/p. 11
QADC Register Access	5-6 cycles	3-4 cycles		√	Low	1.3.1.8/p. 11

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Table 1. MMC2107 to MMC2114 Migration Issue Summary (continued)

Device Feature	Device Implementation		Impact		Migration Criticality	Section/Page
	MMC2107	**MMC2114**	**Hardware**	**Code**		
Stop Mode Current	10uA	150uA	√		Medium	1.2.2.1/p. 5
Bus Timing	Good	Better	√		Low	1.3.2.3/p. 12
Chip ID	$1700	$1E00		√	None	1.3.1.1/p. 6
Port Read when Primary Function Active	Yes	No		√	Low	1.3.1.6/p. 10
Timer Limitations during OC	Yes	No		√	Low	1.3.1.7/p. 11
JTAG/OnCE Bugs	Yes	No			None	1.3.1.9/p. 12
OnCE Security Bypass	No	Yes			None	1.3.1.9/p. 12

1.1 MMC2107/MMC2114 Comparison Overview

The major feature differences between these two family members are described in the following sections.

1.1.1 Improved Flash

The MMC2114 uses Second Generation Flash for M•CORE (SGFM), which has distinct advantages over the MMC2107's CDR MoneT Flash (CMFR) technology as follows:

- SGFM does not require any externally applied programming voltage. CMFR requires 5V+/-5% applied to V_{PP} during Flash programming or erasing. Also, there is no restriction on the SGFM power supply voltage (V_{DDF}) during programming/erasing other than meeting the device V_{DD} requirements. For CMFR, it is necessary to maintain V_{DDF} at 3.3V+/-5% during Flash programming or erasing.

- The SGFM programming and erasing algorithms are much simpler than those of CMFR, and overall programming time is substantially shorter for SGFM.

- SGFM offers a sophisticated security feature, which ensures that unauthorized access to code resident in internal Flash cannot occur.

- SGFM offers a three-way protection scheme. Each 8K sector of Flash has its own protection settings for program and erase access, unlimited versus supervisor mode access, and data versus data and program use. These protection settings are initialized based on Flash configuration settings programmed in Flash, but can be overridden by writing to each of the three protection registers. For more details see Section 10.7.2, "Banked Register Descriptions," in the *MMC2114 Advance Information Manual* (order number: MMC2114/D).

- SGFM has a much higher endurance than that of CMFR. While CMFR allows up to 100 program/erase cycles for each block in the array, SGFM specifies 1000 program/erase cycles for each page over the entire array. Data retention for the two types of Flash is the same at 10 years.

1.1.2 Flash Size

The MMC2114 has twice as much Flash as that found in the MMC2107. The 256 Kbytes of the MMC2114's Flash is organized as two separate 128K arrays, which allows execution of code in one array to program the other array.

1.1.3 More Static Random-Access Memory (SRAM)

The MMC2114 has four times more SRAM than the MMC2107. The 32K of SRAM in the MMC2114 allows for a greater amount of concurrent data storage and room for more stack space.

1.1.4 LVD Circuit

The MMC2114 offers a low-voltage detection (LVD) monitor, which, upon the sensing of a low-voltage V_{DD} state, allows the central processor unit (CPU) to either cause an interrupt from normal program flow and take appropriate action, or reset the device.

1.1.5 5V-tolerant Inputs

The digital input/output (I/O) ports on the MMC2114 have been made more flexible by allowing up to 5 volts to be applied to all pins configured as inputs without danger of damage to the port or to the device. The oscillator or crystal input pin, EXTAL, is not included in this group of 5V-tolerant input pins, and requires an oscillator input voltage no greater than V_{DD}.

1.1.6 New Package

Along with the 100- and 144-pin low-profile quad flat pack (LQFP) packages offered for the MMC2107, the MMC2114 is also offered in a very compact 196-ball plastic mold array process ball grid array (MAPBGA). This package has the same pinout features as those in the 144-pin LQFP.

This application note highlights the relatively minor differences, and specifies what needs to be done with existing designs to allow the replacement of the MMC2107 by the MMC2114.

1.2 Hardware Considerations

This section enumerates the hardware differences between the two devices, focuses on the pinout for each package, and discusses performance issues that need to be considered when replacing the MMC2107 with the MMC2114. The voltage range for the various common supplies – V_{DD}, V_{DDH}, V_{DDA} and V_{STBY} – are the same for the two devices. Two supplies, V_{PP} and V_{DDSYN}, are not required for the MMC2114 as they are for the MMC2107. This is discussed below. Also, the system operating frequency range and reference frequency range for these two devices are identical.

1.2.1 Package Pinouts

The 100-pin LQFP package MMC2114 is a drop-in replacement for the 100-pin LQFP package MMC2107, and similarly the 144-pin LQFP package MMC2114 is a drop-in replacement for the 144-pin LQFP package MMC2107. No changes are absolutely necessary, but some changes can be made to reduce the overall cost of a target system or to benefit from the enhancements that the MMC2114 offers. These changes are discussed in the following sections.

1.2.1.1 V_{PP} Pin

Since the MMC2114's Flash does not require any external programming voltage, the 5-volt power to the V_{PP} pin can be removed and the pin may be left unterminated. In fact, if there is no other 5-volt requirement in the system, then this power supply can be disabled or removed from the system. Keep in mind that if the Queued Analog-to-Digital Converter (QADC) module is used, then a 5-volt supply is needed on its power input, V_{DDA}. Note that the QADC module will operate at 3.3V, but its accuracy is not guaranteed. Also, if the QADC port is being used as a 5-volt I/O port, then 5 volts is needed on the V_{DDH} supply pin, and V_{DDA} and V_{DDH} must always be within 1 volt of each other. See Table 2 for pinout differences between the MMC2107 and the MMC2114.

Table 2. Pinout Differences between the MMC2107 and the MMC2114

Pin Number			Device	
144-Pin Package	100-Pin Package	MAPBGA Package [1]	MMC2114	MMC2107
87	59	J13	No Connect	V_{PP}
123	85	D8	PLLEN	V_{DDSYN}
126	88	-	V_{SS}	V_{SSSYN}

[1]   MAPBGA package only available for the MMC2114

1.2.1.2 V_{DDSYN}

The MMC2107 requires a filtered supply for the phase-locked loop (PLL) of the internal clock module. This V_{DDSYN} power supply is not needed for the MMC2114 as its PLL is powered by V_{DD}. This pin, which is called PLLEN on the MMC2114, serves the purpose of clock mode selection during chip configuration, just as the V_{DDSYN} pin does on the MMC2107. That is, when the $\overline{RCON}$ pin is asserted during reset, the states of several data bus pins, plus the V_{DDSYN}/PLLEN pin, determine how the chip is configured for operation, including the clocking mode. The only difference in how clock mode is specified for the MMC2114 is that this PLLEN pin need only be a standard digital input, read during chip configuration, instead of being derived from a power supply. So to enable the internal PLL during chip configuration, PLLEN needs to be a high input, and data pins D23 and D22 still need to be set to specify either 1:1 PLL mode, normal PLL mode with a crystal reference, or normal PLL mode with an external clock reference. PLLEN should remain driven at this configuration state at all times during operation. For existing designs, the V_{DDSYN} power supply can still be used and applied to the PLLEN pin to specify PLL operation during chip configuration. Or to save cost, the special power supply or filtering components for V_{DDSYN} can be eliminated, and a non-filtered digital input signal can be applied to this pin. See Section 4 of the *MMC2114 Advance Information Manual* for more information about chip configuration.

1.2.1.3 D28 during Chip Configuration

Another simplification to chip configuration for the MMC2114 is realized as a result of the low power requirement of the SGFM. Because of the very low power that this Flash consumes when not being accessed, there is no need to disable it when it is not used. It is always in an enabled state when the device is running, and there is no configuration option to disable it. Therefore data pin D28 does not need to be driven during chip configuration, as is the case for the MMC2107. D28 can still be driven during the MMC2114's chip configuration, but it has no effect.

1.2.1.4   Security Implementation

Flash security is implemented on the MMC2114, which also has an impact on chip configuration. This security, when set, prevents unauthorized access to the SGFM and its contents. As a condition of security, the device must be operating in single-chip mode and, in fact, operation in any other mode is disabled. When security is set, the device is therefore forced into single chip mode, 32-bit data port size and internal boot regardless of the RCON pin configuration. Other RCON configuration settings, such as output drive strength and clock mode, are implemented as dictated by the chip configuration pin states. Security for the MMC2114's SGFM is discussed in great detail in Appendix A of the *MMC2114 Advance Information Manual*.

1.2.1.5   5 Volt-tolerant Inputs

Because the MMC2114's digital inputs are 5-volt-tolerant, no input protection or level translation is necessary when applying 5 volts to these inputs. Existing components used for this purpose can be removed from the target system, or they may remain if their cost is not an issue. Note that the oscillator or crystal input pin, EXTAL, is not included in this group of 5V-tolerant input pins, and requires an oscillator input voltage no greater than V_{DD}.

1.2.1.6   Port QB Pins

An enhancement to the Queued Analog-to-Digital Converter (QADC) Module was done for the MMC2114, which allows the Port QB pins to be configured as either inputs or outputs. For the MMC2107 these pins could only be configured as inputs. This allows for 4 more pins to be driven at V_{DDA}/V_{DDH} potential when these pins are not being used as analog inputs. These pins are configured by default as inputs, so for MMC2107 migrations, nothing needs to be done to the Port QB data direction register to retain compatibility with the existing design. Be aware that if the port A data direction register is being set with a 16-bit write in the application, then the port B data direction register may inadvertently be written, as these two 8-bit registers share the same 16-bit half-word in the register map. See Section 19.8.4 of the *MMC2114 Advance Information Manual* for Port QB configuration.

1.2.2   Performance Differences

1.2.2.1   Power Requirements

There are no differences from the MMC2107 in supply voltage, system operating frequency or temperature ranges within which the MMC2114 may operate. Because of the different processes, however, there are differences in the amount of power that the two devices consume, but these differences are fairly small. See Section 23.7 of the *MMC2114 Advance Information Manual* for more information on power supply current.

1.2.2.2   Bus Timing Differences

The MMC2114 has a difference in emulation mode in the way transfer acknowledge (TA) works. In this mode for the MMC2107, the Flash module asserts TA after an access even though the access is external (to the Flash emulation memory). This is done to keep the number of wait states consistent between internal and emulated memory. Because a different type of Flash is used on the MMC2114, the external memory or chip select must assert TA after an access to terminate the cycle. This difference is not seen in master mode, and therefore should not be an issue with migration.

There are also some minor external interface timing improvements for the MMC2114. These improvements should not impact existing MMC2107 interface designs, and these designs can be used without change for

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the MMC2114. For comprehensive interface timing specifications, see Section 23.11 of the *MMC2114 Advance Information Manual*.

1.2.3 Other Hardware Considerations

An additional hardware consideration when migrating to the MMC2114 relates to the low-voltage detection feature of this device. This feature supports the monitoring of V_{DD} and can be made to cause either an interrupt or a reset upon detection of a low supply-voltage state. If a MMC2107 design that is being migrated to the MMC2114 implements this function with an off-chip supervisor device, it may be advantageous to eliminate the device from the new design and use the functionality that the MMC2114 provides to monitor the supply voltage.

1.3 Software Considerations

This section deals with potential code incompatibilities when migrating MMC2107 code to run on the MMC2114. Since these two devices are within the same family and share the same CPU, there are no instruction-set, addressing, operating mode, or CPU register/mode differences. The following sections detail code issues on a module-by-module basis that the user needs to know to make a smooth transition from using the MMC2107 to the MMC2114.

1.3.1 Module Port/Register Differences

1.3.1.1 Chip Configuration Module

From a software perspective, the only difference between the MMC2107 and the MMC2114 in this module is the value of the read-only Chip Identification Register. For the MMC2114, this identification number is $1E00, where the MMC2107's value is $1700. All other registers have the same functionalities and default/read values. It should be reiterated here, however, that chip configuration has changed slightly for the MMC2114. D28, which controls the enabling of the internal Flash for the MMC2107, serves no function during chip configuration for the MMC2114. The MMC2114's SGFM Flash is always on when the device is powered. Also, the V_{DDSYN} pin, which is used to set the clock mode and serves to enable the internal PLL during chip configuration, has been renamed to PLLEN in the MMC2114 and serves the same function. After chip configuration, the PLLEN pin should be maintained at the same level at all times. This application of voltage is consistent with the MMC2107's V_{DDSYN} pin, which also serves as the PLL's power supply in the MMC2107.

1.3.1.2 Reset Controller Module

A low voltage detection circuit was incorporated into the MMC2114, which monitors the level of V_{DD} and can be configured to cause either an interrupt or a reset upon detection of a low supply-voltage state. The control of this feature has been placed in the Reset Control Register (RCR). Also, the read-only Reset Status Register (RSR), which specifies the cause of the last reset, has been modified to support this source of reset. The MMC2114's RCR has five additional bits that serve the following functions:

- The low-voltage detect enable (LVDE) bit enables/disables low voltage detection. This bit is set and this function is enabled by default.

- The low-voltage detect stop enable (LVDSE) bit enables/disables low voltage detection in stop mode. This bit is set and this function is enabled by default.

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NOTE

When the LVDSE bit is set and the device enters stop mode, additional power is consumed to keep this low-voltage detect circuit running. The internal voltage regulator is also left running and this also adds to the additional power.

- The low-voltage detect reset enable (LVDRE) bit enables/disables resets caused by low-voltage detection. This bit is set and this function is enabled by default. A reset caused by low-voltage detection when the LVDRE bit is set is reflected by the setting of the LVD bit in the RSR after the reset.

- The low-voltage detect interrupt enable (LVDIE) bit enables/disables interrupts caused by low-voltage detection. This bit is clear and this function is disabled by default. Interrupts caused by low-voltage detection when the LVDIE bit is set are serviced in the LVD interrupt service routine (ISR), which shares an interrupt vector with INT0 of the EDGE Port module. Both of these two interrupt sources are numbered 32 and proper arbitration needs to be conducted in the shared ISR to determine the source of the interrupt if both of these interrupts are enabled.

- The low-voltage detect flag (LVDF) bit is set when the LVDE bit is set and a low-voltage state is detected. The setting of this flag may trigger an interrupt when the LVDIE bit is set, or may trigger a reset if the LVDRE bit is set. The initial state of this bit is determined by the cause of the last reset. If the last reset was LVD-triggered, then this bit will be set after reset. This flag is cleared by writing a one to this bit if the LVD condition is no longer present.

The MMC2114's RSR has one additional bit than the RSR of the MMC2107. It's called the low-voltage detect (LVD) bit, and like the LVDF bit in the RCR, the initial state of this bit is determined by the cause of the last reset. If the last reset was LVD-triggered, then this bit will be set after reset. Unlike the LVDF bit in the RCR, writing to the LVD bit in the RSR has no effect. The LVD bit, and all other bits in the RSR, are read-only and cannot be modified in code.

A few points need to be made about the use of low voltage detection and stop mode. Entering stop mode with both LVDE and LVDSE set allows low-voltage detect and, when low voltage is detected, the programmed action (interrupt or reset) to take place. However, the cost of this functionality is higher current draw, about 90uA with LVD enabled, while in stop mode. The good news is that the oscillator circuit in the Clock Module does not need to be active (by setting STPMD[1:0] in the Synthesizer Control Register) to enable low-voltage detection in stop mode. So the 1mA needed to drive the oscillator circuit is not necessary for low-voltage detection during stop mode.

Designers need to give careful consideration when deciding the action taken upon low-voltage detection in stop mode. Setting the LVD to interrupt the CPU upon low-voltage detection to wake up out of stop mode may not be the best choice. Consider that it takes 200 microseconds for the PLL to go into lock after getting a clock, which could take in the tens of milliseconds for some crystals. If the voltage supply is collapsing fairly quickly, then with this delay coming out of stop to service the low-voltage interrupt, there may not be enough time to take any action before the supply voltage is too low to support the device. Also, the additional load on the power supply to support the device's run mode I_{DD} might hasten the power supply's degradation. To reduce this impact, it may be beneficial to have the PLL clock the device as slowly as practical, balancing the need to take action as quickly as possible, when coming out of stop until it is determined why it came out of stop. As a general rule, it's always a good idea to save all operational and recovery-critical parameters to non-volatile memory before entering stop mode.

Another consideration about the LVD and stop mode operation is that if low-voltage detection is enabled in run mode (LVDE set) but disabled in stop mode (LVDSE cleared), then a slightly longer wakeup time of about 100uS will occur when coming out of stop mode. This is required to allow the Power Management

Module (PMM) to restart the regulator when waking up. It holds off the wakeup signal to the PLL and the internal clocks until the regulator is running again. If either the oscillator/PLL or LVD is enabled in stop mode, then the PMM passes the wakeup signal right away and this additional delay does not occur.

See Section 5, "Reset Controller Module," of the *MMC2114 Advance Information Manual* for more details about low voltage detection and its two control and status registers.

1.3.1.3   Interrupt Controller Module

The Interrupt Controller Module of the MMC2114 differs from that of the MMC2107 only in the sources of interrupts. There are three additional sources of interrupts for the MMC2114. These three sources of interrupts share vectors with Edge Port interrupts such that the total effective number of interrupt sources remains at 40. One of these interrupt sources relates to low-voltage detection and has already been discussed. The other two interrupt sources relate to the MMC2114's SGFM and can be used when programming the Flash. One of these interrupt sources, the SGFM Buffer Empty interrupt is triggered when the Command Buffer Empty Interrupt Flag (CBEIF) in the (banked) SGFM User Status Register (SGFMUSTAT) is set, and the Command Buffer Empty Interrupt Enable (CBEIE) bit in the (unbanked) SGFM Configuration Register (SGFMCR) is set. The SGFM Buffer Empty interrupt is used during a Flash program or erase sequence and gives notification that the SGFM state machine is ready for a new command.

The second of the SGFM interrupts is called the SGFM Command Complete interrupt. This interrupt is enabled by setting the Command Complete Interrupt Enable (CCIE) bit in the SGFMCR, and is triggered when the Command Complete Interrupt Flag (CCIF) in the SGFMUSTAT is set. As its name implies, the setting of this bit signifies that the previously issued SGFM commands have completed and no commands are pending.

Both the SGFM Buffer Empty interrupt and the SGFM Command Complete interrupt share an interrupt vector and ISR with each other and with the Edge Port's INT0 interrupt. These interrupt sources are numbered 33 and proper arbitration needs to be conducted in the shared ISR to determine the source of the interrupt if two or more of these interrupt sources are enabled. See Sections 8.8.5 of the Interrupt Controller Module, and Sections 10.7.1 and 10.7.2 of the SGFM section of the *MMC2114 Advance Information Manual* for more details about these interrupts and their functions.

Table 3 shows the sharing of these three new interrupts with the existing Edge Port interrupts.

Table 3. New Interrupt Sources for the MMC2114

Source	Module	Flag	Source Description	Flag Clearing Mechanism
32	EPORT	EPF0	Edge Port Flag 0	Write EPF0 = 1
	PMM [1]	LVDF	LVD	Write LVDF = 1 [2]
33	EPORT	EPF1	Edge Port Flag 1	Write EPF1 = 1
	SGFM [3]	CBEIF	SGFM Buffer Empty	Write CBEIF = 1
	SGFM [3]	CCIF	SGFM Command Complete	CCIF cleared automatically

[1] Interrupt source 32 is shared by INT0 of the EPORT and low voltage detect (LVD) of the power management module (PMM), a sub-module of the reset mode.

[2] The LVDF can be cleared only if the low-voltage condition is no longer present.

[3] Interrupt source 33 is shared by INT1 of the EPORT and two interrupts from the second generation Flash for M•CORE (SGFM) module.

1.3.1.4   Static Random-Access Memory (SRAM) Module

The SRAM in the MMC2114, at 32Kbytes, is four times the size of the MMC2107's SRAM. For a direct migration from the MMC2107 to the MMC2114, there is no need for any program re-organization as the SRAM start address, 0x800000, is the same in the two devices. However, for those applications that might benefit from more heap or stack space, the additional 24K of SRAM in the MMC2114 may be utilized.

1.3.1.5   SGFM Flash Module

The biggest difference between the MMC2107 and the MMC2114 is the Flash technology. Operationally, though, the differences that might impact code migration are the following:

- The SGFM is configurable through a configuration field located in Flash
- The MMC2114 has 256Kbytes of storage, twice as much as the MMC2107
- The SGFM is programmed differently than the MMC2107's CMFR

The first difference, that of configurability of the SGFM, relates to a configuration field in the SGFM Flash module located at 0x0200–0x022b. This configuration field is composed of several sub-fields including:

- A four-byte security word which specifies whether the Flash is secured and whether it can be unsecured by back-door access
- An eight-byte key used for back-door access to the Flash when it has been secured and back-door access is enabled
- Four two-byte fields, one for each 128 Kbyte block-pair of Flash, which enables/disables programming/erasing for each of the sixteen 8 Kbyte sectors of Flash within the block-pair
- Four two-byte fields which sets each of the sectors for supervisor only or supervisor/user mode access
- Four two-byte fields which sets each of the sectors for data address space or data/program address space

Each of these fields gets copied into corresponding registers on the device upon reset, and settings for each of these protection and security modes become effective after reset. Two of the four sets of protection fields, relating to blocks 2 and 3 of the Flash, apply to Flash space which is not implemented on the MMC2114 and the values programmed into these fields do not matter. The values programmed into protection fields for block 0 and block 1 do matter and apply to the implemented Flash on the MMC2114.

As far as the configuration field values are concerned, programming all zeroes into this 44-byte field will result in complete operational compatibility with the MMC2107. By doing this, Flash security will be disabled and all of Flash will be set for unrestricted mode space, able to be programmed/erased and able to contain both data and program code. See the SGFM section and the security appendix in the *MMC2114 Advance Information Manual* for a more detailed description of the configuration field and all the registers of the SGFM Flash module.

Another reason for mentioning this configuration field, aside from notifying the reader that it exists and should be properly programmed, is that the presence of this field at this location in Flash might necessitate a change in program organization for code that is being ported from the MMC2107. That is, if the existing MMC2107 code is set to reside starting at location 0x200, it should be moved to a location after the configuration field. The code space should begin at or after 0x22c when running it on the MMC2114.

The second difference between the Flash modules on these two devices, that of Flash size, should not cause any migration issues since migration direction is toward the larger Flash. If anything, this will ease any optimization/compression requirements to get an application to fit into the available code space. The Flash start address, 0x00, is the same for the two devices.

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The third issue, regarding the difference in programming algorithm, will be a migration issue only for those applications where Flash re-programming is supported within the application. Fortunately for those applications, the program and erase algorithms for the SGFM is much simpler and easier to implement than the MMC2107's.

The SGFM command register supports four commands – program, page erase, mass (array) erase and (array) erase verify.

- The program command is used to program a single 4-byte (32-bit) word.
- The page erase command erases 1 Kbytes of Flash. Two 512-byte pages from interleaving physical blocks are erased in this operation.
- The mass erase command erases all 128 Kbytes of Flash from two interleaving physical blocks. A mass erase is only possible when no PROTECT bits are set for that block. The MMC2114 has two such 128 Kbyte arrays, so a full erase of Flash requires a mass erase of each of the two arrays.
- The erase verify command verifies that all 128 Kbytes of Flash from two interleaving physical blocks are erased. If both blocks are erased, the BLANK bit will set in the SGFMUSTAT register upon command completion.

A three-step command-write sequence is used to execute any of these four commands. No intermediate writes to the SGFM module are permitted between these three steps. The command write sequence is as follows.

1. Write the 32-bit word to be programmed to its location in the SGFM array. The address and data will be stored in internal buffers. All address bits are valid for program commands. The value of the data written for verify and erase commands is ignored. For mass erase or verify, the address can be any location in the SGFM array. For page erase, address bits [9:0] are ignored.

2. Write the program, erase, or verify command to SGFMCMD, the command buffer.

3. Launch the command by writing a 1 to the CBEIF flag. This will clear CBEIF. When command execution is complete, the Flash state machine will set the CCIF flag. The CBEIF flag will also be set again, indicating that the address, data, and command buffers are ready for a new command sequence to begin.

See the SGFM section in the *MMC2114 Advance Information Manual* for a description of all the registers available to access this Flash.

1.3.1.6 Ports Module

The only difference with the ports between the MMC2107 and the MMC2114 relates to the value read in the Port Pin Data/Set Data Register (PORTxP/SETx) when the port is configured for its primary function. For the MMC2107 reading this register reflects the value present at the port at the time, while a read of this register in the same configuration for the MMC2114 yields all lows. For example, if port C is configured as data lines D[15:8] as part of a 32-bit wide data port in master mode, the Port C/D Pin Assignment Register (PCDPAR) will reflect that these two ports are configured for primary function, or as data bus lines. In this configuration for the MMC2114, reading PORTCP/SETC will return all zeroes instead of the actual value of that byte of the data bus. If an existing MMC2107 application does not rely on reading the data bus in this manner, then this limitation should not be a consideration when migrating from the MMC2107 to the MMC2114.

1.3.1.7 Timer Modules

The timer in the MMC2107 has two limitations when doing output compares. These limitations are documented in the MMC2107's errata, file name MMC2107MSE1.PDF, accessible at the MMC2107 Product Summary page. A summary of the MMC2107 timer errata is shown below for convenience.

Two problems appear when the source of the counter clock is not the system clock with a prescalar of one (the default). This includes all other possible sources of the counter clock: system (with prescalar other than one), PACLK, PACLK/256, and PACLK/65536.

Problem 1: Enabling the TCRE causes the timer counter to reset to 0x000 when a channel 3 compare is made. When the timer counter reset enable (TCRE) bit is set, the counter stays at the channel 3 compare value for only one timer clock cycle and then it resets to 0x0000. The 0x0000 count is then one timer counter clock cycle short. (for example, three clocks for div 4). The net result is that a count is lost in the whole repeating loop.

Problem 2: The toggle-on-overflow (TOV) feature does not work for prescalars greater than one (the default). This problem exists for all channels of both timers in the MMC2107. The output compare value does in fact cause a toggle, but toggles for the same number of times as the divisor (for example, toggles twice for div2, four times for div4, etc). The TOV should always be disabled for prescalars larger than one to prevent unintentional edges from appearing.

These problems do not exist in the MMC2114. If the workaround for problem 1 (see errata) is implemented in a MMC2107 design and is carried over to the MMC2114, then it will need to be modified to NOT compensate for a lost timer clock count. The workaround for problem 2 can be carried over to the MMC2114 without change. For new MMC2114 designs, the primary effect of this correction means that output compares using toggle on overflow can be carried out on any channel when using any prescalar for the timer.

1.3.1.8 Queued Analog-to-Digital Converter (QADC) Module

Three major changes have been made to the QADC of which the user should be aware. One of these changes, which has already been mentioned, allows the configuration of Port QB to either inputs or outputs. This is the same configuration as Port QA is in the MMC2107 and MMC2114. Because of this selectability, the MMC2114's Port QB has a Data Direction Register. Port QB pins are configured by default as inputs, so nothing needs to be done to the Port QB data direction register to retain compatibility with migrated MMC2107 designs. See Section 19.8.4 in the QADC section for more details about the Port QB Data Direction Register.

Another change to the QADC module affects the way the QADC's clock rate is set up. The Prescalar Clock Divider Field (QPR[6:0]) in the QADC Control Register 0 (QADC0) has been changed in the MMC2114 to simplify the QADC clock frequency (f_{QCLK}) setup. To program this field for a particular f_{QCLK} based on a known system frequency (f_{SYS}), the formula is given as:

$$QPR[6:0] = f_{SYS}/f_{QCLK} - 1, \text{ where } 1 <= QPR[6:0] <= 127.$$

If QPR[6:0] = 0, then the QPR register field value is interpreted as a 1. See Section 19.8.1.5 in the *MMC2114 Advance Information Manual* for more information about the setting of the QADC clock setting.

The last change to the QADC module does not impact the coding directly, but could have a minor impact on application timing when accessing QADC registers. In the MMC2114, accesses to the QADC registers are 2 cycles faster than in the MMC2107. It takes 5-6 clocks for a QADC register access for the MMC2107, depending on activity in the queue. It takes 3-4 cycles for QADC register access for the MMC2114.

1.3.1.9 JTAG Test Access Port and OnCE

There are a number of errata listed for the OnCE port and debug operation in the MMC2107's errata, file name MMC2107MSE1.PDF, accessible at the MMC2107 Product Summary page. All of these errata have been corrected in the MMC2114. Since OnCE port operation does not have a direct bearing on normal device operation, details of these changes are outside the scope of this document. No design changes are needed because of these changes when migrating from the MMC2107 to the MMC2114.

One change to OnCE operation relates to SGFM security. The MMC2114's OnCE Module supports a command called LOCKOUT_RECOVERY, which allows a secured device to be accessed. The command opcode is 11 (decimal), and issuance and execution of this command causes the entire SGFM Flash array to be erased including the Flash security word at $228-$22B. After the erase operation, the device can be accessed.

1.3.2 Access Time Differences

1.3.2.1 Static Random-Access Memory (SRAM) Module

Timing for SRAM accesses is the same for the MMC2107 and the MMC2114. No code changes are necessary to normalize execution time between the two devices with respect to SRAM accesses.

1.3.2.2 SGFM Flash Module

All SGFM Flash accesses are single cycle on the MMC2114, and could therefore allow a slight decrease in overall Flash execution time. The read operation for SGFM Flash differs from the MMC2107's CMFR Flash in that a MMC2107 read operation normally takes one cycle, but takes two cycles when a read falls outside the 32-byte read page buffer and the buffer needs to be reloaded. Although this timing difference is relatively small, the user should keep this in mind especially in applications where specific activity is not timed or externally triggered.

1.3.2.3 External Bus Interface (EBI) and Chip-Select (CS) Modules

Although bus timing has improved on the MMC2114, there should be no impact on code migration with respect to execution time or the need to change the number of wait states for the chip selects. No MMC2114 timing parameter is worse than that for the MMC2107.

1.3.3 Low-level Device Driver Differences

A device-specific device driver library has been created for the MMC2114, which should be used when migrating from a MMC2107 design that utilizes the MMC2107's device driver library. Most of the MMC2114's low-level drivers are unchanged from those of the MMC2107, but some have been changed to reflect the changes in the modules described herein. In particular, new SGFM Flash programming drivers have replaced the CMFR drivers in the MMC2107's device driver library. The MMC2114 drivers and documentation can be downloaded from the MMC2114 Product Summary page.

1.4 Summary

Great care has been taken with the MMC2114 design to make the migration from the MMC2107 as simple as possible. For those applications that may take advantage of the additional or improved features that the MMC2114 offers, the few design changes required to make the migrations should be well worth the effort.

Freescale Semiconductor, Inc.

Migrating from the M•CORE MMC2107 to the MMC2114

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