PowerPC™

Application Note

Special considerations when implementing an ISDN BRI and a Ethernet port on the MPC850DH

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Below is the system architecture of an ISDN BRI to Ethernet router application using the MPC850DH. There are some special considerations discussed below for building an ISDN to Ethernet router.

Note: This document is preliminary status because not all aspects have been tested to date.

System Block Diagram

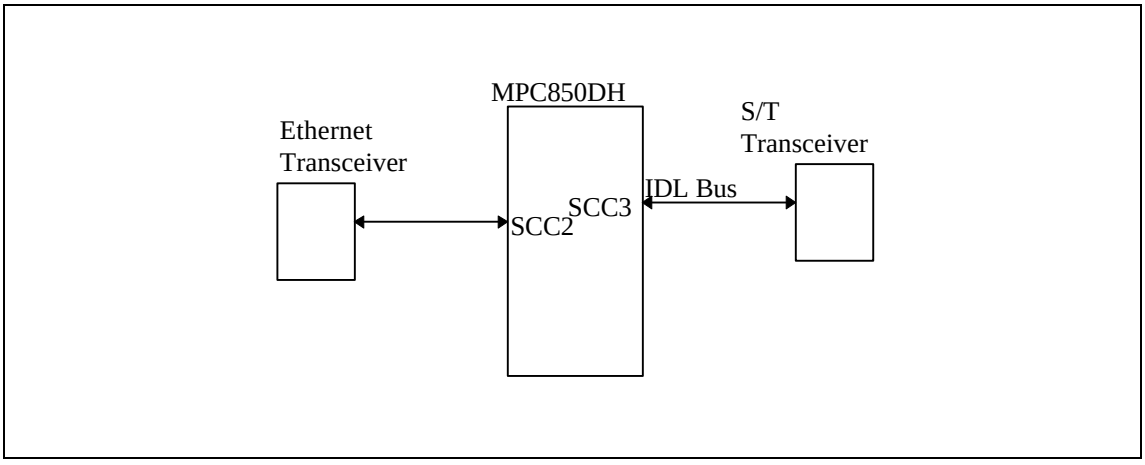

Figure 1: General Block Diagram

1. Using the QMC feature to implement a BRI on a single SCC.

1. The QMC mode is necessary implement the 3 channels of the BRI while only using a single SCC. The figure below shows how the data flows from the IDL interface through the SCC into memory. The Serial interface TSA is programmed to send the all three channels to SCC3. SCC3 in QMC mode has its own TSA which is programmed to route the BRI into the B or D channels which are routed to their own individual data buffers. Please refer to the QMC User's Manual (QMCSUPPLEMENT/AD) for details on the QMC controller setup.

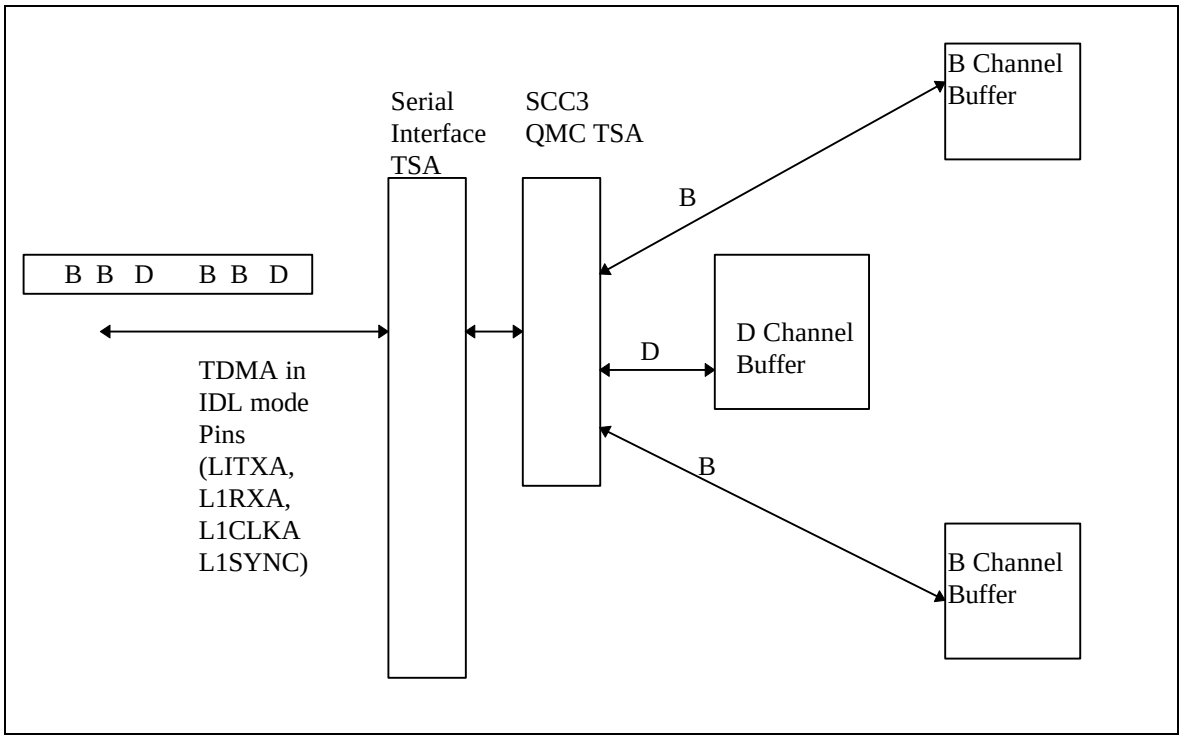

Figure 2: Data Flow

The figure below shows the recommended pin connections between the MPC850DH and the MC145574 S/T transceiver. The 850 to data transceiver interface is configured in IDL mode, and the SPI is used to communicate with the transceiver internal registers.

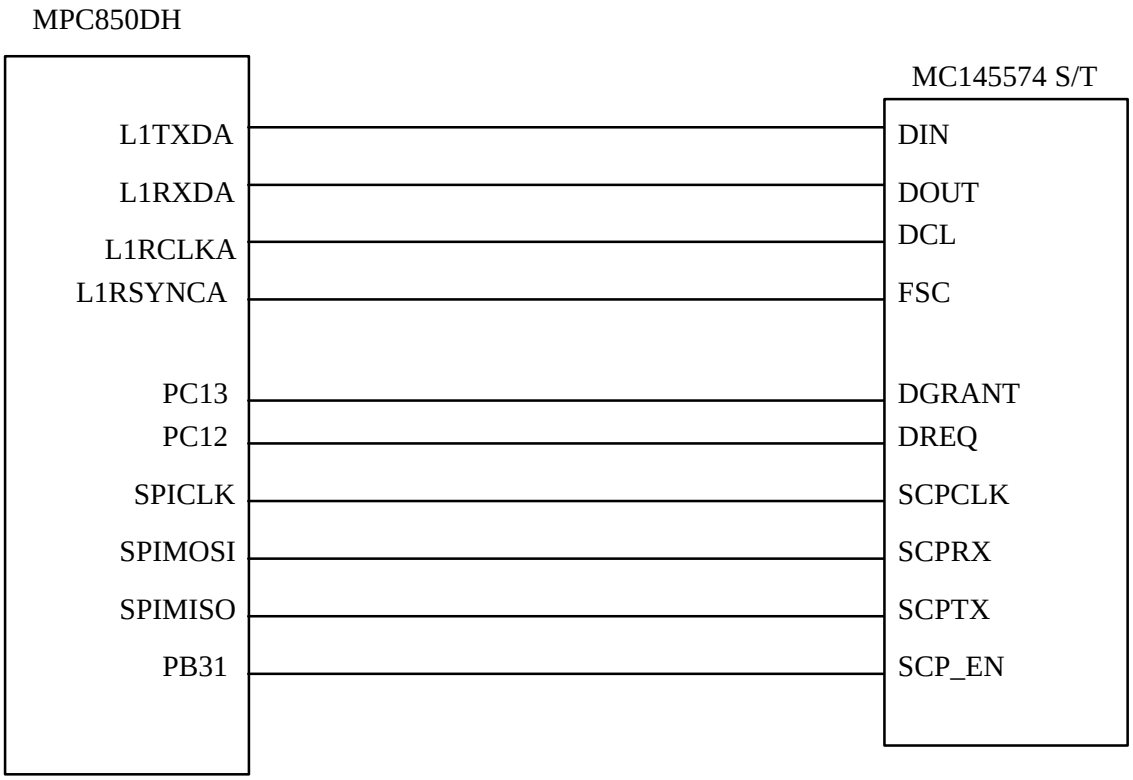

Figure 3: MCP850DH to Transceiver chip connections

2. Implementing D Channel collision on the MC145574 S/T transceiver using software control of PIO pins

The 850DH only has only two SCCs. In an ISDN to ethernet router application, one SCC will be required for ethernet and leaving only one for the BRI. With the use of the QMC mode which allows multiple HDLC or transparent channels to be implemented on a single SCC, an ISDN BRI with three channels (2B+D) can be implemented with a single SCC. In fact, multiple BRIs can be implemented with a single SCC. If the requirement for D channel collision detection and retransmission is added, then it becomes necessary to implement a software algorithm executed on the PPC host processor to detect the collision and retransmit the D Channel frame. It can be implemented in software, and two general purpose IO pins as follows.

Note: Only one MC145574 S/T transceiver can be supported with collision detection because the MC145574 must be in master mode to support D-channel collision.

L1REQ and L1GNT are implemented on 850 PIO pins, L1GNT should be assigned a PIO input pin with interrupt capability; PC13 was chosen for this recommendation because port C pins are interruptable and can be configured to interupt on both the rising and falling edges. The S/T chip can also be programmed to issue an interrupt on collision, so you could connect the S/T IRQ pin to another interruptable input but we will use L1GRNT for this application note.

When there is a frame to transmit:

1. The S/W should assert L1REQ and wait for L1GNT to be asserted by the transceiver (noticed by an interrupt arriving on the PIO input pin).
2. Start transmitting the frame. See QMC user's manual (QMCSUPPLEMENT/AD) for details on the QMC controller setup.
3. When L1GNT is negated - indicating a collision on the S/T bus - L1REQ should be negated by S/W.
4. Next a STOP TRANSMIT command should be issued to the QMC channel assigned to the D channel.
5. Then wait for the SCC FIFO to clear of the D channel data that has already been sent by the CP. This will be a 500uSec for a 16 byte FIFO SCC2 and 5 QMC channels. Since the minimum frame length is 7 bytes minus 2 bytes address, 1 byte control, 2 bytes CRC, 1 byte flag, 1 byte "high", and we can assume that the collision is on the address portion of the frame, we have 5 bytes which is 2.5 msec. This is plenty of time to allow S/W to negate L1REQ pin, issue the STOP transmit command and allow the the FIFO to clear.
6. While waiting for the FIFO to clear, set up the transmit buffer descriptor to retransmit the D channel frame.
7. Wait for the L1GNT to be reasserted by the transceiver.
8. Re-issue the START TRANSMIT command to attempt to transmit the frame again.

3. Special RAM Microcode needed to relocate the SPI and SMC buffer space

The SPI and SMC normally use dual port RAM memory space which is need by SCC2 in ethernet mode and SCC3 in QMC mode respectively. There is a which will remap the SPI and the SMC to unused portions of dual ported RAM to retain their functionality while running ethernet and QMC mode. Contact your sales office or field engineer for this microcode.

The microcode will use up both blocks of daul port RAM designated as RAM microcode areas so this space cannot be used for QMC parameters.