Application Note

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Checklist for Converting from Pre-RevD Silicon for the MPC860 Family

This document includes changes and additions to the MPC860 Rev. D design specifications. These changes must be taken into account when migrating from MPC860 Rev. C and earlier silicon (Rev. B and earlier silicon for the MPC860T) to the MPC860 Rev. D.3/D.4.

Chapter and section numbers in this document refer to the MPC860T Rev. D supplement.

Note that although most changes reflect additional functionality, the following two changes affect previously defined functionality and must be taken into account for proper operation:

- Section 4.1. The changes to the Port D pin multiplexing scheme.
- Section 6.2.8 . The addition of the FEC_PINMUX bit to the ECNTRL register.

These changes are marked as **Important**.

4.1 **Important.** Replace Table 4-1 with the following:

Table 4-1. Port D Pin Assignments [1]

Signal	Signal Function					
	PDPAR = 0	PDPAR=1, UT=0		PDPAR=1, PDDIR=0		Input to On-Chip Peripherals
		PDDIR=0	PDDIR=1	UT=1	UT=0	
PD15	PORT D15	L1TSYNCA	MII-RXD3 (I)	UTPB[0]	L1TSYNCA	L1TSYNCA=GND
PD14	PORT D14	L1RSYNCA	MII-RXD2 (I)	UTPB[1]	L1RSYNCA	L1RSYNCA=GND
PD13	PORT D13	L1TSYNCB	MII-RXD1 (I)	UTPB[2]	L1TSYNCB	L1TSYNCB=GND
PD12	PORT D12	L1RSYNCB	MII-MDC (O)	UTPB[3]	L1RSYNCB	L1RSYNCB=GND
PD11	PORT D11	RXD3	MII-TX-ERR (O)	$\overline{\text{RXEnb}}$	RXD3	RXD3 = GND
PD10	PORT D10	TXD3	MII-RXD0 (I)	$\overline{\text{TXEnb}}$	TXD3	—
PD9	PORT D9	RXD4	MII-TXD0 (O)	UTPClk	RXD4	RXD4 = GND
PD8	PORT D8	TXD4	MII-RX_CLK (I)	—	TXD4	—
PD7	PORT D7	RTS3	MII-RX-ERR(I)	UTPB[4]	RTS3	—
PD6	PORT D6	RTS4	MII-RXDV (I)	UTPB[5]	RTS4	—
PD5	PORT D5	REJECT2	MII-TXD3 (O)	UTPB[6]	REJECT2	$\overline{\text{REJECT2}}$=VDD
PD4	PORT D4	REJECT3	MII-TXD2 (O)	UTPB[7]	REJECT3	$\overline{\text{REJECT3}}$=VDD
PD3	PORT D3	REJECT4	MII-TXD1 (O)	SOC	REJECT4	$\overline{\text{REJECT4}}$=VDD

[1] Any UT and PDDIR bit combination not listed is reserved and should not be used.

4.1.2 **Important.** Add a third step (if MII is used) to enable MII mode as follows:

3. Set ECNTRL[FEC_PINMUX]; see Section 6.2.8.

6.2 Add the transmit watermark register to the X_WMRK at 0xEE4.

Table 6-1. FEC Parameter RAM Memory Map

Address	Mnemonic	Name
0xE00	ADDR_LOW	Lower 32-bits of our address
0xE04	ADDR_HIGH	Upper 16-bits of our address
0xE08	HASH_TABLE_HIGH	Upper 32-bits of hash table
0xE0C	HASH_TABLE_LOW	Lower 32-bits of hash table
0xE10	R_DES_START	Beginning of Recv descriptor ring
0xE14	X_DES_START	Pointer to beginning of xmit des ring
0xE18	R_BUFF_SIZE	Receive buffer size
0xE40	ECNTRL	Ethernet Control Register
0xE44	IEVENT	Interrupt Event Register
0xE48	IMASK	Interrupt Mask Register
0xE4C	IVEC	Interrupt Level and Vector Status
0xE50	R_DES_ACTIVE	Receive ring updated ag
0xE54	X_DES_ACTIVE	Transmit ring updated ag
0xE80	MII_DATA	MII data register
0xE84	MII_SPEED	MII Speed Register
0xECC	R_BOUND	End of RAM (read-only)
0xED0	R_FSTART	Receive FIFO start address
0xEE4	X_WMRK	Transmit Watermark
0xEEC	X_FSTART	Transmit FIFO start address
0xF34	FUN_CODE	Function code to SDMA
0xF44	R_CNTRL	Receive Control register
0xF48	R_HASH	Receive Hash register
0xF84	X_CNTRL	Transmit Control register

6.2.8 **Important.** Add the ECNTRL[FEC_PINMUX] bit to Figure 6-8 and Table 6-9.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
FIELD	SPARE													FEC_ PINMUX	ETHER_EN	RESET

Figure 6-8. ECNTRL Register

Table 6-9. ECNTRL Field Description

Bits	Name	Description
29	FEC_PINMUX	FEC enable. Read/write. The user must set this bit to enable the FEC function in the 860 in conjunction with 860 pin muxing control.

6.2.17 Add a new section here to describe X_WMRK.

The X_WMRK register, shown in Figure 6-17, is used to control the amount of data required in the transmit FIFO before transmission of a frame can begin. This allows the user to minimize transmit latency (X_WMRK = 0x) or allow larger bus access latency (X_WMRK = 11) due to contention for the system bus. Setting the watermark to a high value lowers the risk of a transmit FIFO underrun due to system bus contention.

X_WMRK is zero at reset.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	0000_0000_0000_0000															
BIT	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
FIELD	0000_0000_0000_00														X_WMRK	

Figure 6-17. X_WMRK Register

Table 6-19 provides the bit field descriptions for X_WMRK.

Table 6-19. X_WMRK Field Description

Bits	Name	Description
0–29	—	Reserved. Should be written to zero by the host processor.
30–31		Transmit FIFO watermark. Read/Write. Frame transmission begins when the number of bytes selected by this eld ha ve been written into the transmit FIFO or if an end of frame has been written to the FIFO or if the FIFO is full before the selected number of bytes have been written. 0x64 bytes written to the transmit FIFO 10128 bytes written to the transmit FIFO 11256 bytes written to the transmit FIFO

6.2.20 Update Figure 6-20 and Table 6-22 with bit 27, BC_REJ.

BIT	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
FIELD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BIT	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
FIELD	0	0	0	0	0	0	0	0	0	0	0	BC_REJ	PROM	MII_MODE	DRT	LOOP

Figure 6-20. R_CNTRL Register

Table 6-22. R_CNTRL Field Description

Bits	Name	Description
27	BC_REJ	Broadcast frame reject. Read/write. If set, frames with DA + 0xFFFF_FFFF_FFFF are rejected unless the PROM bit set. If both BC_REJ and PROM = 1, frames with broadcast DA are accepted and RxBD[M] is set.

6.2.21 In Table 6-23, replace the description of the MAX_FRAME_LENGTH with the following:

User read/write field. Resets to decimal 1518. Length is measured starting at DA and includes the CRC at the end of the frame. Transmit frames longer than MAX_FRAME_LENGTH cause an BABT interrupt. Receive frames longer than MAX_FRAME_LENGTH cause a BABR interrupt and set the LG bit in the end-of-frame BD. The recommended value to be programmed by the user is 1518 or 1522 (if VLAN tags are supported).

6.4.1 Replace this section with the following:

Ethernet Receive Buffer Descriptor (RxBD)

The RxBD is shown in Figure 6-23. The first word of the RxBD contains control and status bits. The user initializes RxBD[E,W] and the Rx buffer pointer. When the buffer has been accessed by a DMA, the FEC modifies RxBD[E,L,M,BC,MC,LG,NO,SH,CR,OV,TR] and writes the length of the used portion of the buffer in the first word. The FEC modifies RxBD[M,BC,MC,LG,NO,SH,CR,TR,OV] only if L is set.

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
+0	**E**	RO1	**W**	RO2	L	0	0	M	BC	MC	LG	NO	SH	CR	OV	TR
+2	DATA LENGTH															
+4	**RX BUFFER POINTER A[0–15]**															
+6	**RX BUFFER POINTER A[16–31]**															

Figure 6-23. Receive Buffer Descriptor (RxBD)

The RxBD format is shown in Table 6-27.

Table 6-27. Receive Buffer Descriptor (RxBD) Field Description

Bits	Name	Description
0	E	Empty. Written by the FEC and user. Note that if the software driver sets RxBD[E], it should then write to R_DES_ACTIVE. 0 The buffer associated with this BD is lled with receiv ed data, or reception was aborted due to an error. The status and length elds ha ve been updated as required. 1 The buffer associated with this BD is empty, or reception is in progress.
1	RO1	Receive software ownership bit. Software use. This read/write bit is modi ed b y hardware and does not affect hardware.
2	W	Wrap, written by user. 0 The next BD is found in the consecutive location 1 The next BD is found at the location de ned in RAM.R_DES_START.
3	RO2	Receive software ownership bit. Software use. This read/write bit is not modi ed b y hardware and does not affect hardware.
4	L	Last in frame, written by FEC. 0 The buffer is not the last in a frame. 1 The buffer is the last in a frame.
5–6	—	Reserved.

Table 6-27. Receive Buffer Descriptor (RxBD) Field Description (continued)

Bits	Name	Description
7	M	Miss, written by FEC.Set by the FEC for frames that were accepted in promiscuous mode but were agged as a miss b y the internal address recognition. Thus, while promiscuous mode is being used, the user can use the M bit to quickly determine whether the frame was destined to this station. This bit is valid only if both the L bit and PROM bit are set. 0 The frame was received because of an address recognition hit. 1 The frame was received because of promiscuous mode.
8	BC	Set if the DA is broadcast.
9	MC	Set if the DA is multicast and not broadcast.
10	LG	Rx frame length violation, written by FEC. The frame length exceeds the value of MAX_FRAME_LENGTH in the bytes. The hardware truncates frames exceeding 2047 bytes so as not to over o w receive buffers This bit is valid only if the L bit is set. (Note that the rst re vision of the MPC860T (mask #H56S) must not be given frames in excess of 2047 as it will not truncate frames.)
11	NO	Rx nonoctet-aligned frame, written by FEC. A frame that contained a number of bits not divisible by 8 was received and the CRC check that occurred at the preceding byte boundary generated an error. NO is valid only if the L bit is set. If this bit is set the CR bit is not set.
12	SH	Short frame, written by FEC. A frame length that was less than the minimum de ned f or this channel was recognized.Note that the MPC860T does not support SH, which is always zero.
13	CR	Rx CRC error, written by FEC. This frame contains a CRC error and is an integral number of octets in length. This bit is valid only if the L bit is set.
14	OV	Overrun, written by FEC. A receive FIFO overrun occurred during frame reception. If OV = 1, the other status bits, M, LG, NO, SH, CR, and CL lose their normal meaning and are cleared. This bit is valid only if the L bit is set.
15	TR	Truncate. Set if the receive frame is truncated (≥ 2 Kbytes).
Offset+2	Data length	Data length, written by FEC. Data length is the number of octets written by the FEC into this BD's buffer if L = 0 (the value = R_BUFF_SIZE), or the length of the frame including CRC if L = 1. It is written by the FEC once as the BD is closed.
Offset+4	Rx buffer pointer	Rx buffer pointer A[0–31], written by user. The receive buffer pointer, which always points to the rst location of the associated b uffer, must always be a multiple of 16. The buffer must reside in memory external to the FEC.

For any changes in the device errata, refer to the following documentation:

MPC860 Device Errata Summary (MPC860ERRSUM)

MPC860 Family Device Errata (MPC860ERREF)

Also refer to the following PCNs:

MPC855, MPC860 Product Change Notice—Transition to 860/855 (PCN 5808)

These documents are available for download from:

http://e-www.freescale.com

NOTE

Please note the new added errata effecting only rev D.x G10; restriction of open collector pull up. RAM microcode may need to be recompiled.

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