MPC860 and MC68302 Asynchronous Interface

The main point of this document is to show the flexibility of an asynchronous interface between an MPC860 and an MC68302. Wait states and or the external bus speed of the MPC860 can be adjusted to allow for interfacing the MPC860 and MC68302 at different bus speeds. For the purpose of this document, the following parameters are assumed:

- Interface is between a 40MHz MPC860 and a 20MHz MC68302.
- The MC68302 external master internal asynchronous read write timing is used (Please see Figures 6-17 and 6-18 of the *MC68302 User's Manual*).
- Transaction between the two chips is unidirectional. The MPC860 is the master and the 302 is the slave.
- MC68302 is a 16 bit port size that is defined as part of the upper data bus.
- MC68302 stores its serial data in its dual port RAM. It is not a bus master.
- The MPC860 user programmable machine (UPM) is programmed to generate the proper timing of the signals.
- General purpose lines available from the MPC860 UPM are not needed. Existing signals can be programmed to behave like signals received by the MC68302.

Programming the Option, Mode and Base Registers

The option and base registers of the MPC860 must be programmed as follows for this type of interface. Within the option register, bits 24 through 27 must be programmed according to the timing of the MC68302. Within the base register, bits 20 through 21, and bit 23 must be programmed for a 16 bit non-bursting port. The following tables have been appended from section 15 of the MPC860 Manual.

Table 15-14. Base Register

Bits	Mnemonic	Description	Function
20-21	PS(0:1)	**Port Size.** This field specifies the port size of the memory region.	10 = 16 bit port size
24-25	MS(0:1)	**Machine Select.** This field specifies the machine selected for the memory operations handling.	10 = U.P.M.A or 11 = U.P.M.B
31	V	**Valid Bit.** This bit indicates that the contents of the base register and option register pair are valid. The CS signal does not assert until the V bit is set. Note: An access to a region that does not have the V bit set may cause a bus monitor time out. Following a system reset, the V bit is set in BR0.	

Table 15-15. Option Register

Bits	Mnemonic	Description	Function
23	BI	**Burst Inhibit.** This attribute decides whether or not this memory bank supports burst accesses. In a non-burst case, the memory controller drives the BI signal active when accessing this memory region. Following a system reset, the BI bit is set in OR0.	1= Drive BI asserted. The bank does not support burst accesses.

Table 15-16. Machine A Mode Register

Bits	Mnemonic	Description	Function
8	PTAE	**Periodic Timer A Enable** This bit allows the periodic timer A to request service. Note: Following a system reset, the PTAE bit is reset.	0 = Periodic timer A is disabled

Programming the Signals for a Successful MPC860 and MC68302 Interface

For this interface, the MPC860 signals are programmed to communicate with the MC68302. With examination of the timing specifications and the number of wait states needed by the MC68302, the MPC860 can communicate successfully.

The active low MPC860 chip select signal is programmed to the MC68302 address strobe. The chip select's assertion can be interpreted as a MC68302 address strobe to emulate the MC68302 bus operation. Because you can program chip select like any other MPC860 signal, it makes programming the address strobe simple.

The active low signals BS[0] and BS[1] can be programmed for the upper and lower data strobe signals of the MC68302. These byte select signals are also convenient because they can be programmed using the user programmable machine like any other general purpose signal.

The read/write signal of the MPC860 can directly communicate with the same signal on the MC68302. The timing is not a problem since the read/write signal is asserted directly after the transfer start signal. BS[0] and BS[1] correspond with the byte lanes of the upper half of the data bus.

In Figure 1-1 the interface between the two parts is outlined. There are three three-state buffers. These buffers ensure that more than one device can drive the same line without creating bus contention (for five volt MC68302 parts only). However if a 3.3 volt MC68302 is used, the three-state buffers are not required. It is also important to note that a pull up resistor is connected to each signal keeping the lines high (unasserted) when there is no activity taking place. They should also be sized to meet the MC68302 negation times.

DTACK* and IAC signals are not used in this interface. DTACK* will be asserted internally by the MC68302 after a known number of wait states. IAC can be used as a debugging output to tell if the MC68302 is being selected. All that is needed for the

timing of the DTACK* signal is the cycle length. In order for a 40MHz MPC860 to interface with a MC68302 three wait states must be included in the timing. This will push the number of MPC860 clocks needed to complete the cycle to fourteen (2 x [3 wait states+ 4 clocks] = 14). This interface requires fourteen entries in the UPM RAM. Although only eight entries are available for single read or write operation, the additional burst read and write entries can be used in this application since neither are used. A loop function can also be used to reduce the number entries, but was not included in this application note for clarity. Knowledge of this cycle and the relative bus speeds of the MPC860 and MC68302 enables the user to program the length of the MPC860's read or write cycle appropriately.

The MC68302 SCC's store all data in the internal dual port RAM of the MC68302. This is appropriate for low speed serial channels on the order of 64 kbps or less. It is possible for the MC68302 to obtain bus mastership of the MPC860 bus, but this design is outside of the scope of this document.

A copy of the UPM programming for this interface is available in the MCUinit 860 tool.

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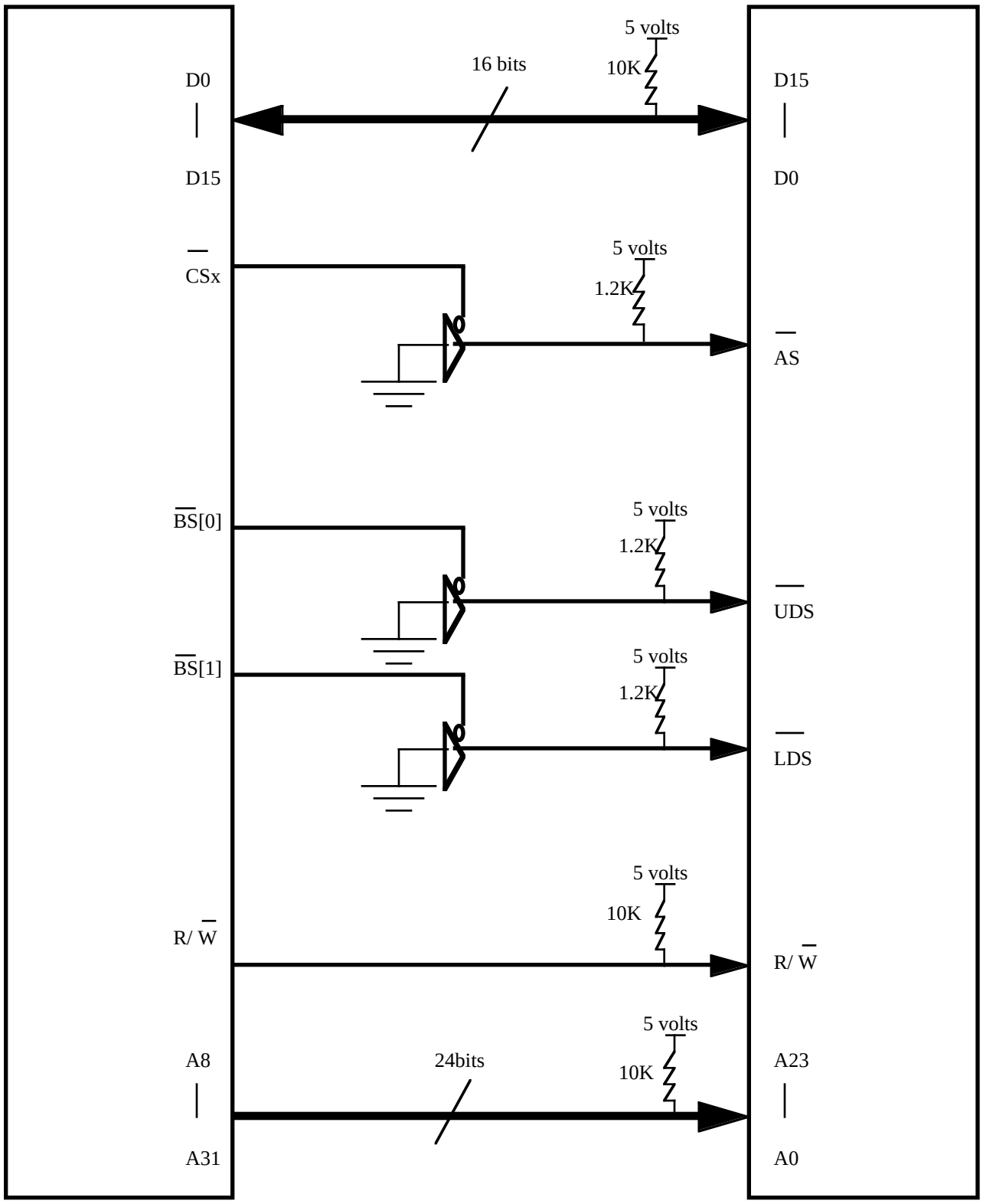

Figure 1. MPC860 — MC68302 Interface