Some Characteristics and Design Notes for Crystal Feedback Oscillators

1. Introduction

This note is written to assist engineers in the production of reliable clock circuits which may be used with devices such as the MPC860, MC68360 and MC68302 and their derivatives. All these devices offer more than one method for the generation of the system clock - the clock which is used throughout the chip. Differences exist between these highly integrated communications processors since they may or may not include a phase lock loop (PLL) stage incorporating a multiplier. When present, PLLs may be used to obtain higher frequencies than those created or input at the clock pins. This note is confined to discussion about basic clock generation excluding the PLL.

The basic clock pins are two, an input pin (EXTAL) and an output pin (XTAL). These pins connect to a digital inverter circuit (fig. 1) and it is important to note the inverter is ONLY defined and tested for its digital characteristics such as risetime, falltime, and propagation delay time, and not for any linear amplification properties.

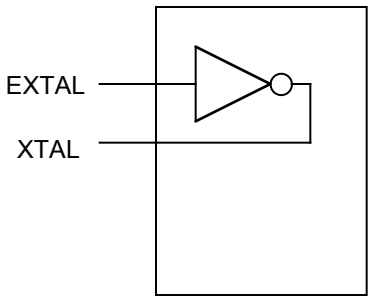


Fig. 1 The Basic Clock Oscillator.

A key decision concerns the type of source to be used for the system clock. The choice generally lies between the following methods:

1. A purpose-designed Hybrid Crystal Clock Oscillator, the type normally found in a metal can with four pins and similar to a Dual In-line Package (DIP).
2. A suitably available and stable on-board clock waveform from another section of the total design.
3. A self-oscillating crystal oscillator composed of a crystal, with tuning capacitors and supplementary resistors.

Most designs will move faster through the design, debugging and production phases if the choice is made from methods 1 or 2. Generally method 1 is used because no comparable alternative exists on the board already. If method 2 is selected, it is important that it is a jitter-free source with extremely low noise constituents, since any shortcoming at this point in the circuit may produce subsequent problems in other parts of the chip, such as the Phase Lock Loops.

The Hybrid Crystal Clock Oscillator used in method 1 is generally a unit which is well designed by experts in their field. Therefore it may be relied upon unfailingly to start at low rail voltage, and to perform in a guaranteed manner over a full temperature range. All specifications including jitter and noise components are known and controlled. The benefit of these qualities cannot be overstated in the total system behavior since the overall performance is critically dependent on the quality of the clock source. Often a double frequency clock is generated and this is followed by a CMOS divide-by-two circuit. This produces a high amplitude voltage swing with accurate matching of each half of the clock waveform to be input to the EXTAL pin. It is important in such circuits that no connection is made to the XTAL pin, even for measurement - clock output pins (CLKO) are provided for any external connections. It is an advantage of this type of circuit that it will be unaffected by typical changes in some chip parameters when revisions and shrinks in size are made over the lifetime of the part. We shall see that these important advantages are not shared by method 3.

Examples employing method 1 are to be found in the schematics for the Freescale evaluation cards on the worldwide web - a good starting point is http://www.mot.com/SPS then follow the specific embedded communications device track using the hot buttons.

Method 3 is a popular and much-used scheme because it is the lowest cost. However its use carries with it potential problems which need care in design and production if it is to remain trouble free over its production lifetime. This method requires particular care in the design and PCB layout process to guarantee an area of the PCB free of digital noise. Its location should be very close to the two clock pins of the chip. Also, the circuit values may require adjustment on test, once samples of the PCB have been produced. Testing should include varying the oscillator passive components both sides of the nominal value to ensure good starting conditions and stable operational frequency. Even so, in production, this circuit may not continue working if the chip goes through a shrink in manufacturing size. In this event, the same set-up procedure must be repeated after changes have re-established a good working set of values once again. The functionality of this circuit will now be examined qualitatively to help understand the main factors involved in its operation.

2. The Self-Oscillating Clock Circuit

The components of a complete oscillator are shown in Fig. 2.

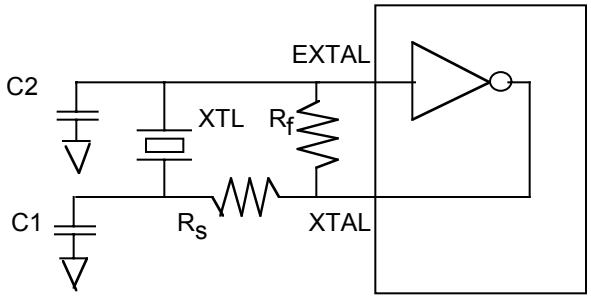


Fig. 2 A self-oscillating clock circuit with external components.

The oscillator circuit has three main sections :

1. Amplifier circuit
2. Crystal component
3. Feedback network.

It is useful to examine each of these stages independently before considering the overall behavior.

2.1. The Amplifier Circuit

The digital inverter stage may be either a single inverter or a triplet of inverters. The equivalent circuit is shown in Fig. 3 complete with a high value feedback resistor necessary for biasing the stage into the linear amplification zone of operation. Because of the 180 degree phase change from input to output, the resistor charges the capacitative input to a stable operating point. If the amplifier is a triplet, only the first stage will be biased into the linear zone with the following two stages acting in normal digital mode. Under some circumstances, triplets can give rise to undesirable modes of oscillation due to parasitic feedback paths within the main feedback loop.

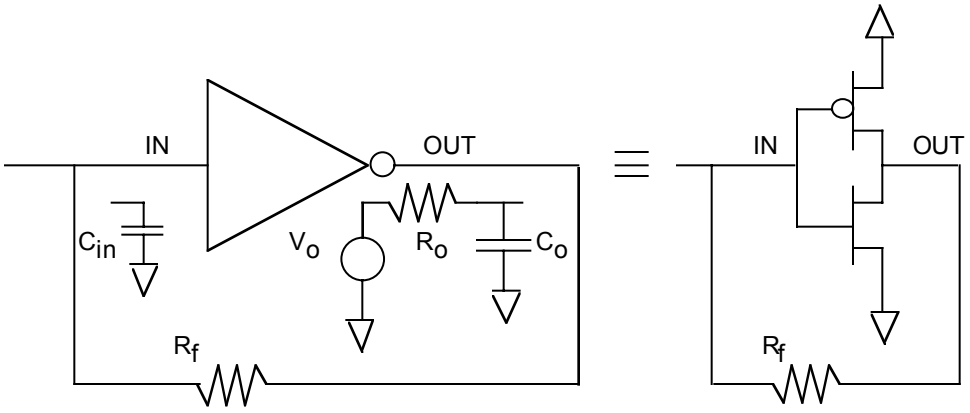


Fig. 3 A digital inverter biased into a linear amplification zone using a single feedback resistor. Both the logical and the circuit-based forms are shown.

This inverting digital amplifier is operated as an analog stage by employing a feedback resistor which charges up the input capacity of the amplifier from the output. The resistor also provides negative feedback to reduce the gain of the stage. Fig. 4 shows the typical response curve for such an amplifier.

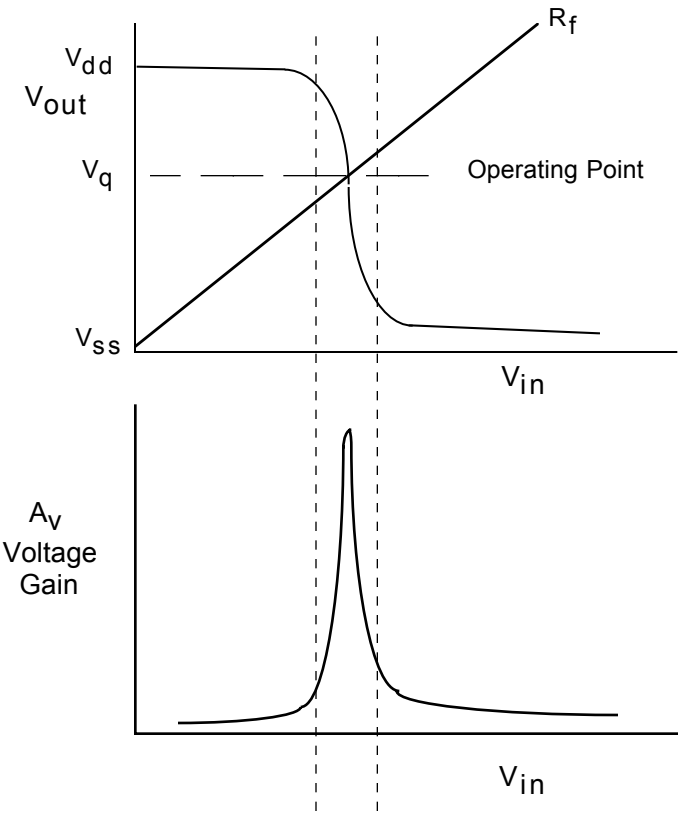


Fig. 4 Stabilized operating point of the amplifier with a load R_f.

The output characteristic of the amplifier approximates to a first order low-pass filter in series with a voltage generator. The roll-off corner frequency represents an upper frequency operational limit for most practical purposes.

2.2 The Crystal

A crystal is a capacitor with quartz as the dielectric. Applying a voltage to quartz makes it bend, and conversely, bending quartz makes it produce a voltage. The equivalent circuit shown in Fig. 5 shows one arm with inductance, capacitance, and resistance connected in series, also a second arm containing capacitance connected in parallel with the first. Therefore the crystal behaves as a very high-Q tuned circuit with a series resonance at f_s formed by L_s with C_s, and a parallel resonance at f_p formed by L_s with C_p. The resistance R_s is only dominant when the crystal is in series resonance, during any other condition it is not significant. The two resonances appear close together on a plot of complex impedance v. frequency.

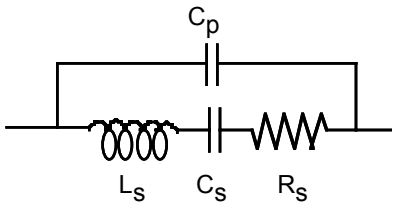


Fig. 5 Equivalent Circuit of a Crystal.

Plotting phase v. frequency shows it is mainly capacitive, but it displays inductive behavior between the series and parallel resonant points. During the capacitive response the voltage lags the current with a phase relationship of -90 degrees, when the response becomes inductive the voltage leads the current with a phase relationship of +90 degrees. Figs. 6 and 7 show a magnified view of the fundamental resonant frequency area for both complex impedance and phase angle.

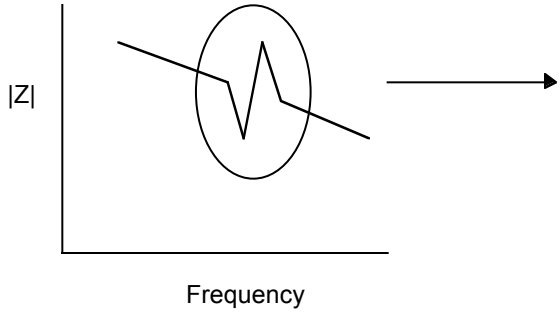


Fig. 6 Complex Impedance v. Freq.

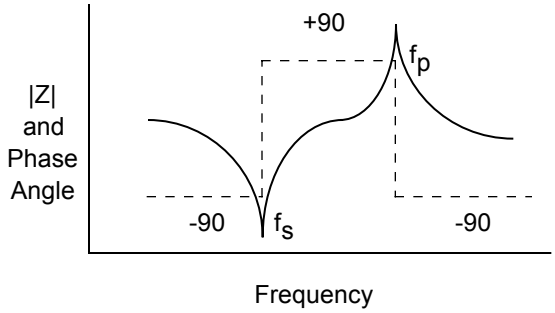


Fig. 7 Complex Impedance and Phase v. Freq. (magnified).

The characteristic of the crystal may be simplified to that of a device with an inductive response between f_s and f_p, and a capacitive response elsewhere.

2.3 The Feedback Network

The Barkhausen criteria for oscillation requires that (a) the phase shift around the feedback loop of an oscillator shall be N x 360 degrees and (b) the gain around the loop shall be greater than one. Oscillators commonly use circuits which combine an amplifier with an L-C resonant circuit. The amplifier provides gain and 180 degrees phase shift and the L-C resonant circuit provides 180 degrees of phase shift with frequency shaping or selectivity. This ensures the criteria will be met for a narrow range of frequencies and guarantees the oscillation will be at the desired frequency.

The circuit shown in Fig. 8 is a circuit which exhibits a 180 degree phase shift across the inductance at parallel resonance. The frequency of resonance is the well known equation $f=1/(2\pi\sqrt{(LC)})$. This equation requires a large change in capacity C, for a moderate change in the value of the resonant frequency.

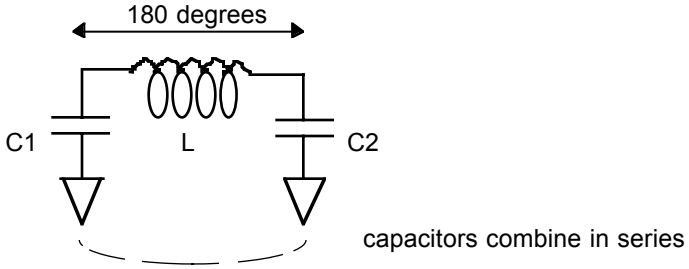


Fig. 8 An L-C Resonant Feedback Network.

If we now replace the inductance in the circuit of Fig. 8 with a crystal, recalling that the crystal exhibits inductive properties in a narrow frequency band, then we get an equivalent circuit which is shown in Fig. 9.

A practical circuit has both series and parallel added capacity, some of this is due to the external components and some due to the PCB. The effect is to shift the peak responses of the crystal circuit. The serial peak will increase in frequency for extra added serial capacity, and the parallel peak will reduce in frequency for extra added parallel capacity. The net result is an operating point which is just to the right of the nominal crystal series resonant frequency, as shown in Fig. 10. Another effect of added capacity is a lessening of the effective circuit-Q, thus reducing loop gain and broadening the overall frequency selection curve.

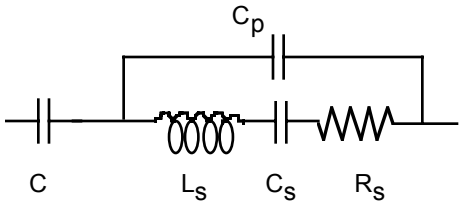


Fig. 9 Equivalent Circuit of a Crystal Feedback Network.

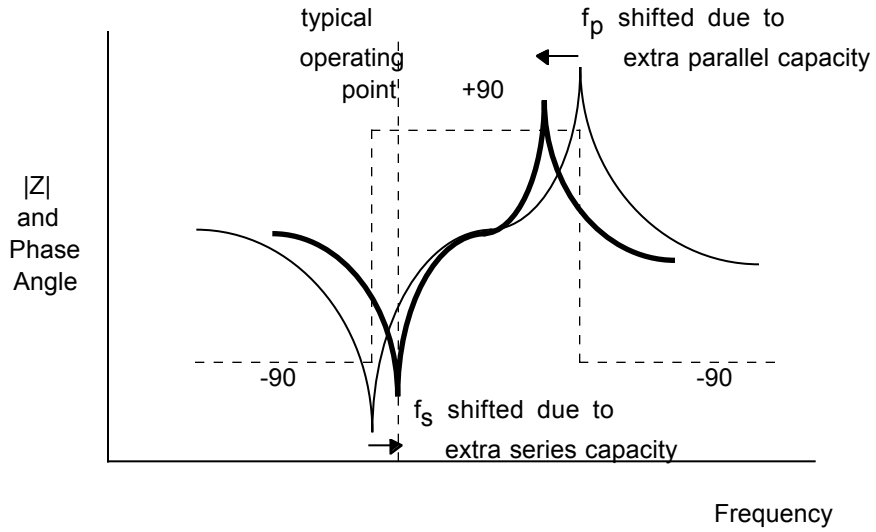


Fig. 10 Complex Impedance and Phase v. Freq. showing the effect of extra series and parallel capacity.

The circuit shown in Fig. 11 now includes a variable capacitor for fine adjustment of the operating frequency. It should be noted the network has no d.c. path, and exhibits high impedance when it has a phase shift of 180 degrees.

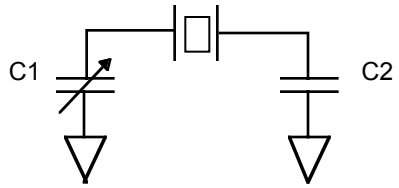


Fig. 11 A Crystal Feedback Network with Frequency Trimming Capacitor.

Earlier, I mentioned problems encountered with these oscillators when the silicon chip goes through a size reduction or shrink. One effect of the shrink is to lower the output impedance of the amplifier. This may effectively short-circuit the input capacitor C1, if the reactance of the input pins of the feedback network is not significantly lower than the output impedance of the amplifier. The resulting phase-shift around the loop may no longer be 180 degrees, which causes the oscillator to fail to start at power switch-on.

The circuit shown in Fig. 12 illustrates the problem and the main components involved. It is necessary for the reactance of the capacitor to be well below the output impedance to avoid this problem - after a shrink, an increase in capacitor value may be needed to maintain the original ratio with the output impedance.

$$X_{C1} << R_o \text{ where } X_{C1} = 1/(2\pi f_s C1)$$

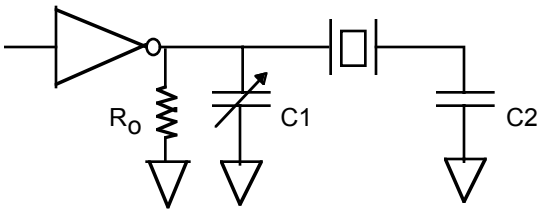


Fig. 12 Possible short-circuit of the input capacitor by the amplifier output impedance.

For circuits operating at lower frequency, the corresponding value of X_{C1} will be higher, leaving this component more prone to being shorted out by R_o. This problem may be solved by inserting a series resistor to isolate the two components, a value around 330K is usually adequate, as in Fig. 13.

The value of V_{DD} used affects the output impedance of the amplifier. Circuits operating at 5V will require different external values from those operating at 3.3V.

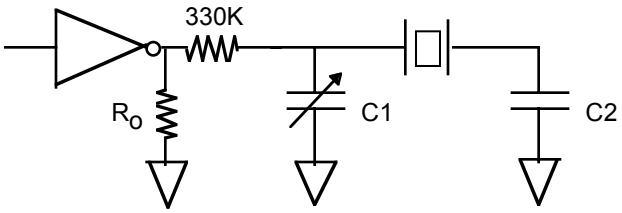


Fig. 13 Series resistor added to isolate the output impedance of the amplifier from the input stage of the network.

3.0 The Complete Oscillator

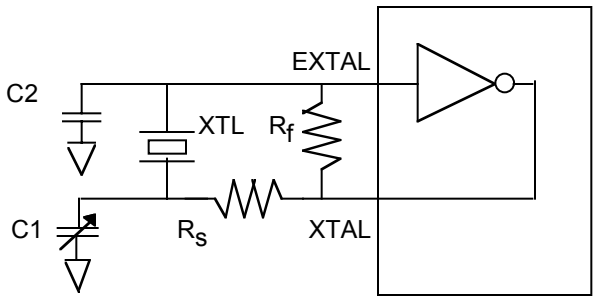


Fig. 14 The complete oscillator with all external components.

As a bandpass filter the Crystal has a very high Q-value, approximately 50K to 1M. Very pure sinusoidal waveforms are generated at the EXTAL input pin, but these are limited by the rail voltage and the amplifier. If a pure waveform is required, clipping may be controlled by inserting a variable resistor after the crystal to control the magnitude of the signal.

The value of the D.C. bias resistor R_f must be sufficiently large to prevent it becoming a parasitic feedback loop, effectively bypassing the feedback network and leading to uncontrolled oscillations.

The series resistance of crystals is very variable and is not usually specified. Instead, an effective series resistance (ESR) is given which is a measurement made at the series resonant frequency with some nominal value of capacity connected in series - the ESR will vary depending on the value of capacity used.

3.1 Some Production Concerns with the Oscillator

The oscillator may produce the wrong frequency after an integrated circuit shrink, due to the frequency response of the amplifier being extended. Higher harmonic frequencies of the crystal, previously well-suppressed, now may be in-band because the corner frequency of the low-pass output filter characteristic is moved to a higher frequency value. Also the output and input capacity of the chip are changed largely due to the impact of protection measures on the chip, thus requiring adjustments to the external components in compensation. The impact of the lowered output impedance has already been discussed

Over the lifetime of the circuit, the crystal properties may change due to ageing. Over a period of years, the tendency is for the crystal to increase its resonant frequency.

Some types of crystal can be overdriven when connected in this type of configuration. Care should be taken that the crystals are suitable for the voltage range in which they are to be used.

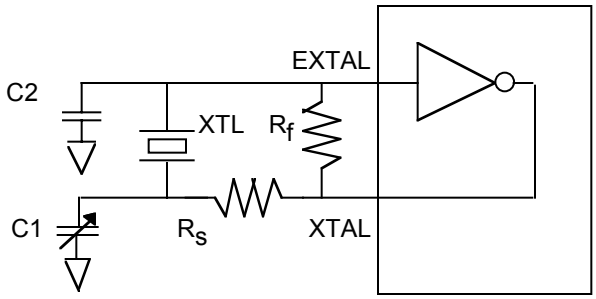
The temperature coefficient of crystals may be a factor for consideration where high stability is required. Frequently, miniature ovens are used for maintaining high stablity oscillators within a narrow operating band of temperature.

All crystals have multiple responses in their frequency characteristics. Firstly, there are the direct overtones or harmonic responses at odd multiples of the fundamental frequency. These are not troublesome if the roll-off frequency of the amplifier and filter network lie below these frequencies. Sometimes there are three-dimensional spurious modes so close to the wanted main frequency, they are difficult to suppress. The oscillator may spontaneously jump between these frequencies and the main frequency causing a form of jitter in the output waveform. To minimize this, manufacturers try to make their crystals as 2-dimensional as possible.

Designers should be aware that AT-strip crystals which are a cut-down form of the circular type, often exhibit multiple spurious responses and should generally be avoided, since these will suffer worse spontaneous jumping problems than other types.

3.2 Initial Values for Practical Oscillators

Differences in performance between various designs can be attributed to the components used as well as the layout employed in the PCB. Nevertheless, the principles described should enable a stable operating point for the oscillator to be reached comparatively easily, but not with zero effort. Because of these variations, there is no single set of values which can be guaranteed to work in every case. However, a set of starting values can be recommended which will mostly function well enough to allow further experimentation and adjustment to achieve final reliable values.



Frequency	C1	C2	Rs	Rf
33KHz	20pF	20pF	330K	20M
4.194MHz	56pF	47pF	1K	10M

Fig. 14 Table of starting values

4.0 Conclusions

This note has examined some of the issues confronting a designer in the choice and use of oscillators with modern integrated communications integrated circuits. Using the techniques described in this paper, it should be possible to achieve stable working oscillators which will perform well over the useful lifetime of the product.

5.0 Acknowledgement

We acknowledge Ken Burch who has worked for many years in this subject and who provided the insight and information.