MC68360
MC68EN360

Product Brief

MC68360 RAM Microcode Package Option Overview

The MC68360 Quad-Integrated Communications Controller (QUICC) contains a communications processor (CP) which performs protocol processing tasks for the device. It currently supports seven protocols: Ethernet, HDLC/SDLC, HDLC Bus, AppleTalk, UART, BISYNC, and totally transparent. The architecture of the QUICC allows for the installation of additional protocol support pacakges in its dual-ported RAM. These packages allow the QUICC to perform new protocols or offload some of the protocol processing work from the CPU to the communications processor.

CURRENTLY OFFERED RAM MICROCODE PACKAGES

This document provides an overview of all of the currently offered RAM Microcode Packages. They are

- Signalling System No. 7 Protocol Support
- Multiple Channel CGI
- ATM Framing
- Asynchronous HDLC for Point-to-Point Protocol (PPP) Support
- PROFIBUS Controller
- Enhanced Ethernet Filtering

MICROCODE PACKAGE USE

These RAM microcode packages are supplied as Motorola S-Record format files containing the object code for the RAM microcode. They are usable on any mask version of the MC68360 or MC68EN360, there is no special silicon which needs to be ordered. At boot time, the user program loads the data from the S-Record into the Dual-Ported RAM inside the QUICC whose operation is to be modified. The area into which the microcode is loaded is inaccessible to the user after this point. Therefore, a QUICC running one of the microcode packages will lose 768 bytes or 1280 bytes (depending upon microcode size) of space for buffer descriptors inside that QUICC.

SIGNALLING SYSTEM NO. 7

Signalling System #7 (SS7) is a management protocol used in public switching networks. The physical, data link, and network layer functions of the SS7 protocol are called the Message Transfer Part (MTP).

The data link layer portion of the MTP (layer 2) is based upon HDLC frame formats. However, SS7 at layer 2 also includes some unique functions that are difficult to implement using an unaltered HDLC controller. These functions include: counting the number of octets by which a frame is too long; sending fill in signal units (FISUs) and link status signal units (LSSUs) continuously; maintaining the SU Error Monitor; and filtering duplicate back-to-back frames.

FISUs are 5 byte frames (three bytes plus 2 CRC bytes) that are sent continuously back-to-back when no other data needs to be transmitted. LSSUs are also sent back-to-back during the initial alignment of the protocol. LSSUs are 6 or 7 bytes long. SS7 also differs from other HDLC-based protocols in that the closing flag of one frame can be the opening flag of the next frame. Since these characteristics can make SS7 implementations very demanding, the SS7 controller on the QUICC provides additional help in these areas.

This controller only performs the lowest layers of the SS7 protocol stack. The upper layers must be performed in software by the CPU in the system. The software to perform the upper layer protocol is available from third party providers.

The SS7 controller contains the following key features:

- Uses either NMSI or TDM interface and a variety of data encoding schemes.
- Flexible data buffers with multiple buffers per signal unit allowed.
- Separate interrupts for received signal units and transmitted buffers.
- Maintenance of good frame counter, bad frame counter, and SU Error Monitor.
- Standard HDLC features:
  - — Flag/Abort/Idle generation/detection
  - — Zero insertion/deletion
  - — 16-bit CRC-CCITT generation/checking
  - — Detection of non-octet aligned signal units
  - — Programmable number of flags between signal units
- Detection of long SUs.
- Discard short (less than 5 octets) signal units.
- Automatic Fill-In Signal Unit transmission.
- Automatic Link Status Signal Unit retransmission.
- Automatic discard of identical FISUs and LSSUs.
- Octet Counting Mode support.
- Command to force a reset of filtering state.
- Command to force entry into octet counting mode.
- Ability to permanently disable octet counting mode.
- Ability to disable FISU and LSSU filtering.
- Ability to force entry into octet counting mode if a receiver overrun occurs.
- Consumes 1280 bytes of the QUICC's internal memory.

PERFORMANCE

At 25Mhz, an aggregate SS7 bandwidth of 6 Mbps divided among the 4 SCCs consumes 100% of the processing power of the RISC communications engine. If only a percentage of the total available SS7

bandwidth is used, the remaining RISC processing power can be used to run other protocols on other channels. Table 1 shows possible QUICC configuration.

Table 1. SS7 Configuration

SS7 Channels	Risc Bandwidth Consumed (est)	Possible Configuration of Other Channels
1 x 64 Kbit/s	1%	1 x 10 Mbit Ethernet, 2 x 2.048 Mbit HDLC
2 x 64 Kbit/s	2%	2 x 4 Mbit HDLC, 2 x 19.2 Kbit SMC UART
3 x 64 Kbit/s	3%	1 x 6 Mbit HDLC, 2 x 19.2 Kbit SMC UART

ORDERING INFORMATION

Title	Order Number
SS7 Microcode Package on a DOS disk	M68360SWSS7-DOS

Multiple GCI Controller Overview

The MC68360 Quad Integrated Communications Controller (QUICC) can handle connections over two basic rate ISDN links using its Serial Management Controllers. For connection to more than two ISDN links, the Multiple GCI (MGCI) RAM-based microcode provides General Circuit Interface (GCI) handling functions for up to 16 basic rate ISDN subscriber lines. MGCI can be used in any application where multiple ISDN lines need to be terminated, such as 2, 4, 8, or 16-subscriber ISDN line cards and video servers.

Associated with each ISDN subscriber line is a monitor channel, a C/I channel, two B-channels, and one D-channel. MGCI handles only the monitor and C/I channels and has no effect on the B and D channels.

TYPICAL APPLICATION

Figure 1 shows a typical 16-subscriber ISDN line card using MGCI in an ISDN switch. Each subscriber line is terminated on the line card by a U or S/T line transceiver (e.g. MC145572 or MC145574). The multiplexer logic converts between the 16 individual basic rate GCI circuits and time division multiplex links carrying the D, B and control channels. The B channels are routed to the main system via the system interface while the D-channels are handled on the board. The C/I and monitor channels are used on the board to carry control and status information between the MC68360 and the line transceivers.

MGCI CONTROLLER KEY FEATURES

- Implements ISDN GCI and analog GCI monitor channel and C/I channel protocols.
- Handles GCI monitor message reception and transmission automatically.
- Handles four and six bit C/I code reception and transmission.
- User programmable C/I receiver detection mechanism: single change or double last look.
- All receive data is timestamped.
- Handles 2, 4, 8, or 16 ISDN lines with full C/I and monitor channel functions.
- Handles up to 32 ISDN lines with only C/I channels.

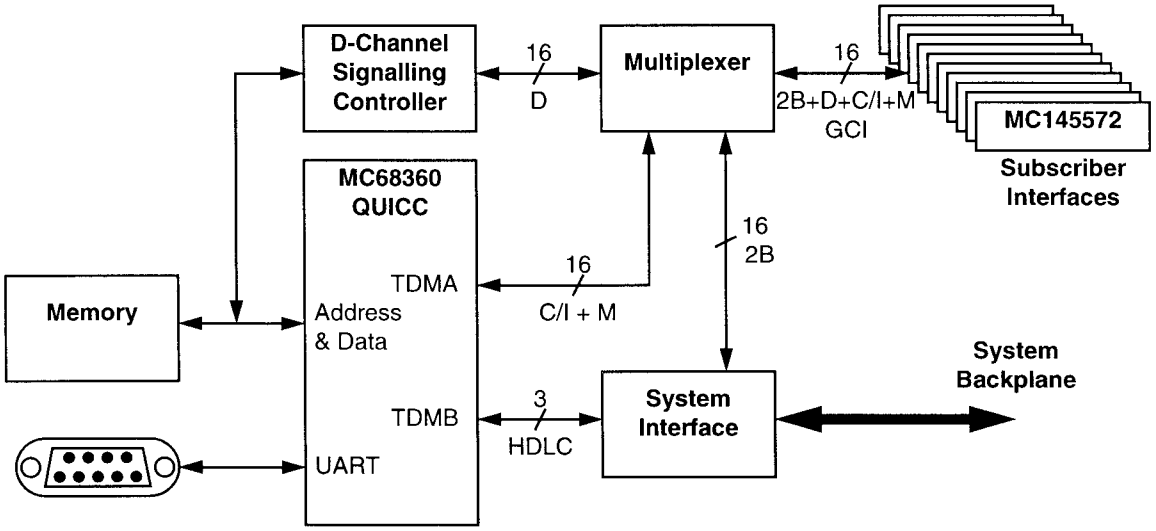

Figure 1. Typical 16-SUbscriber ISDN Line

- Simultaneous detection of multiple C/I code changes and transmission changes.
- Maskable interrupts generated for many events.
- Handles GCI monitor messages from 1 to 64 Kilobytes in length.
- Monitor receiver can be locked into a particular channel.
- Monitor receiver and transmitter include timers to prevent lockup due to inactivity.
- Operates independently of user CPU activity.
- Consumes 1280 bytes of the QUICC's internal memory.

PERFORMANCE

At 25Mhz, an MGCI serial bit rate of 2 Mbps on one SCC consumes 20 - 25% of the processing power of the RISC communications engine. An MGCI SCC operating at a serial bit rate of 2Mbps carries 32 x 64Kbit channels, Table 2 shows possible QUICC configuration.

Table 2. MGCI SCC Configuration

MGCI SCCs	Risc Bandwidth Consumed (est)	Possible Configuration of Other Channels
1 x 2 Mbit/s	25%	3 x 2 Mbit HDLC, 2 x 9.6 Kbit SMC UART
2 x 2 Mbit/s	50%	2 x 2 Mbit HDLC, 2 x 9.6 Kbit SMC UART

ORDERING INFORMATION

Title	Order Number
MGCI Microcode Package on a DOS disk	M68360SWMGCI-DOS

ATOM1/ATM CONTROLLER

ATOM1 provides physical layer ATM functions by converting one or more of the QUICC's Serial Communication Controllers (SCCs) into an ATM cell transmitter and receiver. The microcode provides the user with basic cell streaming facilities (cell reception and transmission) and event indications. The primary application of ATOM1 is intended to be plesiochronous digital hierarchy (PDH) and synchronous digital hierarchy (SDH) E1 and DS1 ATM equipment. Such equipment is used for signalling and low rate data transfer.

Figure 2 shows an ATM / frame relay interworking system as may be used in remote bridging applications. Using the Ethernet channel available on the QUICC, remote LAN bridging equipment can be constructed to link remote Ethernet LANs over E1 telecommunications links.

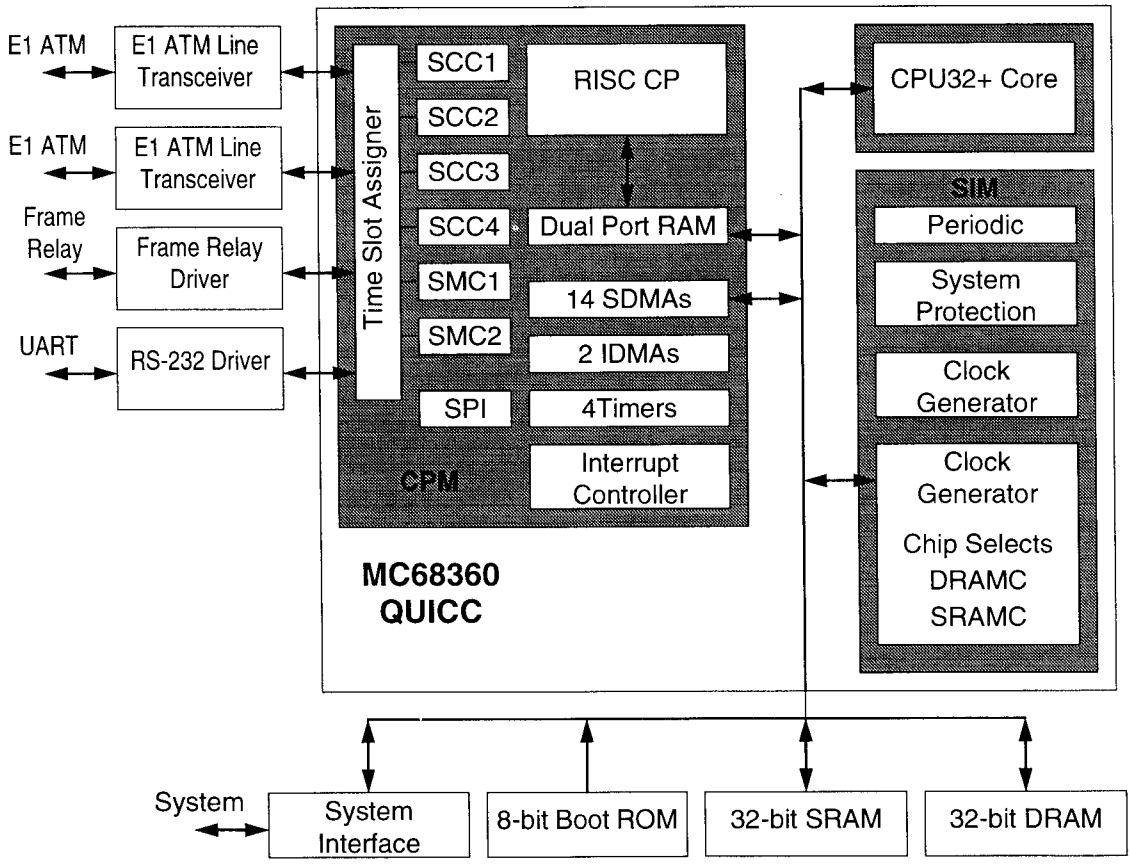

Figure 2. ATM/Frame Relay Interwork System

KEY FEATURES

- Cell transmission and reception for all AAL protocols.
- Transmit and receive data buffers located in main memory.
- Microcode constructs the cell header and appends user defined payload on transmit.
- Microcode verifies cell headers and strips HEC before passing cell to the user on receive.
- Empty cells transmitted when there are no pending data transfers.
- Empty cells and cells with non-matching headers are automatically discarded on receive.
- Scrambling option is provided utilizing the self-synchronizing $X^{43} + 1$ scrambling polynomial.
- Incoming cells with incorrect HECs are received and marked.
- Bandwidth reservation mechanism in the transmitter to allow mixing of data and isochronous services.
- CAM support on reception for handling many connections.
- Consumes 1280 bytes of the QUICC's internal memory.

PERFORMANCE

At 25Mhz, an aggregate ATOM1 bandwidth of 10 Mbps divided among the 4 SCCs consumes 100% of the processing power of the RISC communications engine. If only a percentage of the total available ATOM1 bandwidth is used, the remaining RISC processing power can be used to run other protocols on other channels. Table 3 shows the possible QUICC configuration.

Table 3. ATOM1 Configuration

ATOM1 Channels	Risc Bandwidth Consumed (est)	Possible Configuration of Other Channels
1 x 6 Mbit/s with scrambling	90%	3 x 64Kbit HDLC or Transparent
1 x 10 Mbit/s non-scrambling	90%	2 x 64Kbit HDLC or Transparent
2 x 2 Mbit/s with scrambling	40%	2 x 2.5 Mbit HDLC or Transparent, 9.6 Kbit SMC UART
2 x 2 Mbit/s non-scrambling	40%	1 x 10 Mbit Ethernet, 9.6 Kbit SMC UART

ORDERING INFORMATION

Title	Order Number
ATOM1 Microcode Package on a DOS disk	M68360SWATM1-DOS

ASYNCHRONOUS HDLC FOR PPP

Asynchronous HDLC is a frame-based protocol (see Figure 3), defined by the Internet Engineering Task Force (IETF) "Request For Comments #1549" which uses HDLC framing techniques in conjunction with UART-type characters. This protocol is typically used as the physical layer for the Point-to-Point (PPP) protocol. While this protocol can be implemented by the UART controller on the QUICC in conjunction with the CPU32+, it is more efficient and less compute-intensive for the CPU to allow the Communications Processor Module (CPM) of the QUICC to perform the framing and transparency functions of the protocol.

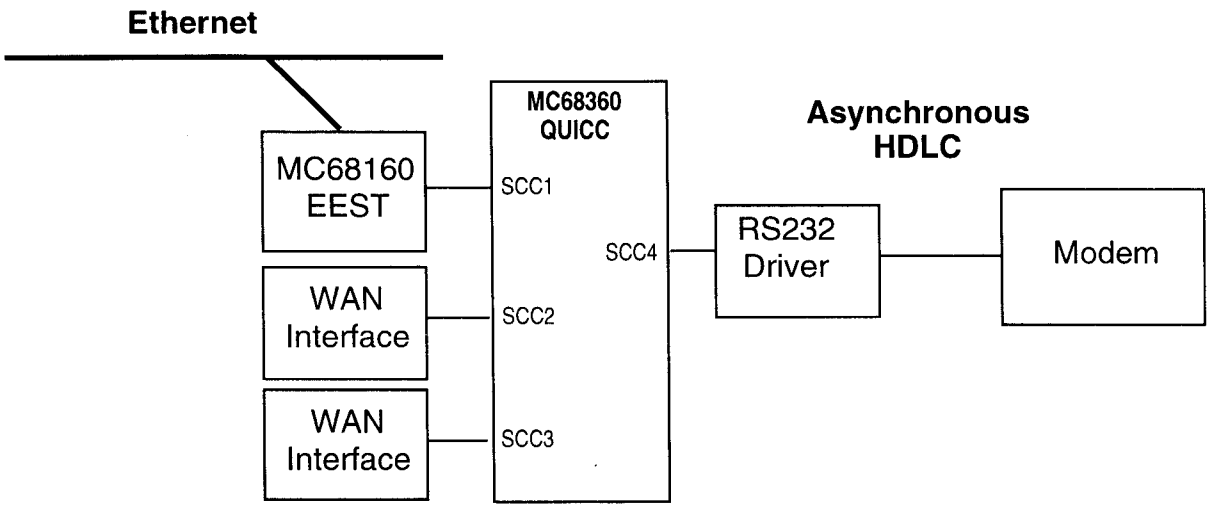

Figure 3. Asynchronous HDLC Block Diagram

KEY FEATURES

- Flexible data buffer structure which allows an entire frame or a section of a frame to be transmitted and received.
- Separate interrupts for received frames and transmitted buffers.
- Automatic 16-bit CRC generation and checking (CRC-CCITT).
- Automatic generation of opening and closing flags.
- Reception of frames with only one “shared” flag.
- Automatic generation and stripping of transparency characters according to the Internet Engineering Task Force RFC 1549 utilizing transmit and receive control character maps.
- Automatic transmission of the ABORT sequence (0x7D,0x7E) after the STOP TRANSMIT command is issued.
- Automatic transmission of IDLE characters between frames and characters.
- Consumes 768 bytes of the QUICC’s internal memory.

PERFORMANCE

At 25Mhz, an aggregate Asynchronous HDLC bandwidth of 3 Mbps divided among the 4 SCCs consumes 100% of the processing power of the RISC communications engine. If only a percentage of the total available Asynchronous HDLC bandwidth is used, the remaining RISC processing power can be used to run other protocols on other channels. Table 4 shows the AHDLC configuration

Table 4. AHDLC Configuration

AHDLC Channels	Risc Bandwidth Consumed (est)	Possible Configuration of Other Channels
1 x 115 Kbit/s	4%	1 x 10Mbit Ethernet, 2 x 1.5 Mbit HDLC, 9.6 Kbit SMC UART
2 x 230 Kbit/s	15%	1 x 10Mbit Ethernet, 1 x 1.5 Mbit HDLC, 9.6 Kbit SMC UART
3 x 230 Kbit/s	24%	1 x 5Mbit HDLC, 2 x 9.6 Kbit SMC UART

ORDERING INFORMATION

Title	Order Number
ASYNC HDLC Microcode Package on a DOS disk	M68360SWAHDL-DOS

PROFIBUS CONTROLLER

Process field bus (PROFIBUS) is a UART- based master slave protocol that specific data between 9.6 kbps to 1.525 Mbps. The PROFIBUS protocol is mainly used in industrial process control applications. The protocol is defined in the German DIN standard 19 245.

The PROFIBUS microcode running on the QUICC RISC controller assists the core in handling some of the time-critical PROFIBUS link layer functions, leaving more of the core available for the application software.

KEY FEATURES

- Frame preceding IDLE sequence generation/checking
- Flexible Frame Oriented Data Buffers
- Separate interrupts for Frames and Buffers (Receive and Transmit)
- Maintenance of six 16-bit error counters
- Two Address Comparison Registers with Mask
- Frame Error, Noise Error, Parity Error Detection
- Detection of IDLE in middle of a frame
- Check Sum generation/checking
- End Delimiter (ED) generation/checking
- Init Rx/Tx, Stop TX, Restart TX and Enter Hunt Mode Commands
- Token Rotation Timer, Idle Timer, Slot Timer and Time-out Timer
- Consumes 1280 bytes of the QUICC's internal memory.

ORDERING INFORMATION

Title	Order Number
PROFIBUS Microcode Package on a DOS disk	M68360SWPRO-DOS

ENHANCED ETHERNET FILTERING

The enhanced Ethernet filtering microcode has been created to add a bit more flexibility to the current Ethernet Controller. It allows the user to perfectly accept or reject frames with destination addresses that are contained in a table of 24 entries. In addition to the filtering capability, the microcode adds the ability to replace the externally sampled tag byte with one that is extracted from the address table.

KEY FEATURES

- Can accept or reject incoming frames if the destination MAC address is contained in a list of 24 preprogrammed entries.
- Allows a shorter list to obtain better peripheral performance.
- Can optionally tag incoming accepted frames with an 8-bit tag appended to the end of the frame (rather than using a CAM).
- The filtering can be turned off to allow tagging with no frame rejection.
- Can filter on group and individual addresses.
- Is a "small" microcode (consumes 768 bytes of DPRAM).
- Filtering is only supported on one Ethernet channel (SCC1), the other channel operates normally.

PERFORMANCE

The overhead incurred by the filtering algorithm will depend upon the number of entries in the address table. Table 5 shows possible configurations of other channels given the load added by a number of entries in the address table.

Table 5. Channel Configuration

Number of addresses	Possible Configuration of Other Channels
1-8	1 x 10 Mbit Ethernet, 1 x 200 Kbit HDLC
9-16	1 x 10 Mbit Ethernet, 1 x 200 Kbit HDLC
17-24	1 x 10 Mbit Ethernet

ORDERING INFORMATION

Title	Order Number
Ethernet Filtering Microcode Package on a DOS disk	M68360SWEFF-DOS

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