Applications Information

Interfacing the MC68060 to the MC68360

This document describes the problems associated with interfacing the MC68060 to the QUICC and how to work around them. This document is describes the pertinent differences in bus timing between the MC68040 family and the MC68060. Other relevant information on power and clocking can be found in section 11 of the MC68060 users manual.

Specification Differences

There are 2 bus specification on the MC68060 that do not match the specifications of the MC68360. The following section describes them in detail along with a suggested work around for each.

1. Specification 253. Clock high to $\overline{TS}$ High.

The MC68060 can negate the $\overline{TS}$ signal as quickly as 3nSec from the rising edge of S1. This does not match specification 253 of the 68360 which requires $\overline{TS}$ to be held for a minimum of 5nSec past the rising edge of S1.

Work Around.

To correct this problem, the user must shift the window of $\overline{TS}$ low. This can be achieved by introducing a delay in $\overline{TS}$ from the MC68060 to the MC68360. One example is to place two FAST logic devices back to back. The total delay through the two is 4.4nSec min to 13.2nSec max. This delay is enough to correct the problem without causing a specification violation on $\overline{TS}$ assertion. (Spec. 13 of MC68060 and Spec. 252 of MC68360)

2. Specification 263. Clock low to data-out high impedance.

The specification for the MC68060 requires that the data bus to be in high impedance as fast as 7nSec after the rising edge of S5 when a read cycle is followed by a write cycle. (spec. 17 of MC68060). This specification was introduced so that the MC68060 can pre-condition the data bus from 5v TTL to 3.3v logic level. This specification does not match specification 263 of the 68360, which indicates that the MC68360 may drive the data bus for as long as 15nSec past the falling edge of S0.

Note: This problem is ONLY for 5V operation. If all components connected to MC68360 and MC68060 are 3.3V then user will need no workhand for this problem.

Work Around.

To correct this problem, the user can insert a idle cycle between back to back accesses from the MC68060 to the MC68360. One method of accomplishing this is to force at least one dead state between $\overline{TA}$ negation and $\overline{TS}$ assertion for the next bus cycle. This can be achieved by arbitrating the bus away from the processor on any long-word or byte read or write access to the MC68360. This forces the processor to release the bus, not begin a new bus cycle.

Once the dead state has been completed, the bus is returned to the processor and normal operation continues. This suggested solution does not affect line (burst) accesses, which are typically cacheable and contain no I/O devices. For this reason, performance is not compromised. In this implementation, the only signal that may be affected is $\overline{BG}$. To accommodate this, $\overline{BG}$ is intercepted and combined with the dead-state inserting logic.

The dead-cycle inserted after each access by the MC68060 to the MC68360 will ensure that the clock low to data-out high impedance specification will be met.

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