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The MSCAN on the MC9S12DP256 compared with the MSCAN on the HC12 family

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1 Introduction

This document compares the new MSCAN module on the MC9S12DP256 MCU with the MSCAN module on the HC12 family of MCUs. This document will therefore be an aid to programmers who wish to port a software driver for the MSCAN on a HC12 MCU to the MC9S12DP256 MCU. In this document, the MSCAN on the HC12 family of MCUs will be identified as the Rev. 0.11 MSCAN, whereas the MSCAN on the MC9S12DP256 MCU will be identified as the Rev. 2.08 MSCAN.

A summary of the main differences is as follows:

- The number of control registers increased from 9 to 12

- The number of receive buffers is increased from 2 to 5

- Three transmit buffers accessible one at a time in a single memory address space

- New Listen Only mode

- Addition of an internal timer for message timestamping

- Each transmit and receive buffer has an individual 16-bit timestamp register

- Port CAN registers removed

- Memory space for entire msCAN module reduced from 128 to 64 bytes

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2 Register Map

The Rev. 0.11 MSCAN occupies 128 bytes in the CPU memory space while the Rev. 2.08 only occupies 64 bytes. See Control Registers for further information on the changes in the registers.

Address Offset	
$_00	Control Registers
$_08	9 Bytes
$_09	Reserved
$_0D	5 Bytes
$_0E	Error Counters
$_0F	2 Bytes
$_10	Identifier Filter
$_1F	16 Bytes
$_20	Reserved
$_3C	29 Bytes
$_3D	Port CAN Registers
$_3F	3 Bytes
$_40	Receive Buffer Window
$_4F	16 Bytes
$_50	Transmit Buffer 0
$_5F	16 Bytes
$_60	Transmit Buffer 1
$_6F	16 Bytes
$_70	Transmit Buffer 2
$_7F	16 Bytes

Address Offset	
$_00	Control Registers
$_0B	12 Bytes
$_0C	Reserved
$_0D	2 Bytes
$_0E	Error Counters
$_0F	2 Bytes
$_10	Identifier Filter
$_1F	16 Bytes
$_20	Receive Buffer Window
$_2F	16 Bytes
$_30	Transmit Buffer Window
$_3F	16 Bytes

Figure 1. Rev 0.11 MSCAN Register Organisation   **Figure 2. Rev 2.08 MSCAN Register Organisation**

3 Modes of Operation

Rev 2.08 has a new Listen Only mode. In addition, the Soft Reset state is now called Initialization Mode in Rev. 2.08. Rev 2.08 also has a MSCAN Enable bit which is not present in Rev. 0.11.

3.1 Normal Mode

For the Rev. 2.08 MSCAN, the CANE bit (bit 7 in CANCTL1 register) must be set to enter Normal mode. The following registers can only be written when the CANE bit is set: CANCTL, CANRFLG, CANRIER, CANTFLG, CANTIER, CANTARQ, CANTAAK, CANTBSEL.

3.2 Initialization Mode

This mode was called "Soft Reset State" in Rev. 0.11 spec. In Rev 2.08 this mode is entered when both the INITRQ and INITAK bits are set. The INITRQ bit replaces the SFTRST bit of the MSCAN Rev. 0.11. The INITAK is a new bit which indicates when Initialization mode has been entered. Any ongoing transmission or reception is aborted and synchronization to the bus is lost. The following registers enter their hard reset state and restore their default values: CANCTL0, CANRFLG, CANRIER, CANTFLG, CANTIER, CANTARQ, CANTAAK, CANTBSEL. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0-7, CANIDMR0-7 can only be written by the CPU when the MSCAN is in Initialization Mode The values of the error counters are not affected by initialization. When leaving Initialization Mode the MSCAN restarts and then tries to synchronize to the can bus. If the MSCAN is not in the bus-off state, it synchronizes after 11 consecutive recessive bits on the bus; if the MSCAN is in bus-off state it continues to wait for 128 occurrences of 11 consecutive recessive bits. Writing to other bits in CANCTL0, CANRFLG, CANRIER, CANTFLG or CANTIER must only be done after Initialization Mode is left, which is when INITRQ = 0 and INITAK = 0. The CPU cannot clear the INITRQ bit before the MSCAN has entered Initialization Mode (INITAK = 1). In the Rev. 2.08 MSCAN, the CANE bit must be set to leave this mode.

3.3 Sleep Mode

No difference, but Rev 2.08 has a Wake-up Enable bit which impacts this mode. The Rev. 2.08 MSCAN will wake up from Sleep mode if it detects activity on the CAN bus only if the WUPE bit is set. The Rev. 2.08 MSCAN does not require the WUPIE bit to be set to wake up from Sleep mode, but the WUPIE bit must be set if the MSCAN is required to wake up the CPU from WAIT mode.

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3.4 Power Down Mode

No difference, but Rev 2.08 has a Wake-up Enable bit which impacts this mode. The Rev. 2.08 MSCAN will wake up from Power Down mode (if WUPE = SLPRQ = SLPAK = 1) if it detects activity on the CAN bus if the WUPE bit is set. The WUPIE bit must be set if the MSCAN is required to wake up the CPU from STOP mode.

3.5 Loop Back Self Test Mode

No difference.

3.6 Listen Only Mode

Listen Only mode is a new mode for the Rev. 2.08 MSCAN. In Listen Only mode, the CAN node is able to receive valid data frames and valid remote frames, but it sends only "recessive" bits on the CAN bus. In addition it cannot start a transmission. If the MAC sublayer is required to send a "dominant" bit (ACK bit, overload flag, active error flag), the bit is re-routed internally so that the MAC sublayer monitors this "dominant" bit, although the CAN bus may remain in recessive state externally.

4 Message Buffer Structures

4.1 Message Receive Buffer Structure

In Rev. 0.11 MSCAN received messages are stored in a two stage input FIFO. In Rev. 2.08 MSCAN, this has been increased to a five stage FIFO structure.

Both Rev. 0.11 and Rev. 2.08 have a similar receive buffer structure – a 16 byte memory space containing a 13 byte data structure. However, in Rev. 0.11, the last two bytes ($_xE and $_xF) of the buffer are unused but in Rev. 2.08, these bytes are used by the MSCAN to store a special 16-bit time stamp, which is sampled from an internal timer after successful reception of a message. This feature is only available if the Timer Enable bit is set.

4.2 Message Transmit Buffer Structure

For transmitting messages Rev. 0.11 MSCAN and Rev. 2.08 MSCAN both employ a triple buffer scheme. There is however a significant difference between the two revisions in how the transmit buffers can be accessed by the CPU.

In Rev. 0.11 MSCAN, all three transmit buffers are present in the CPU memory map at all times whereas in Rev. 2.08 MSCAN, only one transmit buffer is present in the CPU memory map at any given time. The desired transmit buffer is selected by setting the appropriate TXx bit in the MSCAN Transmit Buffer Selection register. This feature simplifies the transmit buffer access and makes the handler software simpler, as well as minimizing the required address space.

The following gives a short programming example of the usage of the CANTBSEL register: The application software wants to get the next available

transmit buffer. It reads the CANTFLG register and writes this value back into the CANTBSEL register. In this example transmit buffers TX1 and TX2 are available. The value read from CANTFLG is therefore %00000110 (% is used to indicate binary notation). When writing this value back to CANTBSEL the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to '1' is at bit position 1. Reading back this value out of CANTBSEL results in %00000010, because only the lowest numbered bit position set to '1' is presented. This mechanism eases the selection of the next available Tx buffer for the application software.

```
LDAA CANTFLG ; value read is %00000110
STAA CANTBSEL ; value written is %00000110

;Fill selected TxBuffer

LDAA CANTBSEL ; Read actual TxBuffer selection; value read is
%00000010
STAA CANTFLG ; Transmit selected TxBuffer
```

Both Rev. 0.11 and Rev. 2.08 have a similar transmit buffer structure – a 16 byte memory space containing a 14 byte data structure. However, in Rev. 0.11, the last two bytes ($_xE and $_xF) of the buffer are unused but in Rev. 2.08, these bytes are used by the MSCAN to store a special 16-bit time stamp, which is sampled from an internal timer after successful transmission of a message. This feature is only available if the Timer Enable bit is set.

4.3 Identifier Acceptance Filter

The only difference is that the reset state of the Identifier Acceptance registers and the Identifier Mask registers are $00 in Rev. 2.08 as opposed to undefined after reset in Rev. 0.11.

4.4 Timer Link

Both revisions of MSCAN have a link to a timer which may be enabled if message timestamping is required. On the Rev. 0.11 MSCAN the timer link is to a separate on-chip timer module which is programmed independently from the MSCAN module. The timestamp value for each successive successful transmit or receive event is stored in a single timer capture register. The timer value is captured at the end of the EOF field of the CAN message. However, on the Rev. 2.08 MSCAN the timer link is to a timer internal to the MSCAN module. This is a free running timer which is clocked at the CAN bit rate. The timer value is captured at the sample point of the ACK delimiter bit of the CAN message and is stored in the timestamp register of the appropriate transmit or receive buffer.

5 Control Registers

5.1 MSCAN Control Register 0

Referred to as MSCAN12 Module Control Register 0 (CMCR0) in Rev. 0.11 and MSCAN Control 0 Register (CANCTL0) in Rev. 2.08, there are several changes to this register: three new bits, two bits with new names and modified meaning and one bit moved to Control Register 1.

Address Offset: $xx00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	CSWAI	SYNCH	TLNKEN	SPLAK	SLPRQ	SFTRES
Write:			CSWAI		TLNKEN		SLPRQ	SFTRES
Reset:	0	0	1	0	0	0	0	1

Figure 3. Rev 0.11 Control Register 0 (CMCR0)

Address Offset: $xx00

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
Write:	RXFRM		CSWAI		TIME	WUPE	SLPRQ	INITRQ
Reset:	0	0	0	0	0	0	0	1

Figure 4. Rev 2.08 Control Register 0 (CANCTL0)

Rev 0.11

Read: anytime.
Write: SFTRST anytime; other bits are writeable only when SFTRST = 0

Rev 2.08

Read: anytime
Write: anytime when INITRQ = INITAK = 0; INITRQ can only be cleared when INITRQ = INITAK = 1

Bit 7   Rev 0.11

No meaning, reads as '0'.

Rev 2.08

RXFRM — Receiver Frame Flag

This bit is read and clear only. It is set by the MSCAN when a valid message has been received correctly, independently of the filter configuration. Once set, it remains set until cleared by software or reset. This bit is cleared by writing a '1' to the bit. This bit is not valid in loop back mode.

1 = A valid message was received since last clearing this flag.
0 = No valid message received since last clearing this flag.

Bit 6   Rev. 0.11

No meaning, reads as '0'.

Rev. 2.08

RXACT — Receiver Active Flag

This flag indicates the MSCAN is receiving a message. This bit is read only. This bit is not valid in loop back mode.
1 = MSCAN is receiving a message (including when arbitration is lost.)
0 = MSCAN is transmitting or idle.

Bit 5   Rev. 0.11 and 2.08

CSWAI — CAN Stops in Wait Mode

No change in bit name but the reset state is '0' in Rev. 2.08 instead of '1', as in Rev. 0.11.

Bit 4   Rev. 0.11 and 2.08

SYNCH — Synchronized Status

No change.

Bit 3   Rev. 0.11

TLNKEN — Timer Enable

This bit establishes a link between the MSCAN and the on-chip timer.
1 = The MSCAN timer signal output is connected to the timer input.
0 = The port is connected to the timer input.

Rev. 2.08

TIME — Timer Enable

This bit activates an internal 16-bit wide free running timer which is clocked by the MSCAN bit clock. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active Tx/Rx buffer. As soon as a message is acknowledged on the CAN bus, the time stamp will be written to the highest bytes ($_E, $_F) in the appropriate buffer. The internal timer is reset (all bits set to '0' when Initialization Mode is active.
1 = Enable internal MSCAN timer.
0 = Disable internal MSCAN timer.

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Bit 2   Rev. 0.11

SLPAK — Sleep Mode Acknowledge

In Rev. 2.08 this bit is moved to bit 1 of Control Register 1 (CANCTL1).

Rev. 2.08

WUPE — Wake up Enable

This configuration bit controls whether the MSCAN exits Sleep Mode when traffic on the CAN bus is detected.
   1 = Wake-Up enabled. The MSCAN is able to restart if CAN bus activity is detected.
   0 = Wake-Up disabled. The MSCAN ignores traffic on CAN.

Bit 1   Rev. 0.11 and Rev. 2.08.

SLPRQ — Sleep Mode Request

No change.

Bit 0   Rev. 0.11

SFTRES — Soft Reset

When this bit is set by the CPU, the MSCAN immediately enters the soft reset state. Clearing SFTRST and writing to other bits in CMCR0 must be in separate instructions.
   1 = MSCAN in soft reset state
   0 = Normal operation

Rev. 2.08

INITRQ — Initialization Mode Request

When this bit is set by the CPU, the MSCAN starts to enter Initialization Mode. The module indicates entry to Initialization Mode by setting INITAK = 1. The CPU cannot clear the INITRQ bit before the MSCAN has entered Initialization Mode (INITAK = 1)
   1 = Request MSCAN to enter Initialization mode
   0 = Normal operation

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5.2 MSCAN Control Register 1

Referred to as MSCAN12 Module Control Register 1 (CMCR1) in Rev. 0.11 and MSCAN Control 1 Register (CANCTL1) in Rev. 2.08, there are several changes to Control Register 1: three new bits, two bits moved to different bit positions and one bit which is moved from MSCAN Control Register 0.

Address Offset: $xx01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	LOOPB	WUPM	CLKSRC
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 5. Rev 0.11 Control Register 1 (CMCR1)

Address Offset: $xx01

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 6. Rev 2.08 Control Register 1 (CANCTL1)

Rev. 0.11

Read: anytime
Write: only when SFTRST is set.

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 1.

Bit 7 Rev. 0.11

No meaning, reads as '0'.

Rev. 2.08

CANE — CAN Enable
    CANE is write once in MCU normal modes (multiple writes are possible in MCU special modes). When CANE = 0, the MSCAN is in Initialization mode. When CANE = 1, the MSCAN is enabled.
        1 = The MSCAN module is enabled.
        0 = The MSCAN module is disabled.

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Bit 6   Rev. 0.11

No meaning, reads as '0'.

Rev 2.08

CLKSRC — MSCAN Clock Source
This bit defines the clock source for the MSCAN module.
1 = The MSCAN clock source is the ungated IPbus clock (CLK).
0 = The MSCAN clock source is the oscillator clock (OSC_CLK).

CLKSRC was in bit 0 of Control Register 1 in Rev. 0.11.

Bit 5   Rev. 0.11

No meaning, reads as '0'.

Rev. 2.08

LOOPB — Loop Back Self Test Mode
LOOPB was in bit 2 of Control Register 1 in Rev. 0.11.

Bit 4   Rev. 0.11

No meaning, reads as '0'.

Rev 2.08

LISTEN — Listen Only Mode
This bit configures the MSCAN as a bus monitor. When the bit is set, all valid
CAN messages with matching ID are received, but no acknowledgement or
error frames are sent out. In addition the error counters are frozen. Listen
Only Mode supports applications which require "hot plugging" or throughput
analysis. The MSCAN is unable to transmit any messages when Listen Only
Mode is active.
1 = Listen Only Mode activated
0 = normal operation

Bit 3   Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 2 Rev. 0.11

LOOPB — Loop Back Self Test Mode

Rev. 2.08

WUPM — Wake-Up Mode
WUPM was in bit 1 of Control Register 1 in Rev. 0.11.

Bit 1 Rev. 0.11

WUPM — Wake-Up Mode

Rev. 2.08

SLPAK — Sleep Mode Acknowledge
This flag indicates whether the MSCAN module has entered Sleep Mode. It is used as a handshake flag for the SLPRQ Sleep Mode Request. This is a read only bit. Depending on the setting of the WUPE bit the MSCAN will clear the flag if it detects bus activity on the CAN bus while in Sleep Mode.
1 = Sleep Mode Active
0 = Running – The MSCAN operates normally.

Bit 0 Rev. 0.11

CLKSRC — MSCAN Clock Source

Rev. 2.08

INITAK — Initialization Mode Acknowledge
This flag indicates whether the MSCAN module is in Initialization Mode. It is used as a handshake flag for the INITRQ Initialization request. This is a read only bit. Initialization Mode is active when INITRQ=1 and INITAK=1.
1 = Initialization Mode Active – The MSCAN has entered Initialization Mode.
0 = Running – The MSCAN operates normally.

5.3 MSCAN Bus Timing Register 0

Referred to as MSCAN12 Bus Timing Register 0 (CBTR0) in Rev. 0.11 and MSCAN Bus Timing Register 0 (CANBTR0) in Rev. 2.08, there are no changes to the specification for Bus Timing Register 0.

Rev 0.11

Read: anytime
Write: only when SFTRST = 1

Rev 2.08

Read: anytime
Write: only when INITRQ = INITAK = 1

5.4 MSCAN Bus Timing Register 1

Referred to as MSCAN12 Bus Timing Register 1 (CBTR1) in Rev. 0.11 and MSCAN Bus Timing Register 1 (CANBTR1) in Rev. 2.08, there are no changes to the specification for Bus Timing Register 1.

Rev 0.11

Read: anytime
Write: only when SFTRST = 1

Rev 2.08

Read: anytime
Write: only when INITRQ = INITAK = 1

5.5 MSCAN Receiver Flag Register

Referred to as MSCAN12 Receiver Flag Register (CRFLG) in Rev. 0.11 and MSCAN Receiver Flag Register (CANRFLG) in Rev. 2.08, there have been several changes to the Receiver Flag Register: the five different error interrupt flags are removed and replaced with a single error status change interrupt flag and four error status flags. In addition, the interrupt trigger mechanism has changed from level-sensitive in Rev. 0.11 to edge-sensitive in Rev. 2.08. Thus, depending on the interrupt enable bits in CANRIER, the MSCAN may generate an interrupt whenever a status change occurs.

Address Offset: $xx04

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WUPIF	RWRNIF	TWRNIF	RERRIF	TERRIF	BOFFIF	OVRIF	RXF
Reset:	0	0	0	0	0	0	0	0

Figure 7. Rev 0.11 Receiver Flag Register (CRFLG)

Address Offset: $xx04

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
Reset:	0	0	0	0	0	0	0	0

Figure 8. Rev 2.08 Receiver Flag Register (CANRFLG)

Rev. 0.11

Read: anytime
Write: only when SFTRST = 0. Write '1' to clear a flag, write '0' has no effect.

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 0. Write '1' to clear flag, write of '0' has no effect.

Bit 7   Rev. 0.11 and Rev. 2.08

WUPIF — Wake-Up Interrupt Flag.

No change.

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Bit 6 Rev. 0.11

RWRNIF — Receiver Warning Interrupt Flag.

Rev 2.08

CSCIF — CAN Status Change Interrupt Flag

This flag is set when the MSCAN changes its current bus status due to the actual value of the Transmit Error Counter (TEC) and the Receive Error Counter (REC). Four Receiver/Transmitter status bits (RSTAT[1:0], TSTAT[1:0]) indicate the actual MSCAN status. If not masked, an Error interrupt is pending while this flag is set. CSCIF provides a blocking interrupt. That guarantees that the Receiver/Transmitter status bits (RSTAT/TSTAT) are only updated when no MSCAN Status Change interrupt is pending. If the TECs/RECs change their current value after the CSCIF is asserted and therefore would cause an additional state change in the RSTAT/TSTAT bits, these bits keep their current value until the CSCIF interrupt is cleared again.
    1 = MSCAN changed current error status.
    0 = No change in error status occurred since last interrupt.

Bit 5 Rev. 0.11

TWRNIF — Transmitter Warning Interrupt Flag

Rev. 2.08

RSTAT1 — Receiver Status bit 1

RSTAT1, RSTAT0 — Receiver Status Bits

These bits are read only. The values of the Error Counters control the actual error status of the MSCAN. As soon as the Status Change Interrupt Flag (CSCIF) is set these bits indicate the appropriate receiver related error status of the MSCAN. The coding for the bits RSTAT1, RSTAT0 is:
    00 = RxOK: $0 \leq$ Receive Error Counter ≤ 96
    01 = RxWRN: $96 <$ Receive Error Counter ≤ 127
    10 = RxERR: $127 <$ Receive Error Counter
    11 = BusOff: Transmit Error Counter > 255

NOTE: *When a CAN bus error occurs which would increment the TEC to a value greater than 255, the TEC overflow is detected and the MSCAN enters the Bus-off state.*

Bit 4   Rev. 0.11

RERRIF — Receiver Error Interrupt Flag

Rev. 2.08

RSTAT0 — Receiver Status Bit 0.
   See bit 5 for description of RSTAT0.

Bit 3   Rev. 0.11

TERRIF — Transmitter Error Interrupt Flag.

Rev. 2.08

TSTAT1 — Transmitter Status Bit 1

TSTAT1, TSTAT0 — Transmitter Status Bits
   These bits are read only. The values of the Error Counters control the actual error status of the MSCAN. As soon as the Status Change Interrupt Flag (CSCIF) is set these bits indicate the appropriate transmitter related error status of the MSCAN. The coding for the bits TSTAT1, TSTAT0 is:
   00 = RxOK: $0 \leq$ Transmit Error Counter ≤ 96
   01 = RxWRN: $96 <$ Transmit Error Counter ≤ 127
   10 = RxERR: $127 <$ Transmit Error Counter < 255
   11 = BusOff: Transmit Error Counter > 255

NOTE: *When a CAN bus error occurs which would increment the TEC to a value greater than 255, the TEC overflow is detected and the MSCAN enters the Bus-off state.*

Bit 2   Rev. 0.11

BOFFIF — Bus-Off Interrupt Flag

Rev. 2.08

TSTAT0 — Transmitter Status Bit 0
   See bit 3 for description of TSTAT0.

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Bit 1   Rev. 0.11 and Rev. 2.08

OVRIF — Overrun Interrupt Flag
No change.

Bit 0   Rev. 0.11 and Rev. 2.08

RXF — Receive Buffer Full
No change.

5.6 MSCAN Receiver Interrupt Enable Register

Referred to as MSCAN12 Receiver Interrupt Enable Register (CRIER) in Rev. 0.11 and MSCAN Receiver Interrupt Enable Register (CANRIER) in Rev. 2.08, there have been several changes to the Receiver Interrupt Enable Register: the five different error interrupt enable flags are removed and replaced with a single error status change interrupt enable flag and four error status change interrupt control flags.

Address Offset: $xx05

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WUPIE	RWRNIE	TWRNIE	RERRIE	TERRIE	BOFFIE	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0
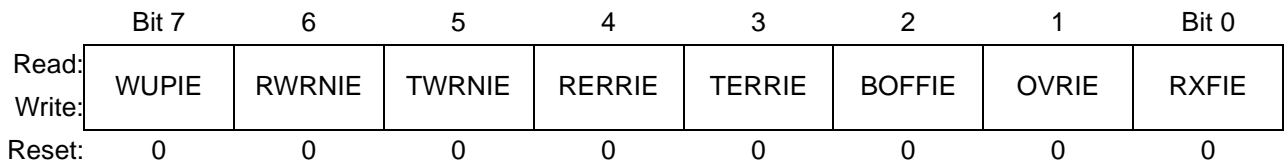
Figure 9. Rev 0.11 Receiver Interrupt Enable Register (CRIER)

Address Offset: $xx05

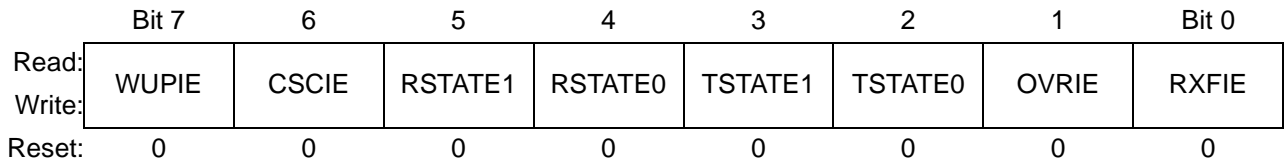|	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0

Figure 10. Rev 2.08 Receiver Interrupt Enable Register (CANRIER)

Rev. 0.11

Read: anytime
Write: only when STFRST = 0

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 0

Bit 7 Rev. 0.11 and Rev. 2.08

WUPIE — Wake-Up Interrupt Enable
   No change.

Bit 6 Rev. 0.11

RWRNIE — Receiver Warning Interrupt Enable

Rev. 2.08

CSCIE — CAN Status Change Interrupt Enable
      1 = A MSCAN Status Change event causes an error interrupt
         request.
      0 = No interrupt request is generated from this event.

Bit 5 Rev. 0.11

TWRNIE — Transmitter Warning Interrupt Enable.

Rev. 2.08

RSTATE1 — Receiver Status Change Enable Bit1.

RSTATE1, RSTATE0 — Receiver Status Change Enable
   These bits control the sensitivity level in which receiver state changes
   cause CSCIF interrupts.
      11 = generate CSCIF interrupt on all state changes
      10 = generate CSCIF interrupt only if the receiver enters or
         leaves "RxErr" or "BusOff" state. Discard other receiver
         state changes for generating CSCIF interrupt.
      01 = generate CSCIF interrupt only if the receiver enters or
         leaves "BusOff" state. Discard other receiver state
         changes for generating CSCIF interrupt.
      00 = do not generate any CSCIF interrupt caused by receiver
         state changes.

Bit 4 Rev. 0.11

RERRIE — Receiver Error Interrupt Enable.

Rev. 2.08

RSTATE0 — Receiver Status Change Enable Bit 0
   See bit 5 for description of RSTATE0.

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Bit 3   Rev. 0.11

TERRIE — Transmitter Error Interrupt Enable.

Rev. 2.08

TSTATE1 — Transmitter Status Change Enable Bit 1.

TSTATE1, TSTATE0 — Transmitter Status Change Enable
  These bits control the sensitivity level in which transmitter state changes cause CSCIF interrupts.
    11 = generate CSCIF interrupt on all state changes
    10 = generate CSCIF interrupt only if the transmitter enters or leaves "TxErr" or "BusOff" state. Discard other transmitter state changes for generating CSCIF interrupt.
    01 = generate CSCIF interrupt only if the transmitter enters or leaves "BusOff" state. Discard other transmitter state changes for generating CSCIF interrupt.
    00 = do not generate any CSCIF interrupt caused by transmitter state changes.

Bit 2   Rev. 0.11

BOFFIE — Bus- Off Interrupt Enable.

Rev. 2.08

TSTATE0 — Transmitter Status Change Enable Bit 0.
  See bit 3 for description of TSTATE0.

Bit 1   Rev. 0.11 and Rev. 2.08

OVRIE — Overrun Interrupt Enable.
  No change.

Bit 0   Rev. 0.11 and Rev. 2.08

RXFIE — Receiver Full Interrupt Enable.
  No change.

5.7 MSCAN Transmitter Flag Register

The MSCAN12 Transmitter Flag Register (CTFLG) in Rev. 0.11 has been split up into two separate registers in Rev. 2.08 – The MSCAN Transmitter Flag Register (CANTFLG) and the MSCAN Transmitter Message Abort Acknowledge (CANTAAK). Here CTFLG is compared with CANTFLG.

Address Offset: $xx06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	ABTAK2	ABTAK1	ABTAK0	0	TXE2	TXE1	TXE0
Write:								
Reset:	0	0	0	0	0	1	1	1

Figure 11. Rev 0.11 Transmitter Flag Register (CTFLG)

Address Offset: $xx06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	TXE2	TXE1	TXE0
Write:								
Reset:	0	0	0	0	0	1	1	1

Figure 12. Rev 2.08 Transmitter Flag Register (CANTFLG)

Rev. 0.11

Read: anytime
Write: only when SFTRST = 0

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 0; write of '1' clears flag, write of '0' ignored

Bit 7　　Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 6　　Rev. 0.11

ABTAK2 — Abort Acknowledge Transmit Buffer 2.

Rev. 2.08

No meaning, reads as '0'. ABTAK2 is moved to CANTAAK register.

Bit 5   Rev. 0.11

ABTAK1 — Abort Acknowledge Transmit Buffer 1.

Rev. 2.08

No meaning, reads as '0'. ABTAK1 is moved to CANTAAK register.

Bit 4   Rev. 0.11

ABTAK0 — Abort Acknowledge Transmit Buffer 0.

Rev. 2.08

No meaning, reads as '0'. ABTAK0 is moved to CANTAAK register.

Bit 3   Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 2   Rev. 0.11 and Rev. 2.08

TXE2 — Transmit Buffer 2 Empty
    No Change.

Bit 1   Rev. 0.11 and Rev. 2.08

TXE1 — Transmit Buffer 1 Empty
    No Change.

Bit 0   Rev. 0.11 and Rev. 2.08

TXE0 — Transmit Buffer 0 Empty
    No Change.

5.8 MSCAN Transmitter Interrupt Enable Register

The MSCAN12 Transmitter Control Register (CTCR) in Rev. 0.11 has been split up into two separate registers in Rev.2.08 – The MSCAN Transmitter Interrupt Enable Register (CANTIER) and the MSCAN Transmitter Message Abort Request (CANTARQ). Here CTCR is compared with CANTIER.

Address Offset: $xx07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	ABTRQ2	ABTRQ1	ABTRQ0	0	TXEIE2	TXEIE1	TXEIE0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 13. Rev 0.11 Transmitter Control Register (CTCR)

Address Offset: $xx07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 14. Rev 2.08 Transmitter Interrupt Enable Register (CANTIER)

Rev. 0.11

Read: anytime
Write: only when SFTRST = 0

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 0

Bit 7   Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 6   Rev. 0.11

ABTRQ2 — Abort Request Transmit Buffer 2.

Rev. 2.08

No meaning, reads as '0'. ABTRQ2 is moved to CANTARQ register.

The MSCAN on the MC9S12DP256 compared with the MSCAN on the HC12 family   21

Bit 5   Rev. 0.11

ABTRQ1 — Abort Request Transmit Buffer 1.

Rev. 2.08

No meaning, reads as '0'. ABTRQ1 is moved to CANTARQ register.

Bit 4   Rev. 0.11

ABTRQ0 — Abort Request Transmit Buffer 0.

Rev. 2.08

No meaning, reads as '0'. ABTRQ0 is moved to CANTARQ register.

Bit 3   Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 2   Rev. 0.11 and Rev. 2.08

TXEIE2 — Transmit Buffer 2 Empty Interrupt Enable
    No Change.

Bit 1   Rev. 0.11 and Rev. 2.08

TXEIE1 — Transmit Buffer 1 Empty Interrupt Enable
    No Change.

Bit 0   Rev. 0.11 and Rev. 2.08

TXEIE0 — Transmit Buffer 0 Empty Interrupt Enable
    No Change.

5.9 MSCAN Transmitter Message Abort Request

The MSCAN12 Transmitter Control Register (CTCR) in Rev. 0.11 has been split up into two separate registers in Rev.2.08 – The MSCAN Transmitter Interrupt Enable Register (CANTIER) and the MSCAN Transmitter Message Abort Request (CANTARQ). Here CTCR is compared with CANTARQ.

Note that the CANTARQ register displaces the CIDAC register of the Rev. 0.11 MSCAN. In the Rev. 2.08 MSCAN, the equivalent CANIDAC register appears at address $xx0B.

Address Offset: $xx07

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	ABTRQ2	ABTRQ1	ABTRQ0	0	TXEIE2	TXEIE1	TXEIE0
Write:		ABTRQ2	ABTRQ1	ABTRQ0		TXEIE2	TXEIE1	TXEIE0
Reset:	0	0	0	0	0	0	0	0

Figure 15. Rev 0.11 Transmitter Control Register (CTCR)

Address Offset: $xx08

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
Write:						ABTRQ2	ABTRQ1	ABTRQ0
Reset:	0	0	0	0	0	0	0	0

Figure 16. Rev 2.08 Transmitter Message Abort Control (CANTARQ)

Rev. 0.11

Read: anytime
Write: only when SFTRST = 0

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 0

Bit 7 Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 6 Rev. 0.11

ABTRQ2 — Abort Request Transmit Buffer 2.

Rev. 2.08

No meaning, reads as '0'. ABTRQ2 is bit 2 in CANTARQ.

The MSCAN on the MC9S12DP256 compared with the MSCAN on the HC12 family   23

Bit 5   Rev. 0.11

ABTRQ1 — Abort Request Transmit Buffer 1.

Rev. 2.08

No meaning, reads as '0'. ABTRQ1 is bit 1 in CANTARQ.

Bit 4   Rev. 0.11

ABTRQ0 — Abort Request Transmit Buffer 0.

Rev. 2.08

No meaning, reads as '0'. ABTRQ1 is bit 0 in CANTARQ.

Bit 3   Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 2   Rev. 0.11

TXEIE2 — Transmit Buffer 2 Empty Interrupt Enable

Rev. 2.08

ABTRQ2 — Abort Request Transmit Buffer 2.

Bit 1   Rev. 0.11

TXEIE1 — Transmit Buffer 1 Empty Interrupt Enable

Rev. 2.08

ABTRQ1 — Abort Request Transmit Buffer 1.

Bit 0   Rev. 0.11

TXEIE0 — Transmit Buffer 0 Empty Interrupt Enable

Rev. 2.08

ABTRQ0 — Abort Request Transmit Buffer 0.

5.10 Transmitter Message Abort Acknowledge

The MSCAN12 Transmitter Flag Register (CTFLG) in Rev. 0.11 has been split up into two separate registers in Rev. 2.08 – The MSCAN Transmitter Flag Register (CANTFLG) and the MSCAN Transmitter Message Abort Acknowledge (CANTAAK). Here CTFLG is compared with CANTAAK.

Address Offset: $xx06

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	ABTAK2	ABTAK1	ABTAK0	0	TXE2	TXE1	TXE0
Write:								
Reset:	0	0	0	0	0	1	1	1

Figure 17. Rev 0.11 Transmitter Flag Register (CTFLG)

Address Offset: $xx09

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
Write:								
Reset:	0	0	0	0	0	1	1	1

Figure 18. Rev 2.08 Transmitter Message Abort Acknowledge (CANTAKK)

Rev. 0.11

Read: anytime
Write: only when SFTRST = 0

Rev. 2.08

Read: anytime
Write: unimplemented for ABTAKx flags

Bit 7 Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 6 Rev. 0.11

ABTAK2 — Abort Acknowledge Transmit Buffer 2.

Rev. 2.08

No meaning, reads as '0'. ABTAK2 is moved to bit 2.

The MSCAN on the MC9S12DP256 compared with the MSCAN on the HC12 family   25

Bit 5 Rev. 0.11

ABTAK1 — Abort Acknowledge Transmit Buffer 1.

Rev. 2.08

No meaning, reads as '0'. ABTAK1 is moved to bit 1.

Bit 4 Rev. 0.11

ABTAK0 — Abort Acknowledge Transmit Buffer 0.

Rev. 2.08

No meaning, reads as '0'. ABTAK0 is moved to bit 0.

Bit 3 Rev. 0.11 and Rev. 2.08

No meaning, reads as '0'.

Bit 2 Rev. 0.11

TXE2 — Transmit Buffer 2 Empty

Rev. 2.08

ABTAK2 — Abort Acknowledge Transmit Buffer 2.

Bit 1 Rev. 0.11

TXE1 — Transmit Buffer 1 Empty

Rev. 2.08

ABTAK1 — Abort Acknowledge Transmit Buffer 1.

Bit 0 Rev. 0.11

TXE0 — Transmit Buffer 0 Empty

Rev. 2.08

ABTAK0 — Abort Acknowledge Transmit Buffer 0.

5.11 MSCAN Transmitter Buffer Selection

The MSCAN Transmit Buffer Selection (CANTBSEL) register is new in Rev. 2.08. There is no equivalent in Rev. 0.11. The CANTBSEL register allows the selection of which actual transmit message buffer will be accessible in the CANTXFG register space.

Address Offset: $xx0A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	TX2	TX1	TX0
Write:								
Reset:	0	0	0	0	0	0	0	0

Figure 19. Rev 2.08 Transmitter Buffer Selection (CANTBSEL)

Rev. 2.08

Read: find the lowest ordered bit set to '1', all other bits will be read as '0'

Write: only when INITRQ = INITAK = 0

Bits 7–3 Rev. 2.08

No meaning, read as '0's.

Bits 2–0 TX2–TX0 — Transmit Buffer Select

The lowest numbered set bit places the associated transmit buffer in the CANTXFG register space. For example TX2=0, TX1=1 and TX0=1 selects transmit buffer TX0; TX2=0, TX1=1 and TX0=0 selects transmit buffer TX1. Note that if none of these bits are set, no transmit buffer is selected, writes to the CANTXFG register space will have no effect and reads will result in meaningless data. Note that a selected transmit buffer cannot be accessed if the corresponding TXEx bit is clear. When reading the TXx bits, only the lowest numbered set bit will be read as '1', the others will read as '0'.

    1 = The message buffer associated with this bit is selected, if this is the lowest numbered set bit.
    0 = The associated message buffer is deselected.

5.12 MSCAN Identifier Acceptance Control Register

Referred to as MSCAN12 Identifier Acceptance Control Register (CIDAC) in Rev. 0.11 and the MSCAN Identifier Acceptance Control Register (CANIDAC) in Rev. 2.08, there are no changes to the MSCAN Identifier Acceptance Control Register. Note that the there is a change of address of this register: in Rev. 0.11 the address is $xx08 whereas in Rev. 2.08 the address is $xx0B.

Rev. 0.11

Read: anytime
Write: only when SFTRST = 1

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 1

6 Error Counter Registers

6.1 MSCAN Receive Error Counter Register

Referred to as MSCAN12 Receive Error Counter (CRXERR) in Rev. 0.11 and the MSCAN Receive Error Counter Register (CANRXERR) in Rev. 2.08, there are no changes to the MSCAN Receive Error Counter Register.

Rev. 0.11

Read: only when SLPRQ = SLPAK = 1 or SFTRST = 1
Write: unimplemented

Rev. 2.08

Read: only when SLPRQ = SLPAK =1 or INITRQ = INITAK = 1
Write: unimplemented

6.2 MSCAN Transmit Error Counter Register

Referred to as MSCAN12 Transmit Error Counter (CTXERR) in Rev. 0.11 and the MSCAN Transmit Error Counter Register (CANTXERR) in Rev. 2.08, there are no changes to the Transmit Error Counter Register.

Rev. 0.11

Read: only when SLPRQ = SLPAK = 1 or SFTRST = 1
Write: unimplemented

Rev. 2.08

Read: only when SLPRQ = SLPAK =1 or INITRQ = INITAK = 1
Write: unimplemented

7 Identifier Filter Registers

7.1 MSCAN Identifier Acceptance Registers

Referred to as MSCAN12 Identifier Acceptance Registers (CIDAR0–7) in Rev. 0.11 and the MSCAN Identifier Acceptance Registers (CANRXERR) in Rev. 2.08. The only difference is that the reset state of the Identifier Acceptance registers are $00 in Rev. 2.08 as opposed to undefined after reset in Rev. 0.11.

Rev. 0.11

Read: anytime
Write: only when SFTRST = 1

Rev. 2.08

Read: anytime
Write: only when INITRQ = INITAK = 1

7.2 MSCAN Identifier Mask Registers

Referred to as MSCAN12 Identifier Mask Registers (CIDMR0–7) in Rev. 0.11 and the MSCAN Identifier Mask Registers (CANIDMR0–7) in Rev. 2.08. The only difference is that the reset state of the Identifier Mask registers are $00 in Rev. 2.08 as opposed to undefined after reset in Rev. 0.11.

Rev. 0.11

Read: anytime
Write: only when SFTRST = 1

Rev. 2.08

Read: anytime

8 Message Buffer Registers

8.1 Receive Message Buffer

In Rev. 0.11 MSCAN received messages are stored in a two stage input FIFO. In Rev. 2.08 MSCAN, this has been increased to a four stage FIFO structure. In Rev. 2.08 each buffer has a time stamp register. The address offset of the receive buffer window has also been changed. In Rev. 0.11 the receive buffer address offset is $xx40, whereas in Rev. 2.08 the receive buffer address offset is $xx20.

There have been no changes in the following:

Identifier Registers

Data Segment Registers

Data Length Register

The Rev. 2.08 Time Stamp register is described in section 8.3

Rev. 0.11 and Rev. 2.08

Read: only when RXF flag is set

Write: unimplemented.

8.2 Transmit Message Buffer

Rev. 0.11 MSCAN and Rev. 2.08 MSCAN both employ a three transmit buffers. In Rev. 0.11 MSCAN, all three transmit buffers are present in the CPU memory map at all times whereas in Rev. 2.08 MSCAN, only one transmit buffer is present in the CPU memory map at any given time. The desired transmit buffer is selected by setting the appropriate TXx bit in the MSCAN Transmit Buffer Selection register. In Rev. 2.08 each buffer has a time stamp register. The address offset of the transmit buffer window is $xx30.

There have been no changes in the following:

Identifier Registers

Data Segment Registers

Data Length Register

The Transmit Buffer Priority Register is undefined after reset in Rev. 0.11 and is initialized to $00 in Rev. 2.08, but is otherwise unchanged.

The Rev. 2.08 Time Stamp register is described in section 8.3

Rev. 0.11

Read: any time

Write: anytime

Rev. 2.08

Read: only when the corresponding TXx flag in CANTBSEL is the lowest set bit and the corresponding TXEx bit in CANTFLG is set

Write: only when corresponding TXx flag is the lowest set bit in CANTBSEL and the corresponding TXEx bit in CANTFLG is set; write of Time Stamp registers is unimplemented.

8.3 Time Stamp Register

The Time Stamp Register does not exist in the Rev. 0.11 specification. The following description is given in the Rev. 2.08 specification:

If the TIME bit is enabled, the MSCAN will write a special time stamp to the respective registers in the active transmit or receive buffer as soon as a message has been acknowledged on the CAN bus. The time stamp is written on the bit sample point for the recessive bit of the ACK delimiter in the CAN frame. In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timestamp value is taken from a free running internal timer which is clocked by the CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to '0') during the Initialization Mode. The CPU can only read the Time Stamp registers.

Address Offset: $xxxE

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
Write:								
Reset:	X	X	X	X	X	X	X	X

Figure 20. Rev 2.08 Time Stamp Register (TSRH – High Byte)

Address Offset: $xxxF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
Write:								
Reset:	X	X	X	X	X	X	X	X

Figure 21. Rev 2.08 Time Stamp Register (TSRL – Low Byte)

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