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Developing DSP56364 Software Using the DSP56362 EVM

by Miguel Moreno

This application note is intended for programmers that wish to develop DSP56364 software on a DSP56362EVM. The DSP56362EVM can be used to develop both DSP56364 RAM based solutions and custom mask ROM codes. This application note addresses the many functions, I/O, and memory map differences to ease the development of DSP56364 software .

This document summarizes from several existing documents including the *DSP56362 User's Manual* (DSP56362UM/D), the *DSP56364 User's Manual* (DSP56364UM/D), and the *56300 Family Manual* (DSP56300FM/AD). For a complete understanding of how to design your DSP56364 software on a DSP56362EVM please refer to the docements listed above.

1 Key Points

- DO NOT USE the 3X Timers, DAX (SP/DIF), HDI08 (unless for GPIO emulation) on the DSP56362.
- DO NOT USE the DSP56362 pins that don't exist on the DSP56364.
- DO NOT USE external data bus pins 8-23.
- DO NOT USE memory on the DSP56362 that cannot be supported on the DSP56364.

2 Hardware Peripheral Differences

The DSP56362 has many peripherals that should not be used when developing DSP56364 software. In Figure 1., we have highlighted the peripherals that should not be accessed on a DSP56362 because they do not exist on a DSP56364.

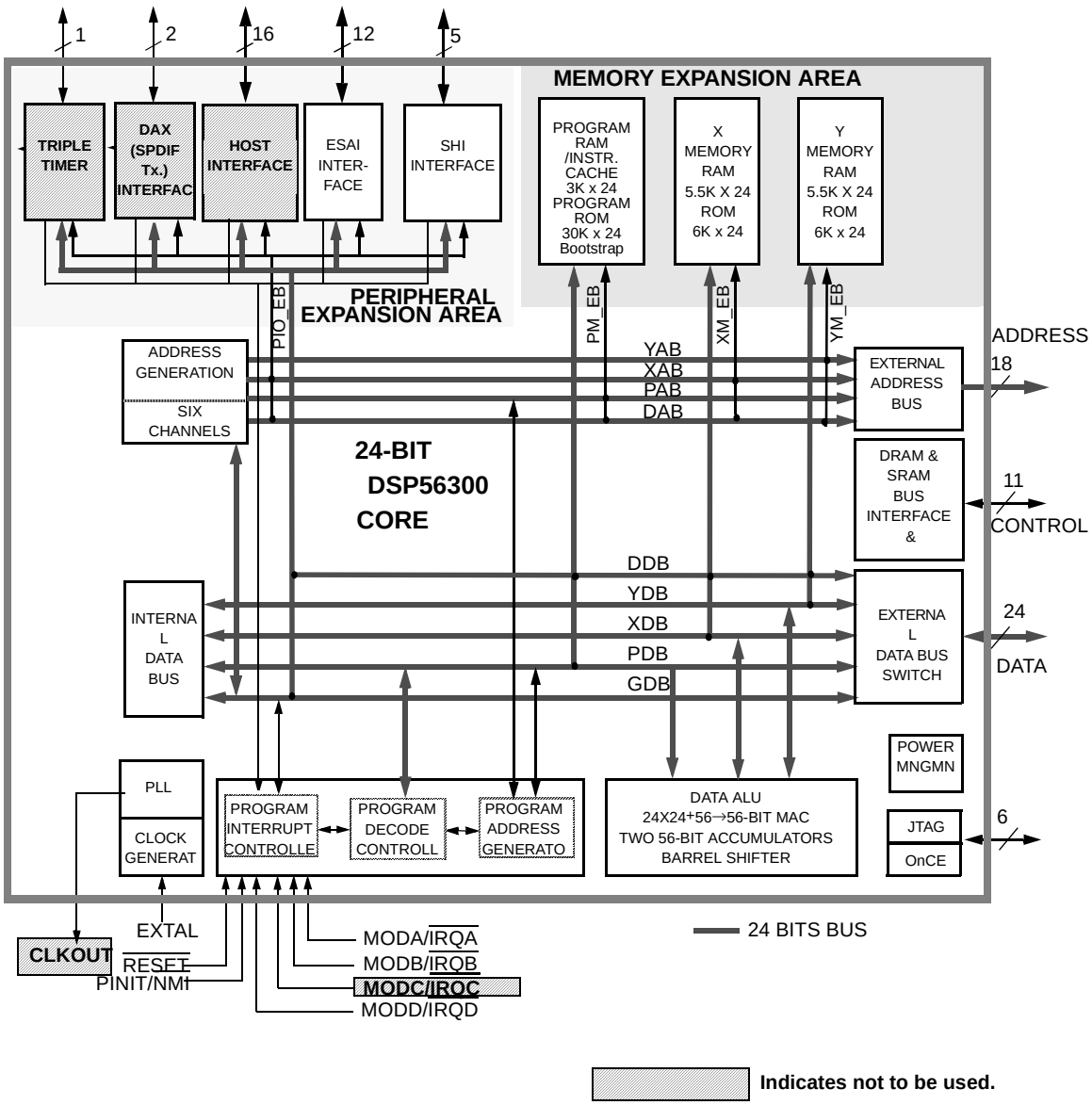

Figure 1. DSP56362 and DSP56364 Differences Diagram.

Triple Timers and DAX (SP/DIF) are core peripherals that should not be addressed. Other peripherals on the DSP56362 can be used to emulate the features of the DSP56364. For example, the DSP56362 HDI08 can be used to emulate the DSP56364 GPIO.

2.1 Emulating the DSP56364 GPIO on a DSP56362EVM

Users can emulate the GPIO peripheral of the DSP56364 using the HDI08 Host Interface peripheral of the DSP56362. To convert the HDI08 interface to GPIO, set the HPCR 16-bit read/write control register on the DSP56362. The Host port control register on the (HPCR)(X:$FFFFC4) on the DSP56362 can be set to many different formats, please refer to Section 6.5.6 in the DSP56362 User's Manual.

To configure the HDI08 for input or output, set the Host Data Direction Register (HDDR) (X: $FFFFC8) on the DSP56362 (section 6.5.7 DSP56362 user's manual). In addition, the Host Data Register (HDR) (X: $FFFFC9) holds the GPIO data value (section 6.5.8 DSP56362 user's manual).

When emulating the DSP56364 GPIO on a DSP56362 EVM remember to only use the four least significant bits of the GPIO since this is the limitation of DSP56364 GPIO.

Slight modifications of the software developed on the DSP56362 emulated GPIO will be needed when using DSP56364 hardware, please note the following register differences.

	DSP56364	DSP56362
GPIO Control Register	PCRB X:$FFFFCF	HPCR (X: $FFFFC4)
GPIO Direction Register	PRRB X:$FFFFCE	HDDR (X: $FFFFC8)
Data Register	PDRB X:$FFFFCD	HDR (X: $FFFFC9)

Refer to Section 6.5.6 in the *DSP56362 User's Manual* for additional information on the configuration of the HDI08 Host Port Control Register and Section 5 in the DSP56364 User's manual. The following section will explain the differences in I/O on core peripherals.

2.2 I/O Pin Differences

When creating software for the DSP56364, be aware of the extra I/Os and I/O differences on the DSP56362EVM.

2.2.1 PLL- Do not use the following:

Signal Name	Type
CLKOUT	Output

2.2.2 Program interrupt controller - Do not access the following:

Signal Name	Type
MODC/$\overline{\text{IRQC}}$	Input

2.2.3 JTAG - Do not access the following:

Signal Name	Type
$\overline{\text{TRST}}$	Input
$\overline{\text{DE}}$	input/output

3 EXTERNAL DATA BUS SWITCH

For external memory access, the DSP56364 uses an eight-bit data bus instead of the 24-bit data bus on the DSP56362. Use only the lowest eight significant bits of the 24 bit data bus to properly represent a DSP56364 data bus (DATA0-7).

3.1 DRAM/SRAM Bus Interface & I-Cache Control - Do not use the following:

Signal Name	Type
AA2-AA3	Output
$\overline{\text{RAS2-RAS3}}$	Output
$\overline{\text{BR}}$	Output
$\overline{\text{BG}}$	Output
$\overline{\text{BB}}$	input/output

Further information on the Signal/Connection Descriptions can be found in Section 2 of the *DSP56364 User's Manual* and the *DSP56362 User's Manual*.

4 Software Memory Map Differences

When programming for a DSP56364, pay careful attention to the memory map differences of the DSP56362. The DSP56362 memory is a superset of the DSP56364 memory, so when developing your software, you should be aware of the boundaries of the DSP56364 memory map. Use the following DSP56364 memory map as a guideline for your development. The DSP56362 memory map has also been included for reference.

4.1 DSP56364 Memory Maps

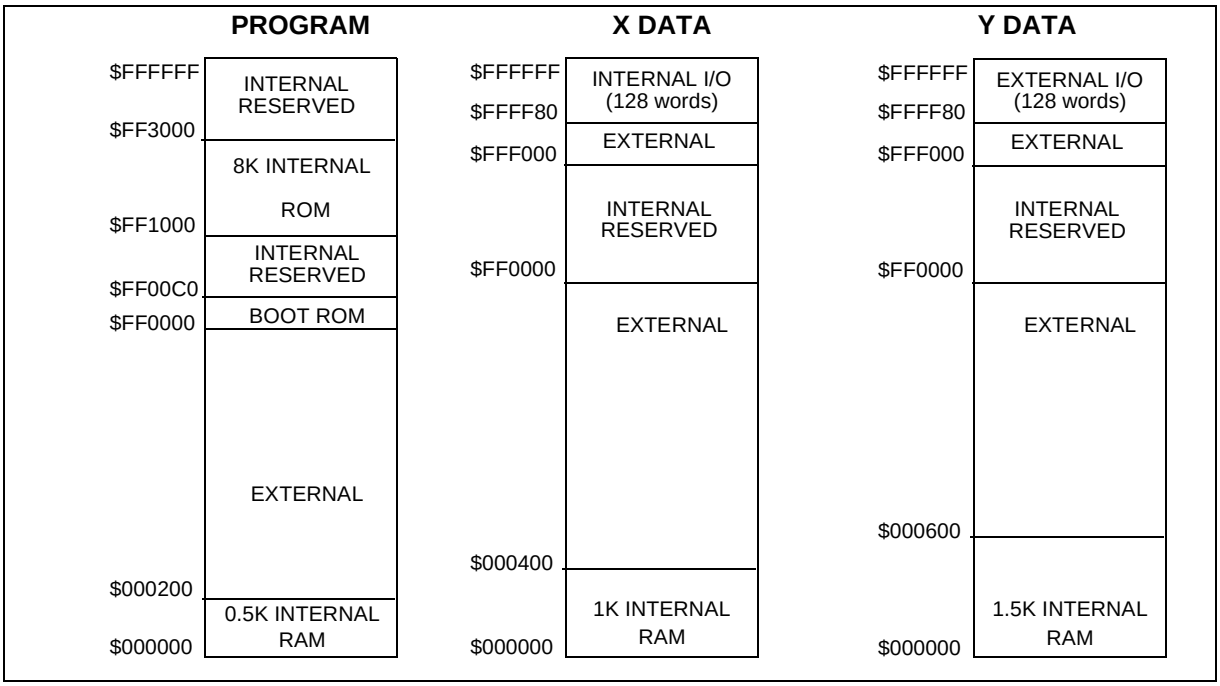

Figure 2. DSP56364 Memory Maps for MS=0, SC=0

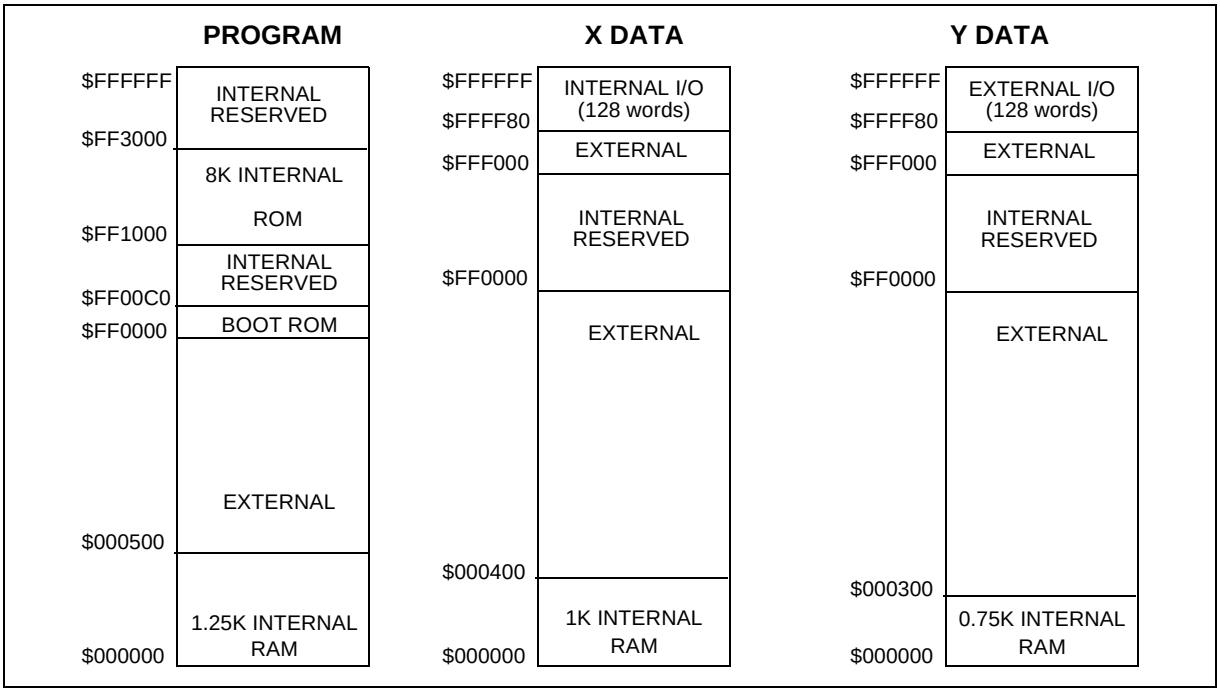

Figure 3. DSP56364 Memory Maps for MS=1, SC=0

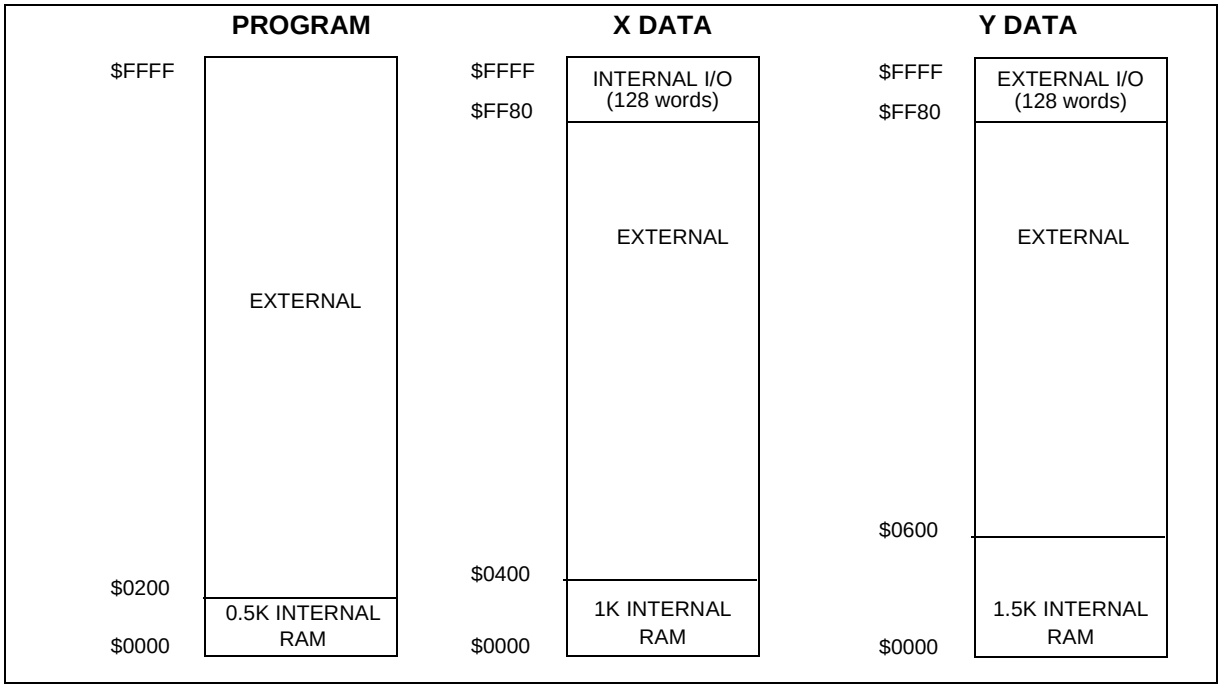

Figure 4. DSP56364 Memory Maps for MS=0, SC=1

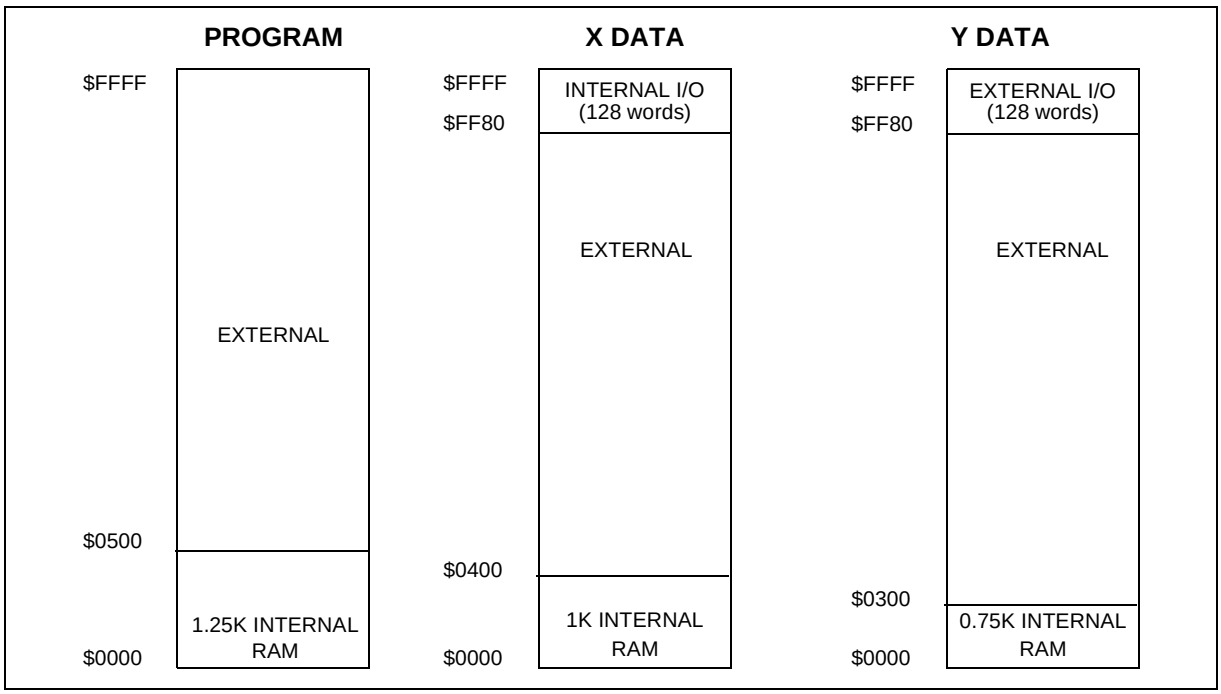

Figure 5. DSP56364 Memory Maps for MS=1, SC=1

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Table 1. DSP56364 On-chip RAM Memory Locations

BIT SETTINGS		RAM MEMORY LOCATIONS		
MS	SC	PROGRAM RAM	X DATA RAM	Y DATA RAM
0	X	$000000-$0001FF	$000000-$0003FF	$000000-$0005FF
1	X	$000000-$0004FF	$000000-$0003FF	$000000-$0002FF

Table 2. DSP56364 On-chip ROM Memory Locations

BIT SETTINGS		ROM MEMORY LOCATIONS	
MS	SC	PROGRAM ROM	BOOT ROM
X	0	$FF1000-$FF2FFF	$FF0000-$FF00BF
X	1	no access	no access

4.2 DSP56362 Memory Maps

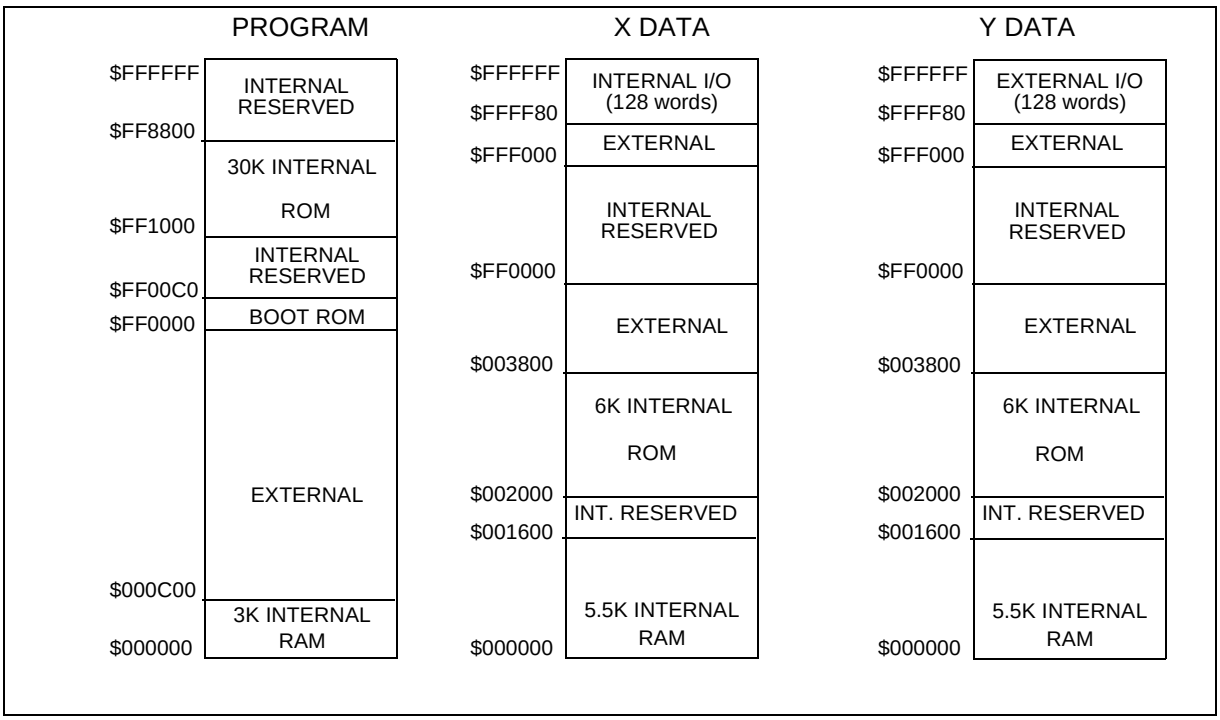

Figure 6. DSP56362 Memory Maps CE=0, MS=0, SC=0

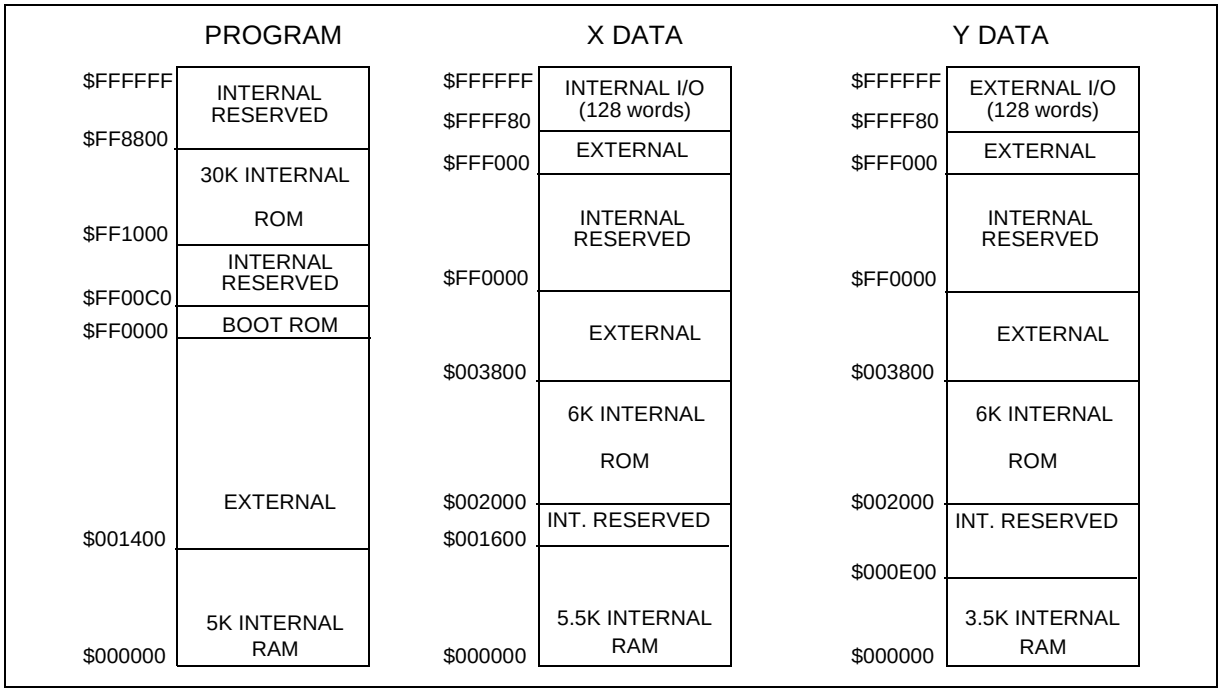

Figure 7. DSP56362 Memory Maps CE=0, MS=1, SC=0

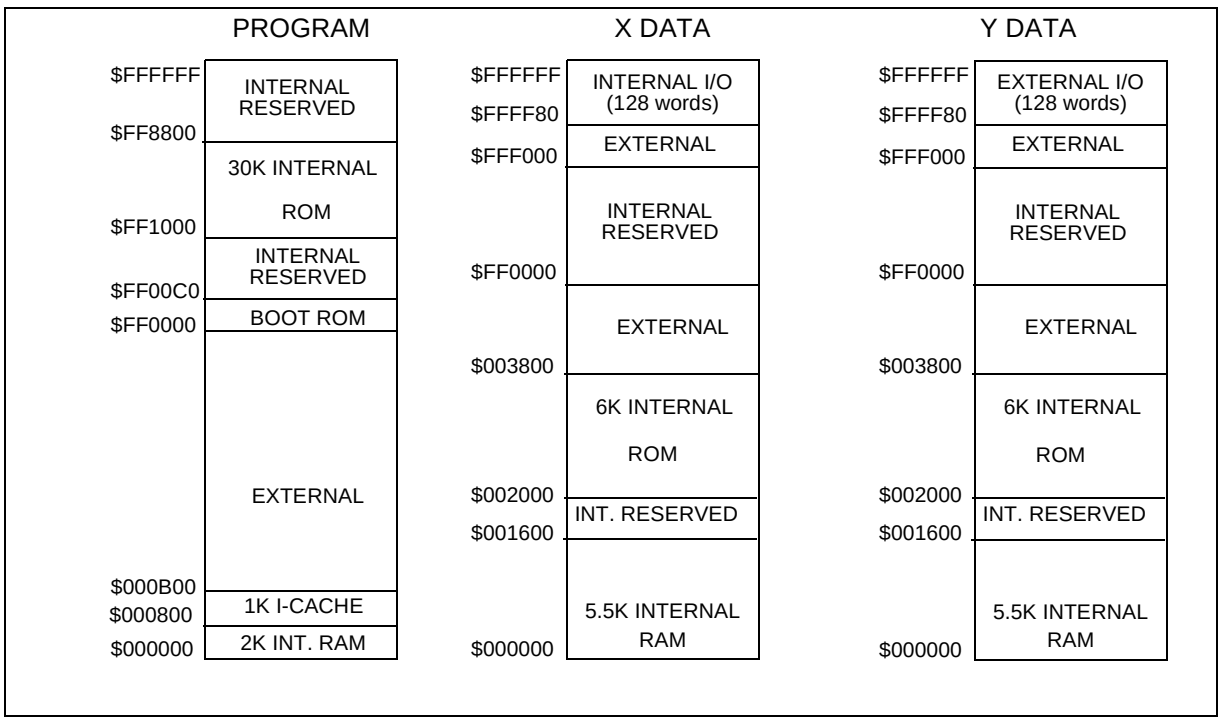

Figure 8. DSP56362 Memory Maps for CE=1, MS=0, SC=0

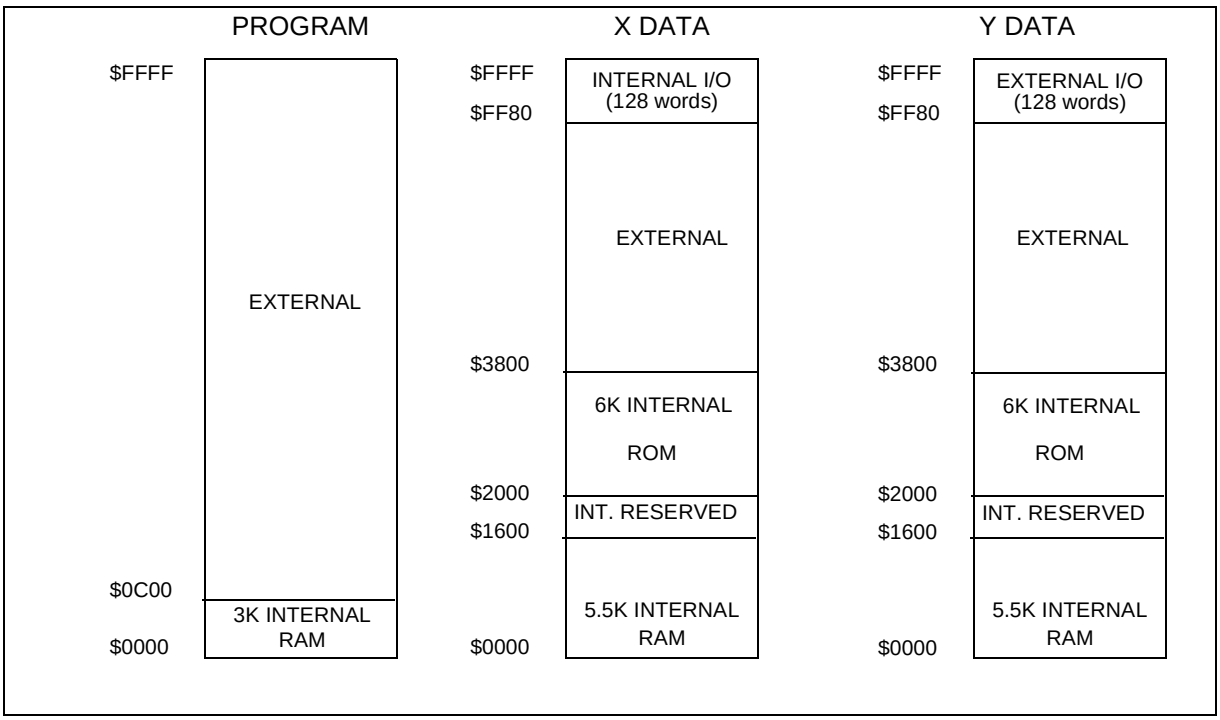

Figure 9. DSP56362 Memory Maps for CE=0, MS=0, SC=1

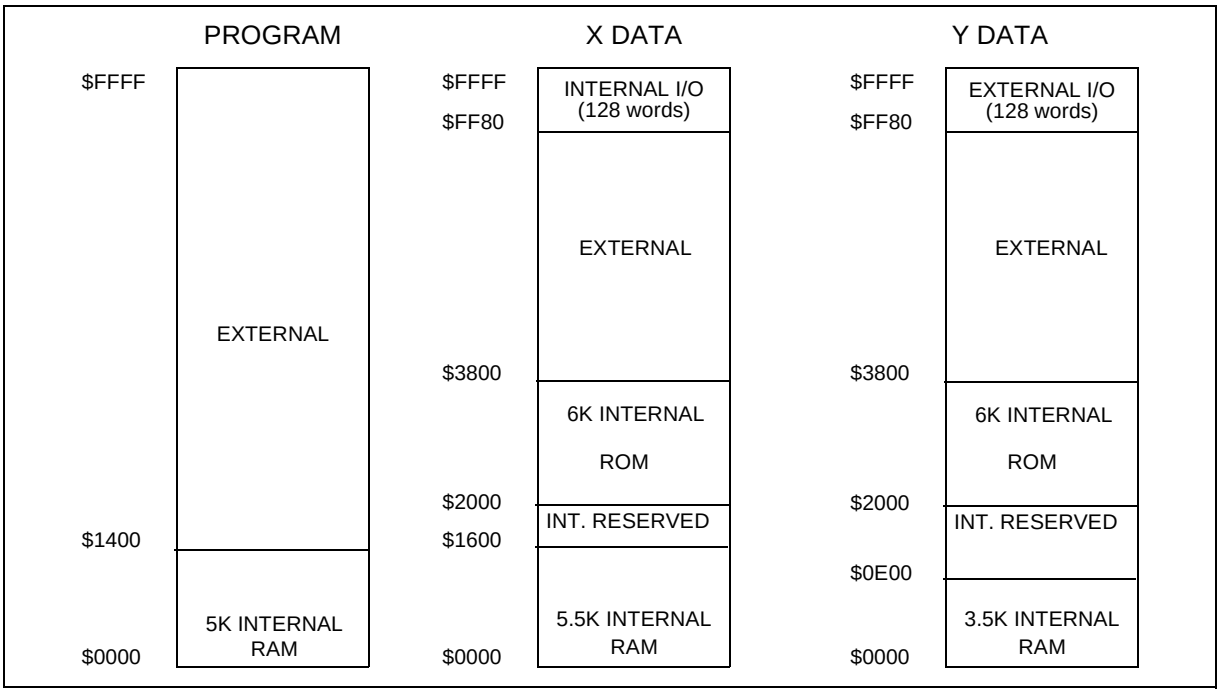

Figure 10. DSP56362 Memory Maps for CE=0, MS=1, SC=1

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Table 3. DSP56362 RAM Memory Locations

Bit Settings			RAM Memory Locations			
CE	MS	SC	Program RAM	Instruction Cache	X Data RAM	Y Data RAM
0	0	0	$0000-$0BFF	—	$0000–$15FF	$0000–$15FF
1	0	0	$0000-$07FF	$0800-$0BFF	$0000–$15FF	$0000–$15FF
0	1	0	$0000-$13FF	—	$0000–$15FF	$0000–$0DFF
1	1	0	$0000-$0FFF	$1000-$13FF	$0000–$15FF	$0000–$0DFF
0	0	1	$0000–$0BFF	—	$0000–$15FF	$0000-$15FF
1	0	1	$0000–$07FF	$0800-$0BFF	$0000–$15FF	$0000-$15FF
0	1	1	$0000–$13FF	—	$0000–$15FF	$0000-$0DFF
1	1	1	$0000–$0FFF	$1000-$13FF	$0000–$15FF	$0000-$0DFF

Table 4. DSP56362 On-Chip ROM Memory Locations

Bit Settings			ROM Memory Locations			
CE	MS	SC	Program ROM	Bootstrap ROM	X Data ROM	Y Data ROM
0	0	0	$FF1000–$FF87FF	$FF0000–$FF00BF	$002000–$0037FF	$002000–$0037FF
1	0	0	$FF1000–$FF87FF	$FF0000–$FF00BF	$002000–$0037FF	$002000–$0037FF
0	1	0	$FF1000–$FF87FF	$FF0000–$FF00BF	$002000–$0037FF	$002000–$0037FF
1	1	0	$FF1000–$FF87FF	$FF0000–$FF00BF	$002000–$0037FF	$002000–$0037FF
0	0	1	—	—	$2000–$37FF	$2000–$37FF
1	0	1	—	—	$2000–$37FF	$2000–$37FF
0	1	1	—	—	$2000–$37FF	$2000–$37FF
1	1	1	—	—	$2000–$37FF	$2000–$37FF

For further reference on memory configurations of the DSP56364 please refer to the *DSP56364 User's Manual* (DSP56364UM/D) section 3.