AN14603

S32K1xx Clock Robustness Design Guide

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Document information

Information	Content
Keywords	S32K1, Clock, Robustness
Abstract	S32K1 clock setup is a necessary step in almost all applications. Clock monitor is the key point in S32K1xx clock robustness design. For S32K11x, user needs to enable the SOSC clock monitor function with reset action and for S32K14x, user needs to enable the SOSC and PLL clock monitor functions with reset action. These will enhance the robustness of the S32K1xx clock.

1 Introduction

The S32K1xx series is NXP's 32-bit general purpose MCU family for automotive and industrial applications. This device supports four clock oscillators and, in S32K14x, one system phase locked loop (SPLL) for a total of up to five clock sources. There are also multiple input pins through which external clock signals can be driven into the MCU. Of the four oscillators, there is a system oscillator (SOSC), a 48 MHz fast internal RC oscillator (FIRC), a 2-8 MHz slow internal RC oscillator (SIRC), and a 128 kHz low-power oscillator (LPO). The SOSC can source from either a signal driven into the EXTAL pin or a crystal oscillator connected to the XTAL and EXTAL pins (henceforth referred to as "XTAL"). EXTAL can support up to 50 MHz, while there are two ranges that are allowed for the XTAL depending on configuration: 4-8 MHz or 8-40 MHz; FIRC can be trimmed to 48 MHz; SIRC can be either 2 MHz or 8 MHz. In addition, the SPLL on S32K14x devices supports frequencies from 90 MHz to 160 MHz.

2 Clock robustness design

Clock setup is a necessary step in almost all applications. Clock monitor is the key point in S32K1xx clock robustness design. It is imperative to adhere to the following guidelines to safeguard the device operation against loss of clock scenarios if the system clock source malfunctions because of any reason.

- System clock source SOSC/SPLL requirement: Ensure that the following sequence is followed while switching system clock to SOSC/SPLL:
  - System clock source (SOSC/SPLL) is enabled.
  - Clock monitors (SOSCCSR[SOSCCME] and SPLLCSR[SPLLCME]) and their corresponding reset event monitors (SOSCCSR[SOSCCMRE] and SPLLCSR[SPLLCMRE]) are enabled for SOSC/SPLL.
  - SOSC/SPLL is selected as system clock source.
- SOSC/SPLL clock monitor disable sequence requirement: Ensure that the following sequence is followed for disabling clock monitors while switching system clock source from SOSC/SPLL:
  - System clock source is switched from SOSC/SPLL.
  - Clock monitors (SOSCCSR[SOSCCME] and SPLLCSR[SPLLCME]) and their corresponding reset event monitors (SOSCCSR[SOSCCMRE] and SPLLCSR[SPLLCMRE]) are disabled for SOSC/SPLL.

Note: *The MCU internal monitor may still detect interference even no abnormality could be monitored by oscilloscope. For S32K11x, user needs to enable the SOSC clock monitor function with reset action and for S32K14x, user needs to enable the SOSC and PLL clock monitor functions with reset action. These will enhance the robustness of the S32K1xx clock.*

3 References

- S32K1XXRM, S32K1xx Series Reference Manual
- S32K1xx Clock Calculator Guide

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Also, note that the Arm attribution must be updated from "ARMnnn" to reflect the correct product name.

4 Revision history

Table 1. Revision history

Document ID	Release date	Description
AN14603 v.1.0	25 March 2025	Initial release

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