AN14577

S32Z2E2 Built-In Self-Test

Rev. 1.0 — 11 April 2025 **Application note**

Document information

Information	Content
Keywords	S32Z2E2
Abstract	This document describes how to configure and execute Built-In Self Test (BIST) for the NXP S32Z2/E2 Automotive Processors.

1 Self-test overview

The S32Z2/E2 microcontrollers include logic and memory Built-In Self-test (BIST) features. These features are designed to provide diagnostic coverage at device power up or shut-down/idle to ensure that logic and memory partitions do not contain permanent faults that might affect proper operation of the device.

The MCU implements BIST using a central self-test controller (CSTCU) and multiple local self-test controllers (LSTCUs) that cooperate to perform the full series of tests. These modules are highly programmable and customizable. As a result, and to ensure proper coverage and correct operation of the test procedure, only the test procedure and data provided with this application note might be used. Other configurations are not supported by NXP.

Start-up (also referred to as “power-up”) self-test is executed by the device’s boot ROM after the “Initialize 1” boot sequence. It is intended to be executed before the application is loaded and executed and it is run only after a Power-On Reset (POR) event.

Shut-down or Idle self-test (sometimes called “online” self-test in previous devices) might be initiated by application control, usually at an idle time or prior to shut-down. Running at this time might be advantageous if the amount of time required to run a self-test cannot be tolerated during start-up.

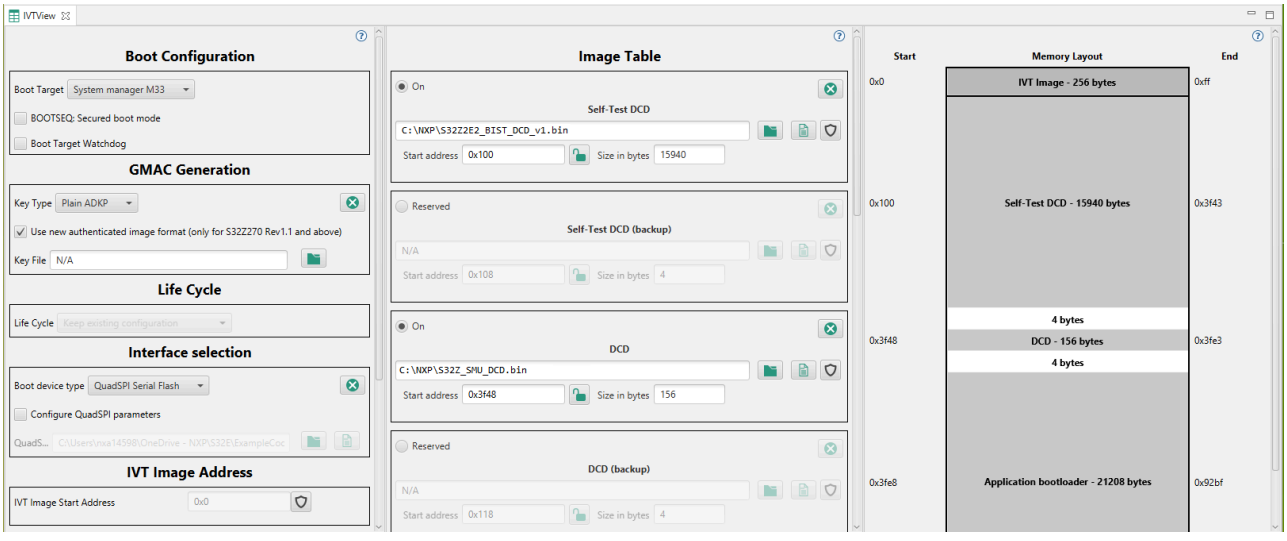
This application note describes both types of self-test initiation.

1.1 Start-up self-test

1.1.1 Configuration

Start-up self-test is configured by including the Device Configuration Data (DCD) binary image for self-test attached to this application note in the Image Vector Table (IVT) boot image. The IVT has pointers to the self-test Image and (optionally) back-up self-test image. The back-up image is simply a redundant copy of the primary self-test image and is used if the primary image should fail to be read or authenticated by the boot process.

If using the S32 Design Studio IVT Tool for configuration, simply enable the self-test DCD section and specify the filename of the binary self-test DCD image. It may be necessary to press “auto align” after doing so to arrange the blocks in the IVT image. Include the back-up image in the same way, if desired.



Include the application binary and specify the Boot Target and Type, the Export BLOB Image to create a bootable flash image containing both the start-up self-test and user application.

1.1.2 Start-up self-test execution

If properly configured in the IVT, no additional steps are necessary to execute self-test. This will occur automatically during application boot after a POR event. BootROM configures the central and local self-test controllers and initiates the test. Upon completion, the device goes through a functional reset and application boot will continue in the “Initialize 2” phase, followed by loading and executing the Hardware Security Engine (HSE) firmware (secure boot) or the application boot-loader (non-secure boot).

Whether a secure or non-secure boot, it is the responsibility of the application to check the status of self-test execution.

1.2 Shut-down self-test

Self-test may also be initiated by the software application at any time. Typically, this will be done during an idle time or prior to shut-down when there is sufficient time available to execute all tests. As with start-up self-test, a reset will occur when test execution is complete.

1.2.1 Preparing for shut-down self-test

There are three basic requirements to run self-test at an idle / shut-down time.

1. Stop running processes and disable interrupts.
2. Ensure any previous self-test run has completed.
3. Disable all active Clock Monitoring Units (CMU_FC)

1.2.1.1 Stop running processes

To ensure no interference from running processes or interrupts during the configuration or execution of shut-down self-test, begin by stopping application processes in RTU, FlexLLCE, and any process on the SMU core but the one conducting self-test.

Disable any peripheral interrupts that might occur during the configuration or executed phases of self-test.

1.2.1.2 Ensure previous self-test procedures are completed

This should be the case if the self-test is being run at a shut-down / idle time, but as a precaution simply read the CSTCU module’s Reset Domain Enable Status (RDENSTAT) fields. All bit fields should read as zero (disabled).

If these status bits do not all read back zero, then it is possible that a previous BIST run was aborted. Write 0 to all four bit fields of the Reset Domain self-test Enable (RDEN) register, and again poll RDENSTAT until it reads back zero.

1.2.1.3 Disable all active clock monitoring units

To avoid false triggering of Clock Monitoring alarms during the execution of self-test procedures, clear the Frequency Check Enable (FCE) bit in each CMU_FC instance’s Global Configuration Register (GCR).

1.2.2 Shut-down self-test configuration

Self-Test configuration consists of setting up MBIST, LBIST, and general CSTCU/LSTCU parameters for the full test run. Below is an outline of this procedure, however this contains many chip-specific details and register settings, not all of which are documented in the User Reference Manual. For full detail of the necessary procedure use as a reference the attached source code files: STCU.C, STCU.h, MMC_GLS_FULL.c, and MMC_GLS_FULL.h.

1.2.2.1 MBIST

1. Set CSTCU.LSCHLVD[MBPLVLD] = 1 to enable MBIST.
2. Perform MTR MBIST configuration.
3. Configure CSTCU's LMBPTR0 through LMBPTR17 to schedule the MBIST sequences.

1.2.2.2 LBIST

1. Set CSTCU.LSCHLVD[LBPLVLD] = 1 to enable LBIST.
2. Perform LBIST MMC Setup
3. Configure CSTCU's LLBPTR0 through LLBPTR17 to schedule LBIST sequences.

1.2.2.3 General CTSTCU/LSTCU

1. Write 1 to CSTCU.RDEN fields SERD0, SERD1, and SERD2 to enable SMU and both RTU domains.
2. Wait for CSTCU.RDENSTAT not equal to 7.
3. Clear to zero the recoverable and unrecoverable error status bits RFSF and UFSF in CSTCU.ERR_STAT.
4. Set LB_DELAY = 15 and MB_DELAY = 15 in CSTCU.STAG and all LSTCU_n.STAG registers to slightly stagger the starts of concurrent LBIST and MBIST partitions.
5. Set RTU0/1__LSTCU0/1.MBPTR registers MBEOL field to 0 and MBPTR field to 1.
6. Set RTU0/1__LSTCU0/1.PH1_DUR[PH1DUR] = 0x3ff.
7. Set RTU0/1__LSTCU0/1.MBPTR0[MBCSM] = 1 to enable concurrent MBIST.

1.2.3 Shut-down self-test execution

Self-test execution is started simply by setting CSTCU.RUNSWREG[RUNSW] = 1. After this, the application may enter an idle loop. The device will automatically issue a functional reset when it completes the self-test procedure.

1.3 Checking self-test results

Regardless of the method chosen for self-test execution, as noted, a reset follows completion of the test procedure. Upon entry into the application code after self-test execution and reset, results can be checked by following these steps:

As a preliminary check, first look at the Reset Generation Module's Destructive and Functional Reset Status registers (MC_RGM.DES and MC_RGM.FES). If MC_RGM.DES[3] or MC_RGM.DES[4] is set, this indicates a BIST destructive reset occurred and the previous self-test run overall failed in an unrecoverable way (e.g. Watchdog reset). No results need be checked. The device should be placed in a safe-state.

If MC_RGM.FES[4] is set, then the previous reset was due to a completed self-test run. If this is the case, the following procedure may be followed to check detailed results.

- Read CSTCU's ERR_STAT[ABORTHW] field. If set to 1, a hardware abort was received during the self-test procedure. Results are invalid and should be ignored. It is recommended to re-run the test procedure by requesting a Power On Reset (POR).
- Read CSTCU's ERR_STAT[UFSF] and ERR_STAT[RFSF] fields to determine if any Unrecoverable or Recoverable error events were logged during the self-test run. If both fields are 0, the test ran successfully and the rest of this procedure may be skipped.
- In the case that there is any error indicated in ERR_STAT, check to ensure the LSTCU pointers for both Logic (LBIST) and Memory (MBIST) are valid by reading the CSTCU's ERR_STAT[INVP_LB] and ERR_STAT[INVP_MB] fields. If either or both bits are set, this may indicate a configuration error. This is an unexpected result since the configuration provided in this application note is correctly structured, however

it might indicate that there was an error reading the configuration. If re-running self-test after another POR indicates the same error, then it may indicate a device failure or a corrupt non-volatile memory.

- (Optional) If LBIST and MBIST pointers are valid, check which local self-test controllers (LSTCUs) reported errors by reading the CSTCU's LRFSTAT0 and LUFSTAT0 registers. For any bit which is set to 1 in either register, determine if this was an LBIST or MBIST failure by reading the corresponding LSTCU's MB_RSTATn and LB_RSTAT0 registers. This only provides some additional detail on the failure location. It is already known at this point that a failure has occurred. The application should at this point log the error and enter a fail-safe state.

1.4 Using the attached self-test source code

The attached source code provides a main procedure for starting a shut-down self-test execution as detailed in this application note. Include the attached source code files in the application build and then invoke function SetupAndRunSTCU() to configure and execute BIST. This is intended to be executed from the System Manager Unit (SMU) CM33 core.

It is recommended to include the steps in "Checking Self-Test Results" above first. Check MC_RGM FES and DES registers as described. If a self-test procedure is not indicates by the reset status registers then execute SetupAndRunSTCU(). If DES and FES indicate a completed BIST run, then check results as described.

Since the self-test involves a system reset after completion, demonstrating this procedure is best done using an external flash or SD-Card boot configuration for the MCU such that the application is able to execute again immediately after reset to check results.

2 References

2.1 NXP references

Table 1. NXP document references

Document ID	Document Title	Source
RM638609	S32Z27 Reference Manual	NXP Secure Files
RM716503	S32E27 Reference Manual	NXP Secure Files
DS718401	S32Z27 Data Sheet	NXP Secure Files
DS718301	S32E27 Data Sheet	NXP Secure Files

2.2 External references

This guide is supplementary to the S32ZSE Reference Manual and Data Sheet.

The following documentation provides useful information about the Arm processor architecture:

- For information about the Arm Cortex-R52 processor, see: https://developer.arm.com/ip-products/processors/cortex-r/cortex-r52
- For information about the Arm Cortex-M33 processor, see: https://developer.arm.com/ip-products/processors/cortex-m/cortex-m33

3 Acronyms and definition

Table 2. Acronyms and definition

Acronym	Definition
ARM	Advanced RISC Machines processor architecture

Table 2. Acronyms and definition...*continued*

Acronym	Definition
BGA	Ball Grid Array package
BOM	Bill of Materials
BSDL	Boundary Scan Description Language
CAN	Controller Area Network
DDR	Dual Data Rate DRAM
EEPROM	Electrically Erasable Programmable Read-Only Memory
ETM	Embedded Trace Macrocell
GND	Ground
GPIO	General Purpose Input/Output
I^2C	Inter-integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	Input Output Multiplexing
JTAG	Joint Test Action Group
LDO	Low Drop-Out regulator
LPDDR4	Low Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
LIN	Local Interconnect Network
MAC	Media Access Control
MDIO	Management Data Input/Output
MII	Media Independent Interface
NC	Not Connect
NMI	Non-Maskable Interrupt
ODT	On-Die Termination
PCB	Printed Circuit Board
PDN	Power Delivery Network
PHY	Physical Layer Interface
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
QSPI	Quad serial peripheral interface.
RGM	Reset Generation Module
RGMII	Reduced Gigabit Media Independent Interface
ROM	Read-Only Memory
SDHC	Secure Digital High Capacity
SDR	Single Data Rate

4 Revision history

Table 3. Revision history

Document ID	Release date	Description
AN14577v.1.0	11 April 2025	Initial public release

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