AN14301

S32K344 to S32K39/S32K37 Migration Guide

Rev. 1.0 — 25 March 2025 Application note

Document information

Information	Content
Keywords	S32K396, S32K344, Migration, Features comparison
Abstract	The document describes main differences between S32K344 and S32K396 family devices. It helps customers quickly migrate from S32K344 to S32K396.

1 Introduction

This document compares the features of the S32K344 to the S32K396 family of devices and identifies differences that affect the migration of an application. The S32K3 MCUs of 32/bit AEC-Q100 qualified MCUs combine a scalable family of Arm® Cortex- M7® cores-based microcontrollers in single, dual, and lockstep core configurations, supporting up to ASIL D function safety automotive and industrial applications.

2 Context

Figure 1 shows the compatibility of the new S32K39/7 device with its predecessor S32K34x and the new S32K35x device being developed in parallel. All the S32K3xx shares the same architecture. S32K39/7 offers higher performances and extended analog/timers modules. Software written for S32K344 can be effortlessly ported to S32K39/7. In the 289 MapBGA package, the certain pin compatibility is kept between the S32K344 and S32K396 devices. Additional new pin functions are assigned to new peripherals.

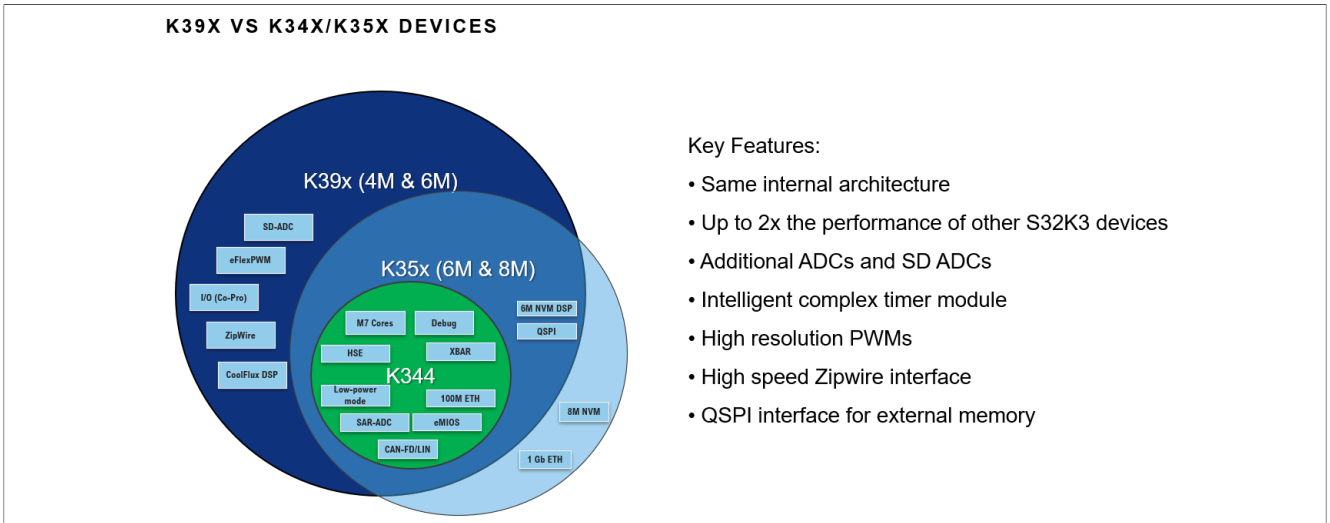


Figure 1. Intersection content of S32K3xx family

3 Comparison with S32K344

The following table compares some of the prominent features between S32K344 and S32K396.

Table 1. S32Kxx family feature comparison

feature	S32K344	S32K396/394	S32K376/374
Safety/ASIL	ASIL D		
Number of CPU cores	2 x Arm Cortex M7 @ 160 MHz	4 x Arm Cortex M7 @ 320 MHz	
Core configuration	1x LS Cortex-M7	2x M7 Lockstep or 1x M7 LS + 2 M7 split lock	
Program flash memory (MB)	4	6/4	6/4
OTA (A/B swap)	Yes (hardware) limited to 2M		
Data flash memory (KB)	128		

Table 1. S32Kxx family feature comparison*...continued*

feature	S32K344	S32K396/394	S32K376/374
Total RAM (KB)	512 KB (incl 192 kB TCM)	800 KB (including 64 KB Standby RAM and 288 KB TCM)	
Standby RAM (KB)	32	64	
Security	HSE_B		
DMA	1x32 Channels	2 x 32 channels (1x 32 channels Lock step)	
Max performance	N/A	2054[1] Mixed ASIL 1 Core in Lockstep (ASIL D) and 2 cores in split lock (ASIL-B)	
ASIL–D DMIPS	342–516[2]	1369	
eTPU	N/A	2x engines @ 320MHz (2x32 ch)	N/A
Coolflux DSP	N/A	160 MHz	
eFlexPWM	N/A	2 x eFlexPWM/Nanoedge (8 channels each)	
FlexCAN (FD)	6		
Ethernet MAC	1 x 10/100 Mbit/s		
LPUART (LIN)	16	4	
Zipwire	N/A	1	
QSPI	1		
LPSPI	6		
MSC (LVDS-DSPI + LPUART)	N/A	1	
I2C	2		
FlexIO	32 channels	8 channels, 32 pins (Emulating UART, I2C, SPI, I2S, SENT, PWM, Camera I/F)	
SAR ADC	3	7	
SDADC	N/A	4	
SWG	N/A	2x 10 bit	
ACMP/LCMP	3	2	
PIT	3		
SWT	1	3	
STM	2	3	
LCU	2		
BCTU	1	2	
TRIGMUX	1	2	
eMIOS	3x24 channels	1x 24 channels	
RTC	1		
289 MapBGA	-	Y	
257 MapBGA	Y	-	
176 LQFP	-	Y	

Table 1. S32Kxx family feature comparison*...continued*

feature	S32K344	S32K396/394	S32K376/374
172 MaxQFP	Y	-	

1. Cortex-M7 DMIPS/MHz 2.14-3.23.
2. Final DMIPS is in a range based on compiler setting. The low number uses the "ground rules" laid out in the Dhrystone documentation. The high number uses the inlining of functions of a simultaneous ("multifile") compilation.

Color wheel description:

Common for all the devices
S32K344 specific / don’t care for K39x and k37x design
S32K37x + S32K39x specific (new compared to S32K344)
S32K39x specific

In summary: S32K344 vs S32K396

- In addition to the new modules in S32K396, the other main difference is the number of modules. Some modules have also been slightly changed.
- Increase the number of cores to 4, one pair of cores is in permanent lock-step. The other pair of cores can be either lock-step or split-lock, so up to 3 cores could be used in total. The system clock frequency has been increased from 160MHz to 320MHz.
- Except for some changes in the number and content of EIM, ERM, and FCCU channels, the safety, and security solutions on S32K344 are same as S32K396.
- S32K396 176 LQFP is not compatible with the S32K344 172 MaxQFP package. They are two different packages.

4 Platform architecture

Figure 2 shows the block diagram for S32K396.

Figure 3 shows the block diagram for S32K344. The main differences are shown in Table 2.

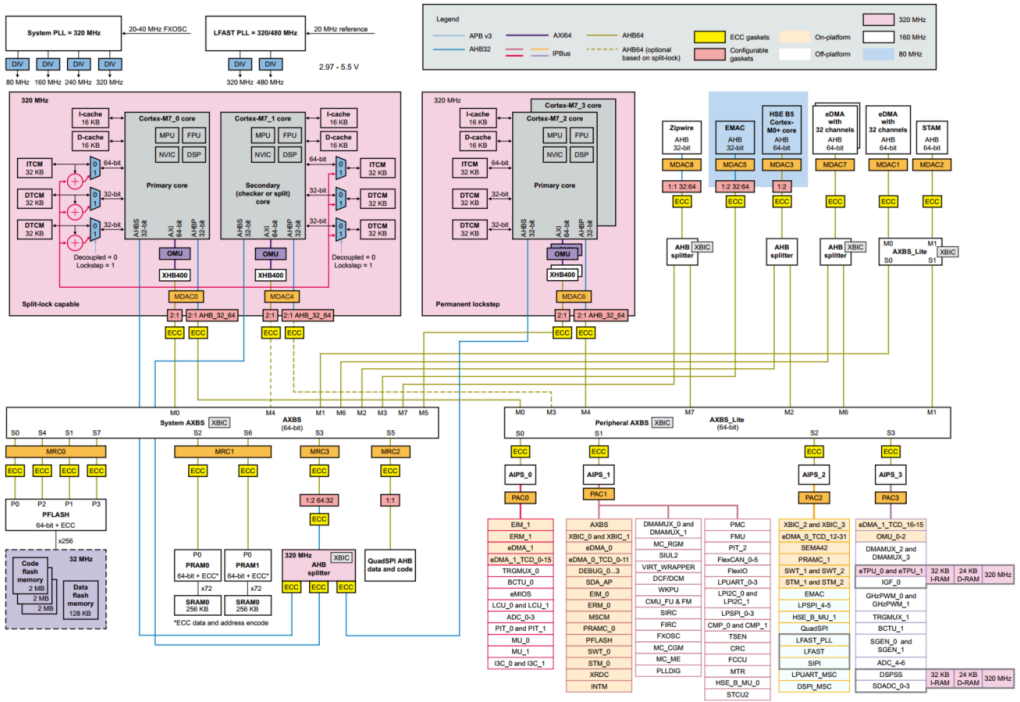


Figure 2. S32K396 block diagram

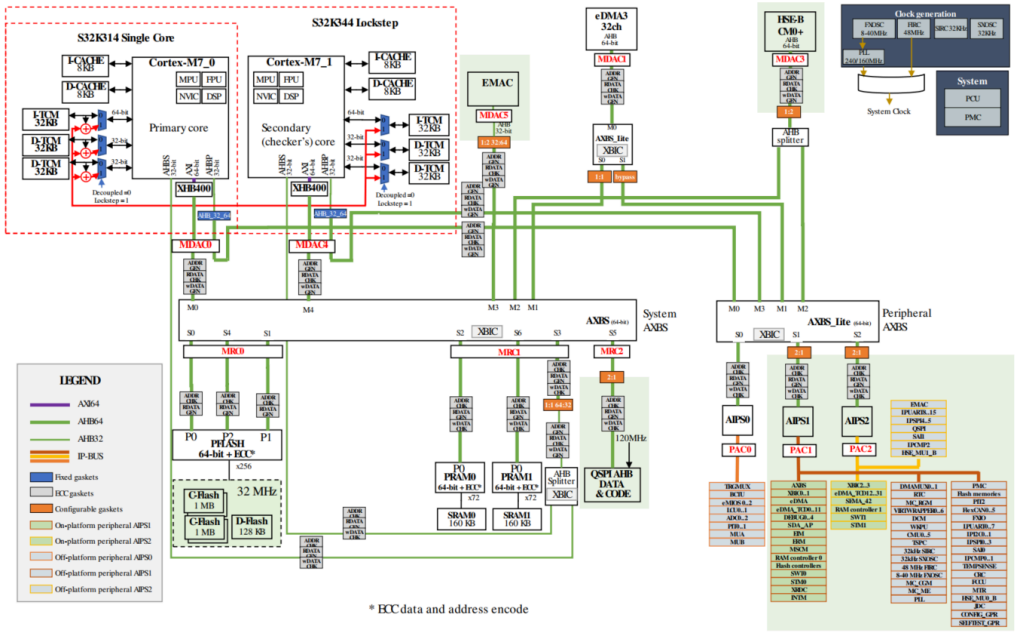


Figure 3. S32K344 block diagram

The platform architectures of both are basically the same. S32k396 add some new peripherals, for example, SDADC, Zipwire, eTPU, eFlexPWM, SWG, and CoolFlux DSP.

Table 2. Platform differences

Feature	S32K344	S32K396
Cores	ARM Cortex M7_0/1	ARM Cortex M7_0/1/2/3

Table 2. Platform differences*...continued*

Feature	S32K344	S32K396
System clock	160 MHz	320 MHz
XBAR	System and peripheral	System and peripheral
AIPS3	No	Yes

5 Module features difference

5.1 Core and systems

5.1.1 OMU

The S32K396 devices support calibration by the use of the Overlay Management Unit, it has 4x OMU instance.

- Two are added in permanent lockstep mode for two cores in permanent lockstep mode
- Two in slit-lock mode, for the other 2 cores in split-lock mode

There is no OMU on the S32K344.

5.1.2 MSCM

MSCM provides information of the system cores and can identify the core that is running currently. As compared with S32K344, since three cores are on S32K396, the number of registers that define the configuration information for the core increases to three. Register interrupt router CPn interrupt generation (IRCP0IGR0 - IRCP1IGR3) and interrupts router CPn interrupt status (IRCP0ISR0 - IRCP1ISR3), where n increased to three. In addition, this module provides more AHB gasket configuration (IAHBCFGREG) features.

5.1.3 TSPC

No TSPC on S32K396.

5.1.4 AXBS_lite

The crossbar switch connects bus masters and bus slaves using a crossbar switch structure.

S32K396 has seven AXBS, as compared to S32K344, two more AXBS are added for DMA1 and Zipwire.

5.1.5 eDMA

S32K396 has two eDMA instances, each having 32 channels. Whereas eDMA_1 is in lockstep for self-check . S32K344 supports 1x DMA, not in lock-step.

5.1.6 DMAMUX

The Direct Memory Access Multiplexer (DMAMUX) routes DMA sources, called the slot, to any of the 16 DMA channels. S32K396 has four DMAMUX instances, DMA channel configuration registers 0-3 support a periodic trigger function. S32K344 has two DMAMUX, all DMA channel configuration registers support periodic trigger functions. DMAMUX_0 and DMAMUX_1 channels are mapped to eDMA_0 channels and DMAMUX_2 and DMAMUX_3 channels are mapped to eDMA_1 channels.

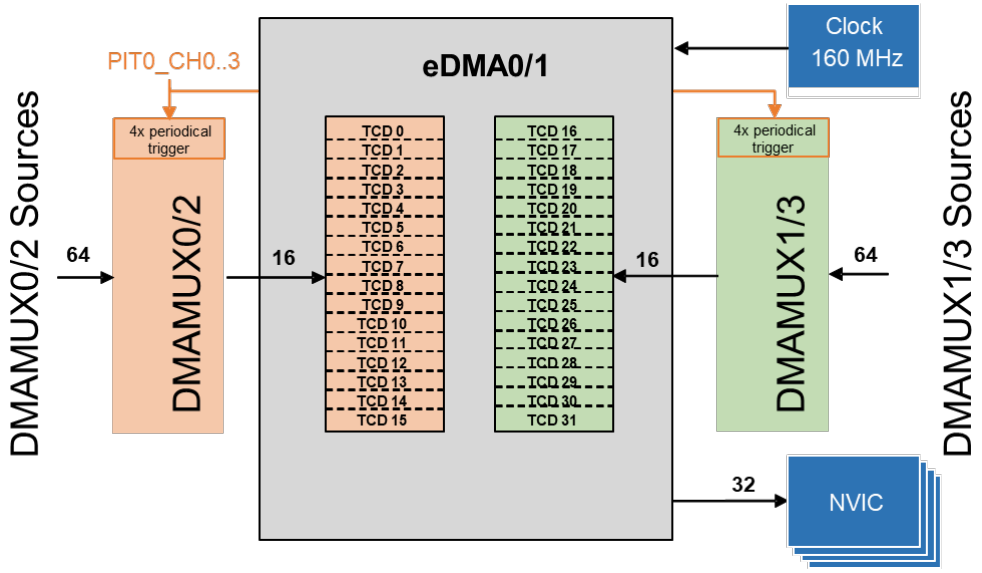


Figure 4. DMAMUX block diagram

5.1.7 XBIC

Table 3 shows the differences of XBIC for S32K344 and S32K396.

Table 3. XBIC differences

Feature	S32K344	S32K396
Instances	4 instances	6 instances Added 2 instances for eDMA and Zipwire

5.2 Memories and memory overview

The following table shows the differences of memories for S32K344 and S32K396.

Table 4. Memory general differences

Feature	S32K344	S32K396
Program flash memory	4 MB	Up to 6 MB
Data Flash	128 KB	128 KB
Flash memory controller cache	Up to four pages of data (256-bit page size) may be buffered in each prefetch buffer for AHP Port 0, Port 1, and Port 2	Up to four pages of data (256-bit page size) may be buffered in each prefetch buffer for AHP Port 0, Port 1, Port 2 and Port 3
RAM	512 KB SRAM (including 384 KB TCM)	800 KB SRAM(including 288 KB TCM)
Standby RAM	32 KB	64 KB
QuadSPI (External Memory interface)	1 instance with up to 4-bit bidirectional data lines.	1 instance with up to 8-bit bidirectional data lines. Hyper RAM feature supported. For more details, see the QuadSPI section.
Error Correcting code	YES	YES

Table 4. Memory general differences*...continued*

Feature	S32K344	S32K396
Cache	8 KB data and 8 KB instruction cache for each CM7 Core	16 KB data and 16 KB instruction cache for each CM7 Core
EEPROM	By Software	By Software

The memory configuration for S32K396 is the same as the configuration of S32K344, including Embedded Flash Memory (c40asf), Flash Memory Controller (PFLASH) and RAM Controller (PRAMC).

There is a few new Master ID added for new modules, such as EMAC, Zipwire, eDMA1 and Cortex-M7_2 on the S32K396.

5.3 Clocking

5.3.1 Clock sources

There are four clock sources available on S32K396 as compared to S32K344, differing in that S32K396 does not have support for a slow external oscillator (SXOSC).

Parameters of the other clock sources remain the same as on the S32K344 device.

5.3.2 System clocks

Main system clocks are generated using MC_CGM MUX_0. Compared to S32K344, there is one more divider to support the generation of CM7_CORE_CLK as the main clock for cores. CORE_CLK is used as a crossbar, peripheral bridge, SRAM, flash memory, QSPI, and fast-speed peripheral clock. In contrast to S32K344 where this clock is also used as a source for CM7 cores. QSPI_MEM_CLK is double the frequency compared to S32K344 since the core clock is also doubled. See the summary in the table below.

Table 5. System clock comparison between s32k39 and s32k344

System clock node	System Clock divider	Maximum frequency	
		S32K344	S32K396
CORE_CLK	MC_CGM.MUX_0_DC_0[DIV]	160 MHz	160 MHz
AIPS_PLAT_CLK	MC_CGM.MUX_0_DC_1[DIV]	80 MHz	80 MHz
AIPS_SLOW_CLK	MC_CGM.MUX_0_DC_2[DIV]	40 MHz	40 MHz
HSE_CLK	MC_CGM.MUX_0_DC_3[DIV]	120 MHz	120 MHz
DCM_CLK	MC_CGM.MUX_0_DC_4[DIV]	48 MHz	48 MHz
LBIST_CLK	MC_CGM.MUX_0_DC_5[DIV]	48 MHz	48 MHz
QSPI_MEM_CLK	MC_CGM.MUX_0_DC_6[DIV]	160 MHz	320 MHz
CM7_CORE_CLK	MC_CGM.MUX_0_DC_7[DIV]	-	320 MHz

5.3.3 Clock generation MC_CGM

S32K396 supports additional multiplexers MUX_13_DC_0[DIV] for STM2 clock, MUX_15_DC_0 for LFAST, and MUX_16_DC_0 for SWG clock.

There is an additional CMU_FC_6 implemented on S32K396 to monitor CM7_CORE_CLK over and under frequency with FXOSC as a reference clock.

5.4 Security and device GPRs

The security configurations for HSE_B, DCF records, DCM_GPR, DCM, and MU on S32K396 are almost the same as the configuration on S32K344. No huge difference between them.

There is an extension for QuadSPI SFP at the Configuration_GPR memory map, which responds to the configuration for QuadSPI SFP access.

There is an extension in the DCM_GPR register, which is extended for Cortex-M7_2 and other new IP or instances, like eTPU and eDMA1. An additional MU_2 is added on S32K396, which is used for communication between application cores.

5.5 Modes and power management

5.5.1 PMC

Table 6 shows the differences between power management controllers for S32K344 and S32K396.

Table 6. PMC differences

Feature	S32K344	S32K396
Bandgaps	No	Two bandgaps to enable independent supply generation and monitoring
LVR monitors	No	Two independent LVR monitors for each safety relevant power supply domain

Figure 5 shows the power management system block diagram for S32K396. Figure 6 shows the power management system block diagram for S32K344.

The key difference here is that for generating the V11 (generated by the PMC module internally by the linear regulator), there is essential to have an external NMOS with low-threshold voltage, having a connected NMOS_CTRL output pin to its gate on S32K396 to regulate a 1.5 V supply (V15 either provided externally or generated by internal SMPS) down to core voltage (V11). The V15 pin is not a high current input (used for voltage sensing) as compared to S32K344 devices where V11 is generated internally with no external NMOS required and V15 is a high current input.

The following are the additional supply domains as compared to S32K344:

- VDD_SD_ADC0, VDD_SDADC1: Power supply domain for sigma-delta ADCs. Those power supply inputs must be shorted to the VDD_HV_A domain at the PCB level.
- VDD_SWG: Power supply domain for the sine wave generators. This power supply input must be shorted to the VDD_HV_A domain at the PCB level.
- VDD_LVDS: Power supply domain for the 3.3V LVDS interface used by the Zipwire communication module.

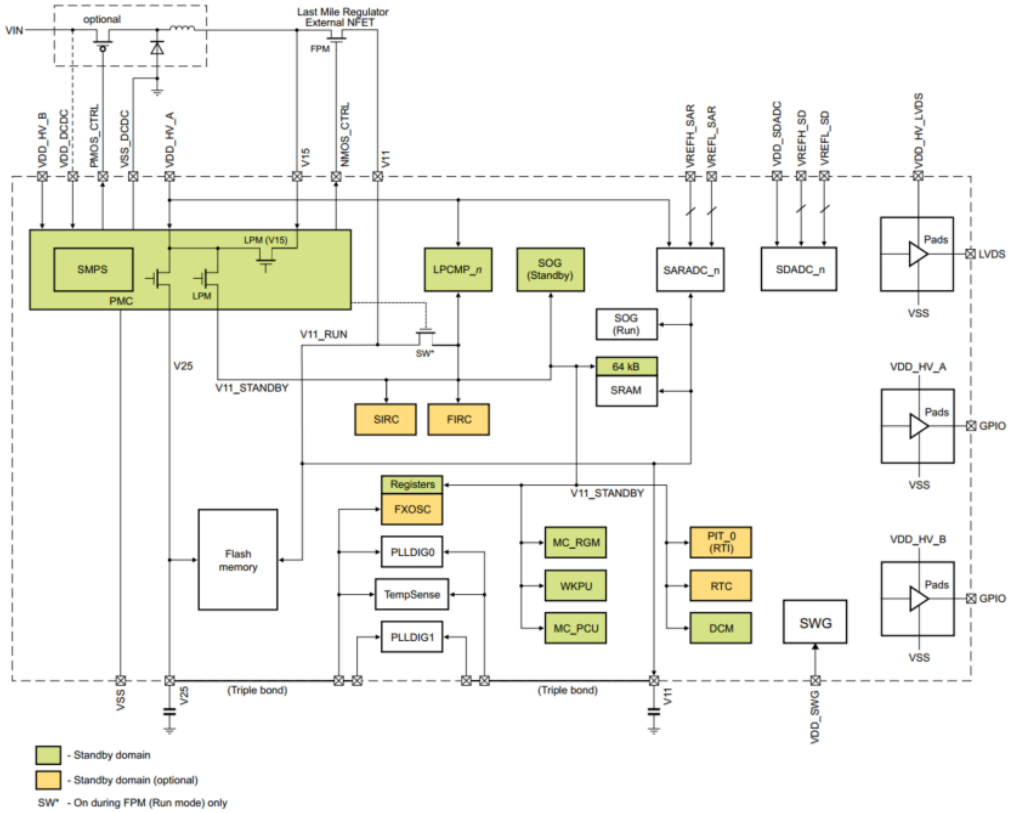


Figure 5. S32K396 Power management system block diagram

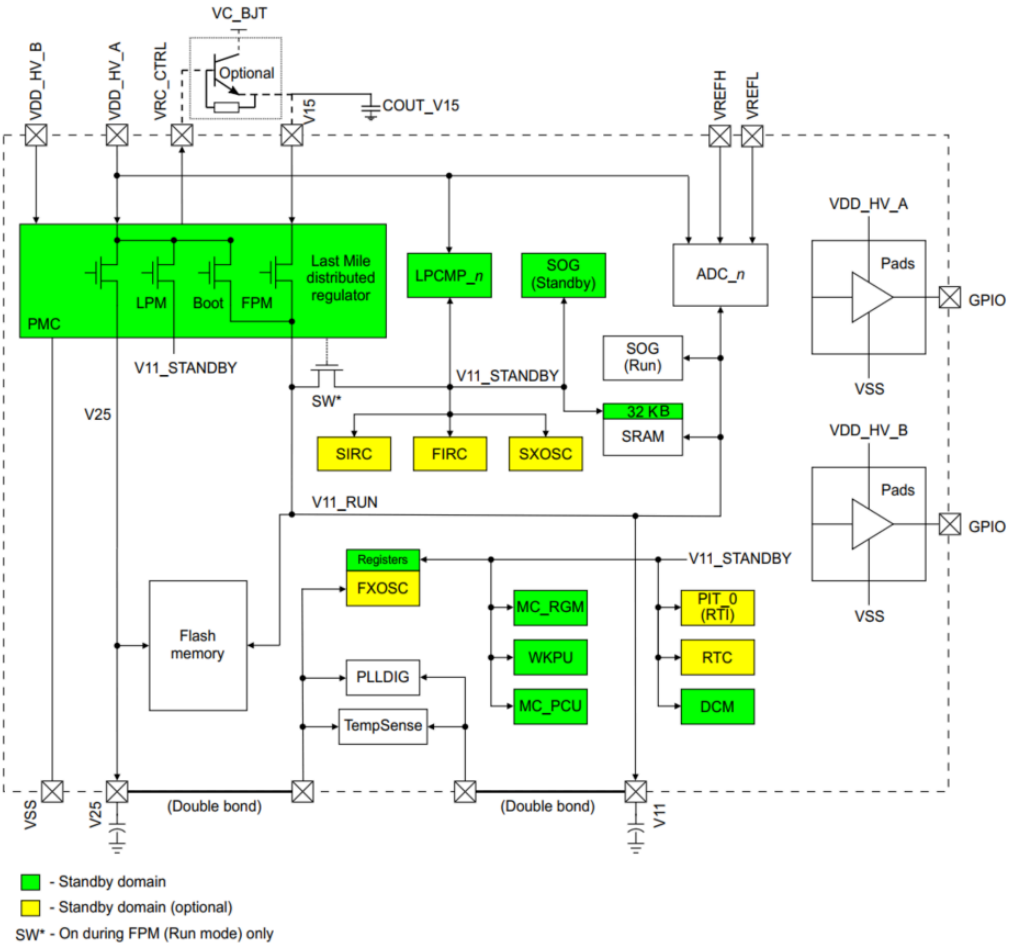


Figure 6. S32K344 Power management system block diagram

5.6 Safety

Table 7 shows the differences between the safety module for S32K344 and S32K396. In addition to the different number of channels, the content of some channels has also changed. See the S32K396 reference manual for more information.

Table 7. Safety module differences

Feature	S32K344	S32K396
EIM channel number	31	19
ERM channel number	31	19
FCCU NCF channel number	8	15

5.7 Real-time control

5.7.1 eFlexPWM

The S32K396 devices support eFlexPWM with 2 instances. eFlexPWM uses the digital Nano-edge module to provide high-resolution PWM outputs. There is no eFlexPWM on the S32K344.

5.7.2 SAR ADC

Table 8 shows the differences of SAR ADC for S32K344 and S32K396.

Table 8. SARADC differences

Feature	S32K344			S32K396						
Instance	ADC_0	ADC_1	ADC_2	ADC_0	ADC_1	ADC_2	ADC_3	ADC_4	ADC_5	ADC_6
Resolution	15 bits	15 bits	15 bits	15 bits	15 bits	15 bits	15 bits	15 bits	15 bits	15 bits
Number of precision channels	8	8	8	8	8	8	8	8	8	8
Number of standard channels	16	16	16	16	16	16	4	4	4	4
Number of external channels	32	32	0	32	32	0	0	0	0	0
DMA support included	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Number of watchdogs	4	4	4	4	4	4	4	4	4	4

5.7.3 SDADC

The S32K396 devices support SDADC with 4 instances. It can be triggered by different motor control IP. There is no SDADC on the S32K344.

5.7.4 ADCBIST

The S32K396 devices support ADCBIST. It can create a sine wave for SDADC test measures. There is no ADCBIST on the S32K344.

5.7.5 LPCMP

Table 9 shows the differences of LPCMP for S32K344 and S32K396.

Table 9. LPCMP differences

Feature	S32K344	S32K396
Instances	3	2

5.7.6 eMIOS

Table 10 shows the differences of eMIOS for S32K344 and S32K396.

Table 10. eMIOS differences

Feature	S32K344	S32K396
Instances	3 (3 x 24 channels)	1 (1 x 24 channels)
Channel types	X, Y, G, H	Z

Compared to S32K344 only 1 instance of eMIOS is implemented on S32K396. The difference is also in the channel types, on S32K396 all the channels (type Z) support the same set of features. For more details of the features supported by, the eMIOS channels see the S32K396 reference manual. Below are the eMIOS channel type diagrams for S32K344 and S32K396.

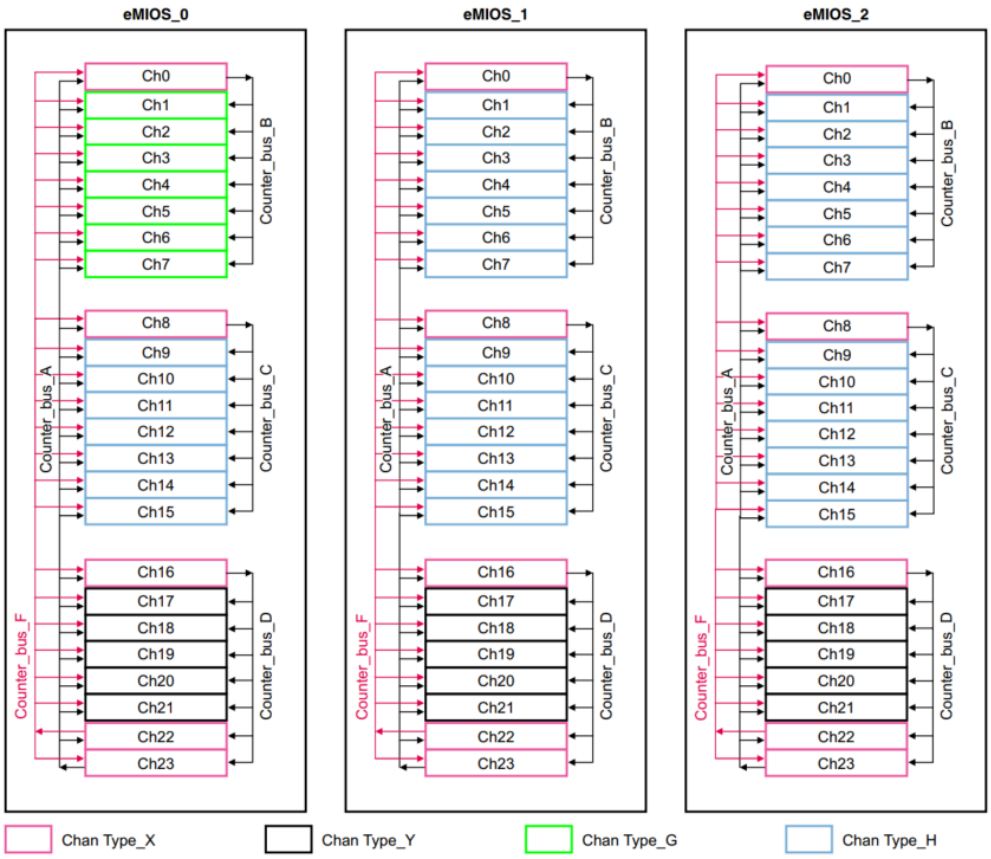


Figure 7. eMIOS channel layout on S32K34

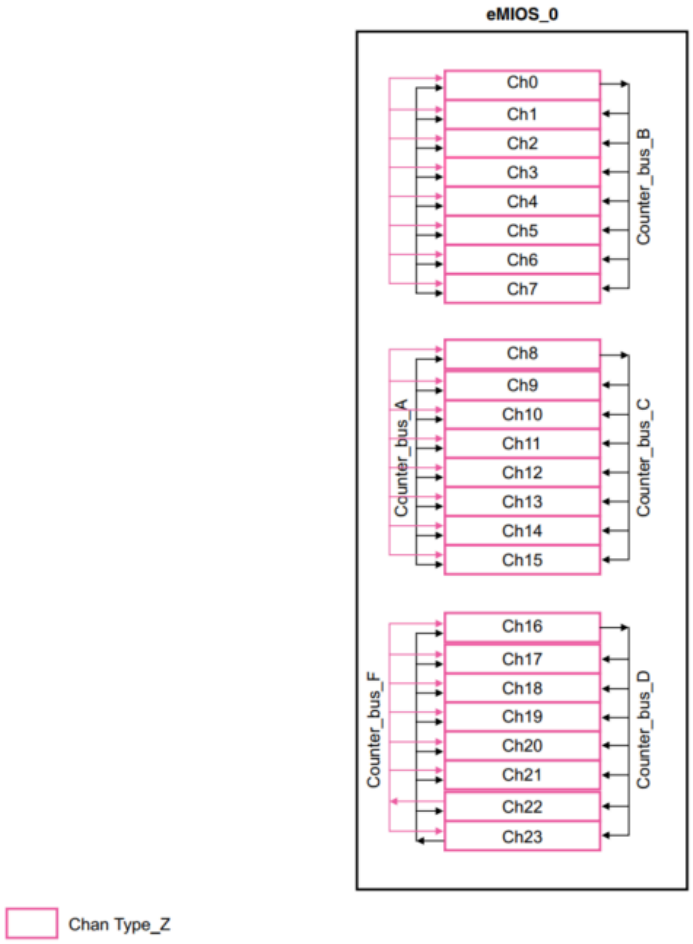


Figure 8. eMIOS channel layout on S32K396

5.7.7 BCTU

There is one more BCTU instance implemented on S32K396 as compared to S32K344 to support an additional four SAR ADC. Table 11 shows the differences of BCTU implementation on S32K344 and S32K396.

Table 11. BCTU differences

BCTU instance	Feature	S32K344	S32K396
BCTU_0	Number of ADCs	3 (ADC0, ADC1, and ADC2)	3 (ADC0, ADC1, and ADC2)
	Number of data FIFO	2	3
	Data FIFO depth	16 (FIFO1) 8 (FIFO2) -	16 (FIFO1) 8 (FIFO2) 8 (FIFO3)
BCTU_1	Number of ADCs	-	4 (ADC3, ADC4, ADC5, and ADC6)
	Number of data FIFO	-	3

Table 11. BCTU differences*...continued*

BCTU instance	Feature	S32K344	S32K396
	Data FIFO depth	-	16 (FIFO1) 8 (FIFO2) 8 (FIFO3)

5.7.8 TRGMUX

There is one additional TRGMUX_MSC added to support the MSC interface and eTPU channels on S32K396.

5.7.9 CoolFlux DSP

S32K396 supports one instance of CoolFlux DSP with four thread hardware multithreading. There is no CoolFlux DSP on S32K344. It is intended to postprocess raw data from the SDADCs and provide the final samples according to the configured sampling rate. Each thread is to process data from one instance of SDADC.

If SDADCs are not used in the application, CoolFlux DSP could be used to perform other operations.

5.7.10 eTPU

S32K396 supports two Enhanced Time Processing Units (eTPU) with a total of 64 channels. The main frequency reaches 320 MHz. There is no eTPU on S32k344.

5.7.11 SGEN

The S32K396 devices support Sine Wave Generator (SGEN) modules with two instances. The SGEN generates a high-quality sinusoidal voltage signal. It can be programmed with the desired oscillation frequency and amplitude voltage.

5.8 Communication

5.8.1 FlexCAN

The FlexCAN module on S32K396 is similar to the one on S32K344. The configuration for this module is the same as that on S32K344. Only a few differences between them must be known, which have been given in the following tables.

Table 12 shows the differences of the FlexCAN module between S32K396 and S32K344.

Table 12. Differences of FlexCAN between S32K396 and S32K344

Feature instances	S32K344						S32K396					
	CAN0*	CAN1	CAN2	CAN3	CAN4	CAN5	CAN0	CAN1	CAN2	CAN3	CAN4	CAN5
Number of message buffers	96	64	64	32	32	32	96	96	96	64	64	64
Enhanced RX FIFO	YES	NO	NO	NO	NO	NO	YES	YES	YES	NO	NO	NO

*For instance FlexCAN0.

Table 13 shows the differences of error injection address mapping between S32K396 and S34K344.

Table 13. Difference of Error injection address mapping between S32K396 and S32K344

RAM content	Memory map	Injection address				
		FlexCAN0	FlexCAN1/2	FlexCAN3/4/5	FlexCAN0/1/2	FlexCAN3/4/5
		S32K344			S32K396	
FlexCAN Registers	——	Not mapped			Not mapped	
MB/s	0080h	0000h	0000h	0000h	0000h	0000h
RXIMRs	0880h	600h	400h	200h	600h	400h
RXIMR_0	0A80h	780h	500h	280h	780h	500h
RXIMR_1	0A84h	784h	504h	284h	784h	504h
RXIMR_2	0A88h	788h	508h	288h	788h	508h
RXIMR_3	0A8Ch	78Ch	50Ch	28Ch	78Ch	50Ch
RXIMR_4	0A90h	790h	510h	290h	790h	510h
RXIMR_5	0A94h	794h	514h	294h	794h	514h
Reserved	0A98h					
RXMGMASK	0AA0h	7A0h	520h	2A0h	7A0h	520h
RXFGMASK	0AA4h	7A4h	524h	2A4h	7A4h	524h
RX14MASK	0AA8h	7A8h	528h	2A8h	7A8h	528h
RX15MASK	0AACh	7ACh	52Ch	2ACh	7ACh	52Ch
TX_SMB0	0AB0h/0F28h	7B0h	530h	2B0h	7B0h	530h
RX_SMB0	0AC0h/0F70h	7C0h/7F8h	540h/578h	2C0h/2F8h	7C0h/7F8h	540h/578h
RX_SMB1	0AD0h/0FB0h	7D0h/840	550h/5C0h	2D0h/340h	7D0h/840	550h/5C0h
RX_SMB0_TIME_STAMP	0C20h	888h	608h	388h	888h	608h
RX_SMB1_TIME_STAMP	0C24h	88Ch	60Ch	38Ch	88Ch	60Ch
HR_TIME_STAMP	0C30h	890h	610h	390h	890h	610h
Enhanced RX FIFO	2000h	A10h	——	——	A10h	——
ERFFEL	3000h	1050h	——	——	1050h	——

All FlexCAN memory must be initialized before operation. Some of these locations are different between S32K396 and S32K344, which is shown in the following table.

Table 14. Differences of the offset address range to be initialized

Chip / Instances	S32K344		S32K396	
	FlexCAN0	FlexCAN1/2/3/4/5	FlexCAN0/1/2	FlexCAN3/4/5
Offset address ranges	080h–ADFh; C20h–31FFh	080h–ADFh; C20h–FFFh	080h–ADFh; C20h–31FFh	080h–ADFh; C20h–FFFh

5.8.2 Zipwire

Serial Inter-Processor Interface (SIPI) and LVDS Fast Asynchronous Serial Transmission Interface (LFAST) modules work together as a single unit called Zipwire. There is no Zipwire implemented on S32K344.

5.8.3 LPUART

Four instances of LPUART are implemented on S32K396 as compared to sixteen instances implemented on S32K344. The configuration of all the LPUART modules on the S32K396 modules is the same as LPUART_0 to LPUART_3 on S32K344. In addition, there are LPUART_4 to LPUART_15 modules on S32K344.

Apart from standard LPUART units there is one additional LPUART_MSC that supports only receiving of the data, and not the transmitting. This module works with the MSC channel communication interface as its upstream part.

5.8.4 SAI

There is no SAI implemented on S32k396.

5.8.5 QSPI flash interface

QuadSPI on S32K396 is similar to the module on S32K344, which added some new features including up to eight bidirectional data lines, support for Hyper-RAM, and secure flash protection.

The configuration for QuadSPI on S32K344 can be used for the IP on S32K396.

Note: *The secure flash protection must be configured properly, which can cause an error when accessing the flash.*

Table 15. Differences in QuadSPI between S32K396 and S32K344

Feature	S32K344	S32K396
Data lines	4	Up to 8
SDR support	YES	YES
DDR support	NO	YES
AHB access	Read	Read
AIPS access	Read/write	Read/write
AHB buffer	256 B	1024 B
RX/TX FIFO	128 B	128 B
LUT SIZE	4	16
Hyper-RAM support	NO	YES
Data learning support	NO	YES
Security flash protection	NO	YES

5.8.6 MSC

S32K396 supports a microsecond channel interface (MSC), which is a serial interface designed to provide I/O expansion by reducing the number of MCU pins required to drive output signals. MSC is composed of DSPI and LPUART_MSC modules. There is no MSC implemented on S32K344.

5.9 Debug

Additional HSE (MTB) interface is supported in S32K396.

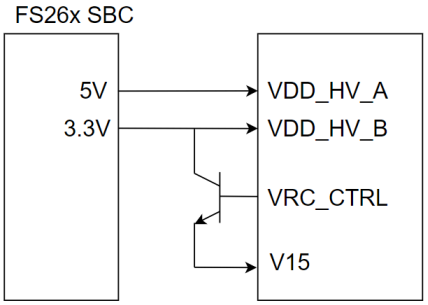
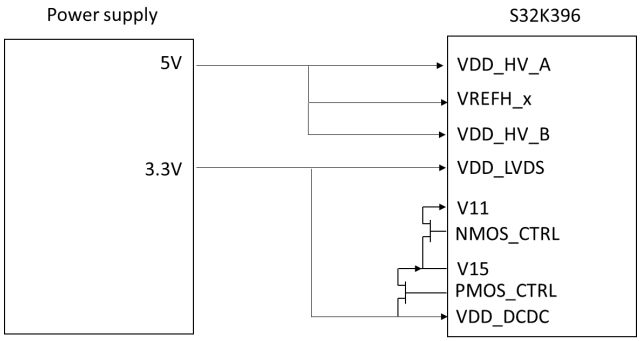
6 Hardware migration

6.1 Power requirement

S32K396 has two main and flexible power domains VDD_HV_A and VDD_HV_B that must be supplied externally. VDD_HV_A is the main I/O and primary supply for analog modules. VDD_HV_B is secondary I/O. Those are the same as on S32K344. The third domain is V15 in which the on-chip SMPS or an external source generates 1.5 V input. The PMC module of the MCU uses this pin to measure the voltage level of V15. V11 is the domain to supply core and internal logic with 1.1 V. It is driven by an external NFET, which is controlled by a linear regulator inside the PMC.

Apart from that there are additional supply sources to power sigma-delta ADCs, Sine wave generators, and LVDS drivers for Zipwire communication.

Table 16. Power domains differences

Feature	S32K344	S32K396
V15 generated internally		

Note: *In the case of 1.5 V generated by on chip SMPS one external ballast generates V15 supply on S32K344. In the case of S32K396 two external transistors are needed: One PMOS for the DCDC block that generates V15 and one NMOS to generate V11. NMOS is mandatory for S32K396 to generate V11 compared to S32K344 where this supply domain does not require external NMOS.*

6.2 FS26 handshake

If FS26 PMIC provides power supply for S32K396 and Standby mode entry is required for both S32K396 and FS26 certain requirements on hardware connection between MCU and PMIC were added to support Standby mode exit:

- EXTWAKE output of S32K396 (available on PTA8, PTA25, or PTE21) must be routed to WAKE1 of FS26 (pin 47) and that must be configured to detect rising edge on the PMIC side.
- RESET_b from S32K396 (PTA5) must be routed to WAKE2 of FS26 (pin 2) and that must be configured to detect the falling edge on the PMIC side.
- RESET_b from S32K396 must be also routed to RSTB of FS26 (pin 16).
- PGOOD input of S32K396 (available on PTA9, PTA20, or PTA26) must be routed to GPIO2 of FS26 (pin 6).
- SPI connection is requested between S32K396 and FS26 for Standby mode entry request.

Figure 9 illustrates the required connections between S32K396 and FS26 for low-power handshake. LDO1 and LDO2 outputs of FS26 are required to be ON during Standby mode. Not all the connections of the power domains are illustrated for the simplification here.

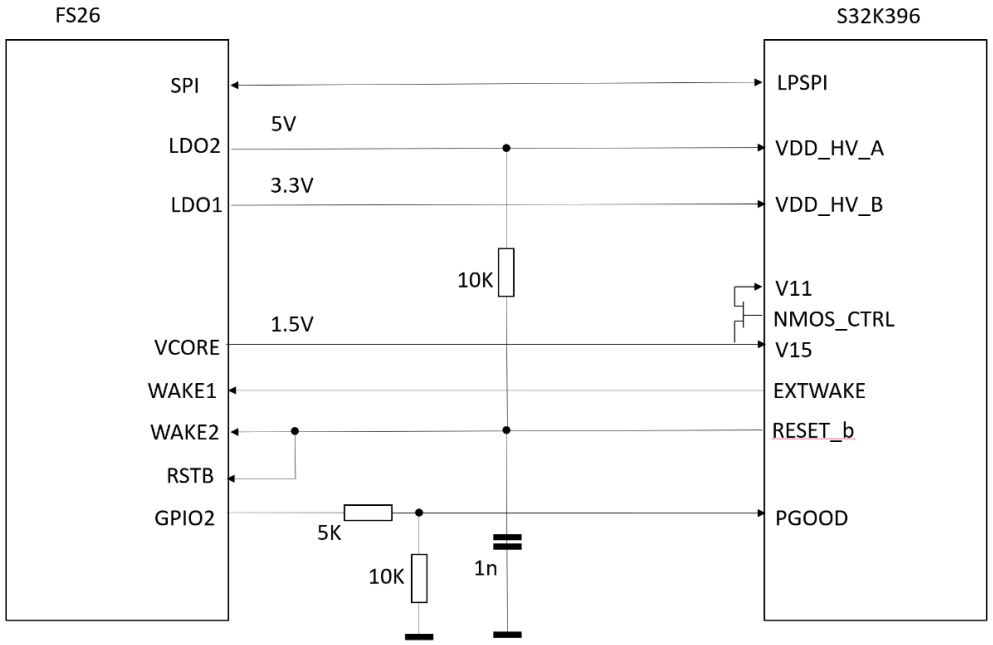


Figure 9. S32K396 and FS26 low-power handshake connections

6.3 Pin support

The pinout is compatible between S32K369 and S32K344, however, there are important changes that must be considered. In total, 66-pin locations have different functions between S32K344 and S32K396.

- 32 balls are new pins that are not present on S32K344 (forming a ring at the center of the package).
- 18 other pins see their functionality change from S32K344 to S32K39x. These pins concern the inclusion of zip wire, sinewave generator, and microsecond bus modules that have dedicated pins on the device.
- 16 pins are now dedicated to ADC channels.

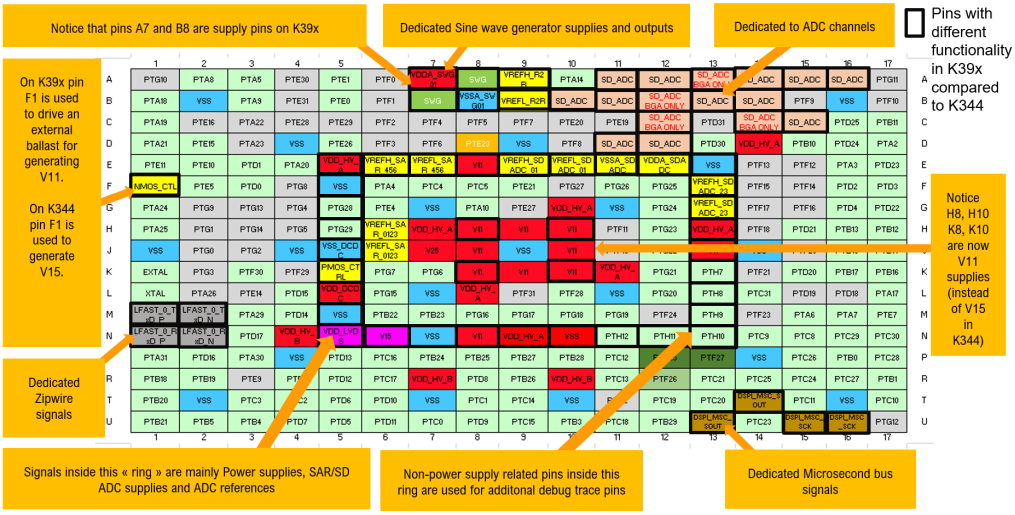


Figure 10. Comparison of PIN distribution between K344 and K396

Zipwire, SWG, ADC channels, and microsecond functionalities are implemented as dedicated functions on the pin. There are no other functions on these pins other than these. On a pin that has GPIO capabilities, the goal is to keep the same muxed functions in S32K396 as in S32K344. In average, the number of functions multiplexed on one pin is bigger in S32K396 vs S32K344 to compensate for the use of dedicated pins.

7 Software migration

7.1 Summary

The primary application cores on the S32K396 devices differ from the cores on S32K344 in data cache sizes and split-lock capability and these differences may affect software functionality and performance when porting. Interrupts use a similar routing approach but the interrupt details and table are different between the S32K396 and the S32K344 devices. Except for the newly added peripherals, the addresses of other peripherals are almost the same. For the memory map the start address for the blocks that are kept are the same, the end address is different. So, the SW developed on S32K344 can be ported with not so much effort to S32K396.

7.2 Cortex-M7 code

Code, in general, can be compiled and run on the Cortex-M7 cores without modification. Consider the following guidelines when porting code. The Data cache on the S32K344 devices is half the size of the 16 kB on the S32K396.

7.3 Interrupt routing

The general operation of the interrupts on the S32K396 family is the same as on the S32K344. The sources of interrupts that are common for both devices have the same numbering. Newly added sources replace those which are no longer present in S32K344 (like SAI, eMIOS1-2, LPUART_5-15) and fills the reserved spaces. For details see *S32K39_and_S32K37_interrupt_map.xlsx* attached to the S32K396 reference manual.

7.4 Peripheral use

There is a high degree of compatibility between peripherals in the two families but the placement in memory is different as is the routing of interrupts and DMA triggers. There are more copies of the peripherals on the S32K396 as compared to the S32K344 and the features of each is higher than that on the S32K344.

8 Revision history

Revision history

Document ID	Release date	Description
AN14301 v.1.0	25 March 2025	Initial release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: https://www.nxp.com

Date of release: 25 March 2025
Document identifier: AN14301