AN14202

Migration guide from KE15Z256 to KE17Z512

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Document information

Information	Content
Keywords	AN14202, Kinetis E series, KE17Z512, KE15Z256, migration guide, flash memory controller (FMC), Touch Sensing Input (TSI), pin assignments
Abstract	This application note provides a feature comparison between the KE17Z512 and KE15Z256 device families. It includes pin assignments and the steps for migration between the two platforms.

1 Introduction

KE17Z512 is a new product of the NXP Kinetis E series after KE18F, KE15Z, KE16Z, and KE17Z. It is similar to the KE15Z but has an upgraded TSI function that helps to realize complex touch solutions. This application note compares the differences between KE17Z512 and the KE15Z256 device family of MCUs. It can be used as a migration guide between the two platforms.

Table 1 shows the parts of KE15Z/14Z with up to 256 KB Flash.

Table 1. Parts of KE15Z/14Z with up to 256 KB flash

Part number	Frequency (MHz)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	TSI channels (TSI0)	GPIOs	ADC channels	Package (LQFP)
MKE15Z256VLL7	72	256	32	32/2	25	89	ADC0(16) ADC1(12)	100
MKE15Z128VLL7	72	128	16	32/2	25	89	ADC0(16) ADC1(12)	100
MKE14Z256VLL7	72	256	32	32/2	–	89	ADC0(16) ADC1(12)	100
MKE14Z128VLL7	72	128	16	32/2	–	89	ADC0(16) ADC1(12)	100
MKE15Z256VLH7	72	256	32	32/3	25	58	ADC0(16) ADC1(11)	64
MKE15Z128VLH7	72	128	16	32/4	25	58	ADC0(16) ADC1(11)	64
MKE14Z256VLH7	72	256	32	32/5	–	58	ADC0(16) ADC1(11)	64
MKE14Z128VLH7	72	128	16	32/6	–	58	ADC0(16) ADC1(11)	64

The KE17Z512 series currently has six parts, as shown in Table 2.

Table 2. Parts of KE17Z512 series with up to 512 KB flash

Part number	Frequency (MHz)	Flash (KB)	SRAM (KB)	TSI channels	GPIOs	ADC0 channels	Package (LQFP)
MKE17Z512VLL9	96	512	96	TSI0(25) TSI1(25)	89	24	100
MKE13Z512VLL9	96	512	96	TSI0(25)	89	24	100
MKE12Z512VLL9	96	512	96	_	89	24	100
MKE17Z512VLH9	96	512	96	TSI0(22) TSI1(25)	58	24	64
MKE13Z512VLH9	96	512	96	TSI0(22)	58	24	64
MKE12Z512VLH9	96	512	96	_	58	24	64

1.1 Feature comparison

Table 3 lists the comparison of KE15Z256 and KE17Z512 in terms of system resources.

Table 3. Comparison of system resources between KE15Z256 and KE17Z512

Component	KE15Z256	KE17Z512
Core	72 MHz, Arm Cortex-M0+	96 MHz, Arm Cortex-M0+
Flash	256 KB	512 KB (dual bank, swap feature)
RAM	32 KB	96 KB
EEPROM/ FlexMemory	2 KB/32 kB	-
Boot ROM	Yes	-
eDMA	8 channel	8 channel
HW Acceleration	MMDVSQ+BME	-
Clock System	IRC48M (±1%) + IRC8M (±3%) + LPFLL + LPO + OSC32K + OSC4-40M	IRC48M (±1%) + IRC8M (±3%) + LPFLL + LPO + OSC4-40M
ADC	2x 12-bit ADC, 1MSPS	1x 12-bit ADC, 1MSPS
CMP/DAC buffer	2/1	1/0
FlexTimers	1x 8-ch + 2x 4-ch FTM	1x 8-ch + 2x 4-ch FTM
		Removed deadtime and quadrature decode
General Timers	4-ch 32-bit LPIT + 16-bit LPTMR + PDB	4-ch 32-bit LPIT + 16-bit LPTMR
PWT	1	1
RTC	1	1
WDOG	1	1
UART/SPI/ I2C	3 x LPUART / 2 x LPSPI / 2x LPI2C	3 x LPUART + 2 x SCI / 2 x LPSPI / 2x LPI2C
FlexIO	Yes (4 timers + 4 shifters)	Yes (4 timers + 4 shifters)
TSI	1 x 25 ch (Each TSI has 1 shield channel)	2 x 25ch (Each TSI channel can be configured as shield channel)
Package	100LQFP, 64LQFP	100LQFP, 64LQFP

The following sections compare the differences between KE15Z256 and KE17Z512 MCUs in terms of memory, clock, and peripherals.

2 Block diagram

Figure 1 shows the system block diagram of KE15Z256.

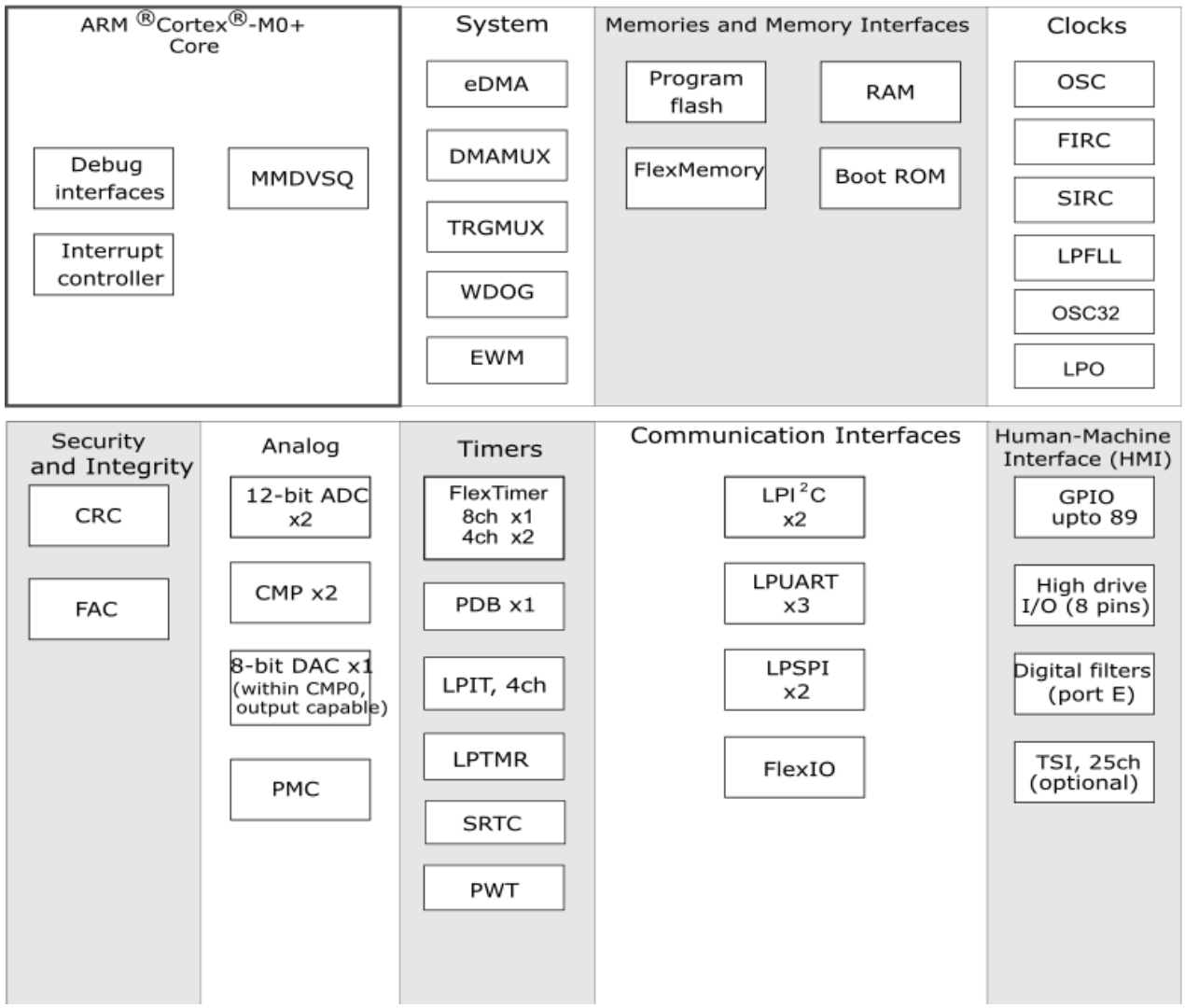

Figure 1. KE15Z256 system block diagram

Figure 2 shows the system block diagram of KE17Z512.

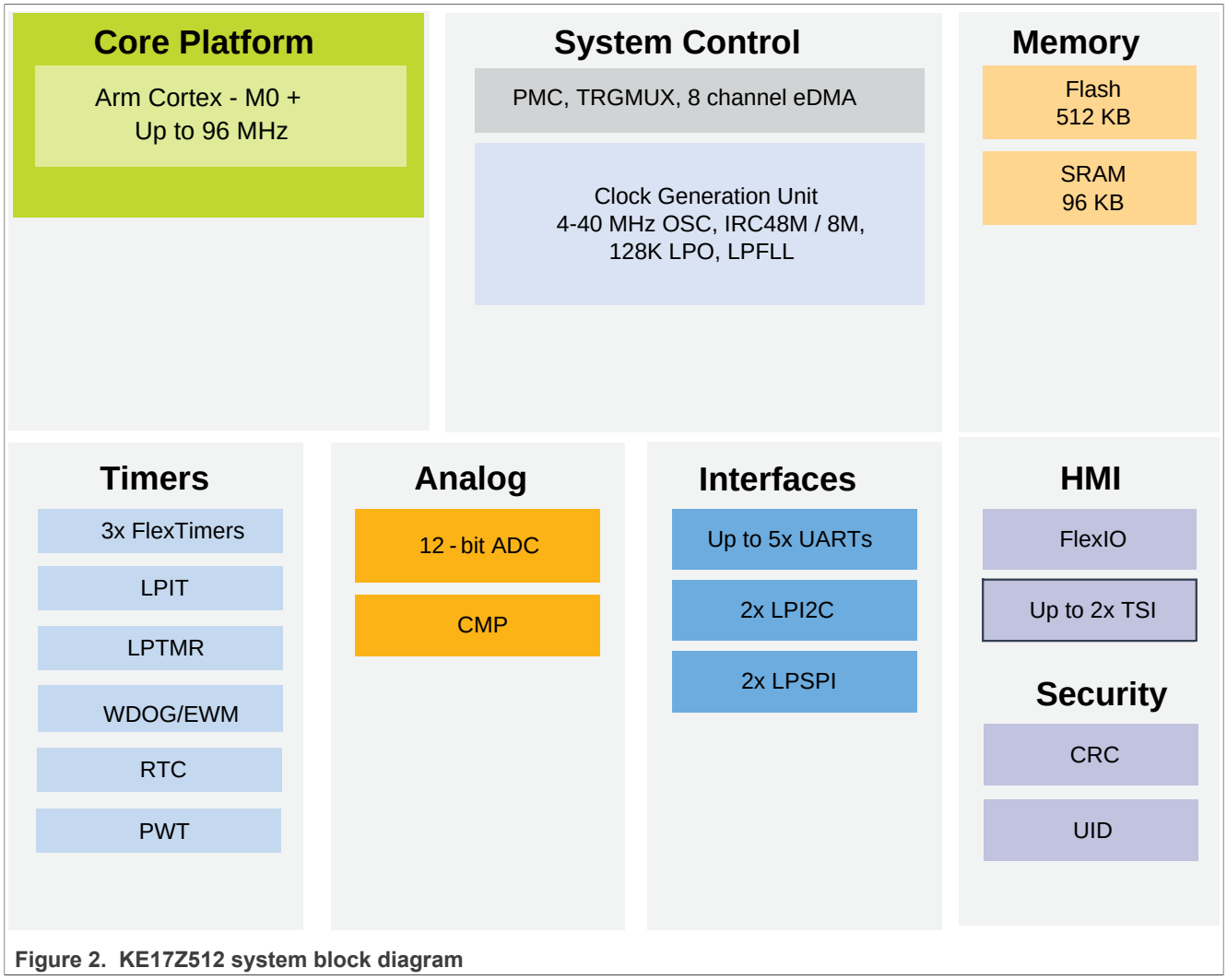

Figure 2. KE17Z512 system block diagram

3 Memory

3.1 Flash memory

KE17Z512 has a 512 KB dual bank flash with swap feature, and there is no ROM in this device. The swap feature enables the lower half of the program flash space to be operational while the upper half is being updated for future use.

KE17Z512 has the flash memory controller (FMC) function. The FMC is the interface between the flash memory blocks and the system. In a typical configuration, the core and system bus clock speeds are faster than the flash memory clock. The FMC cache and prefetch speculation buffer allow the FMC to respond to flash accesses with no added wait states often. Anytime the requested information is available in the cache or prefetch buffer, the FMC responds with no added wait state.

KE15Z256 has 256 KB flash, 32 KB FlexNVM and 2 KB FlexRAM. FlexRAM can be used as traditional RAM or as high endurance EEPROM storage.

KE15Z256 has a flash access control (FAC) function. FAC is a configurable memory protection scheme designed to allow end users to use software libraries while offering programmable restrictions to these libraries. This allows NXP or third-party vendors to pre-program software libraries into a chip and distribute parts to end customers who can use the preprogrammed software libraries.

3.2 SRAM memory

The SRAM size of KE15Z256 is 32 KB and the SRAM size of KE17Z512 is 96 KB. The memory comparison of KE15Z256 and KE17Z512 is shown in Table 4.

Table 4. KE15Z256 and KE17Z512 memory comparison

Memory	KE15Z256 series		KE17Z512 series
	MKE1xZ256VLL7	MKE1xZ128VLL7	MKE1xZ512 (x =7/3/2)
	MKE1xZ256VLH7 (x =5/4)	MKE1xZ128VLH7 (x =5/4)	
Flash	256 KB: (0x0000_0000–0x0003_FFFF)	128 KB: (0x0000_0000–0x0001_FFFF)	**512 KB, dual bank:** (0x0000_0000–0x0007_FFFF)
FlexNVM	32 KB: (0x1000_0000–0x1000_7FFF)	32 KB: (0x1000_0000–0x1000_7FFF)	———
FlexRAM	2 KB: (0x1400_0000–0x1400_07FF)	2 KB: (0x1400_0000–0x1400_07FF)	———
SRAM	32 KB: (0x1FFF_E000-0x2000_5FFF)	16 KB: (0x1FFF_F000-0x2000_2FFF)	**96 KB:** (0x1FFF_8000-0x2000_FFFF)
	SRAM_L, 8 KB: 0x1FFF_E000-0x1FFF_FFFF) SRAM_U, 24 KB: (0x2000_0000-0x2000_5FFF)	SRAM_L, 4 KB: (0x1FFF_F000-0x1FFF_FFFF) SRAM_U, 12 KB: (0x2000_0000-0x2000_2FFF)	SRAM_L, 32 KB: (0x1FFF_8000-0x1FFF_FFFF) SRAM_U, 64 KB: (0x2000_0000-0x2000_FFFF)
Boot ROM	16 KB: (0x1C00_0000-0x1C00_3FFF)	16 KB: (0x1C00_0000-0x1C00_3FFF)	———

4 Clock distribution

Figure 3 and Figure 4 show the clock distribution diagrams of KE15Z256 and KE17Z512 respectively.

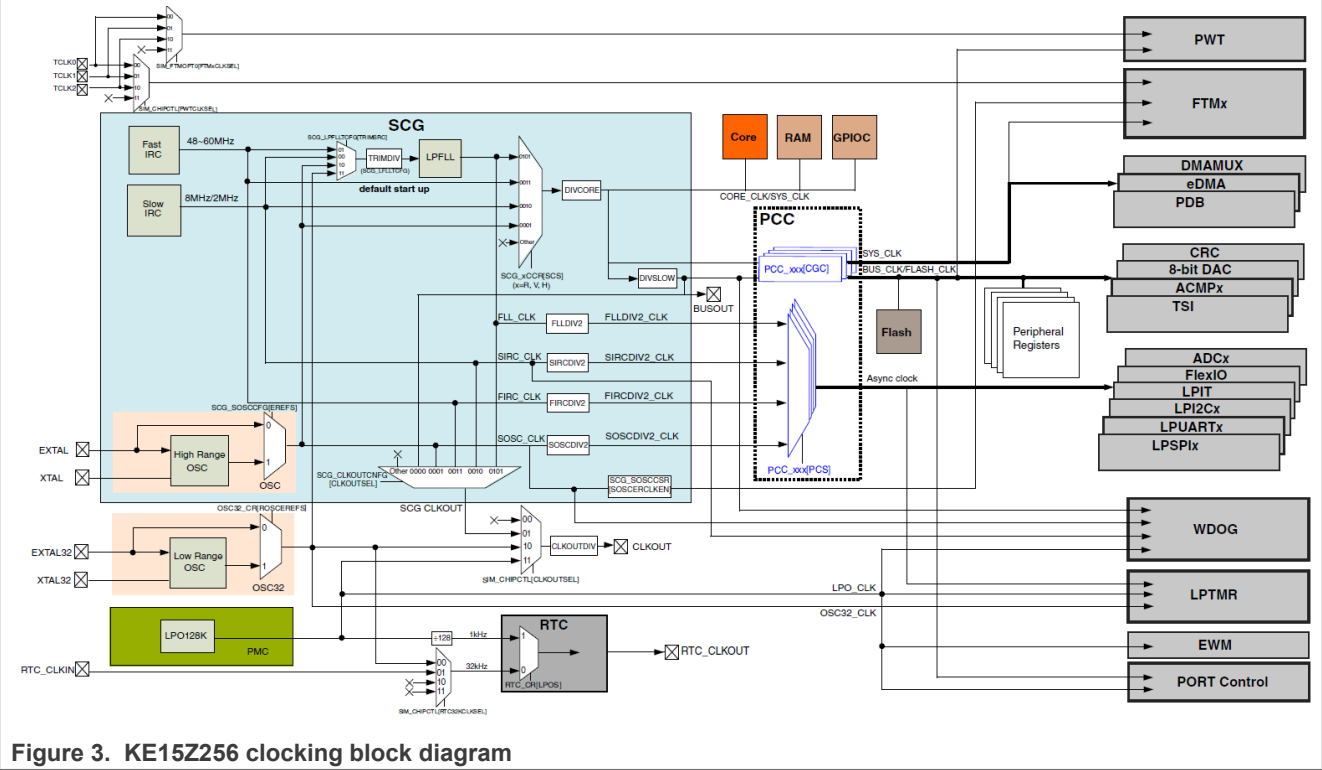

Figure 3. KE15Z256 clocking block diagram

Compared with the KE15Z256 clock system, there is no OSC32 module on KE17Z512. Therefore, LPTMR and RTC cannot choose OSC32_CLK as the clock source. For KE17Z512 RTC module, the external crystal oscillator clock SOSC_CLK can be selected as a clock source.

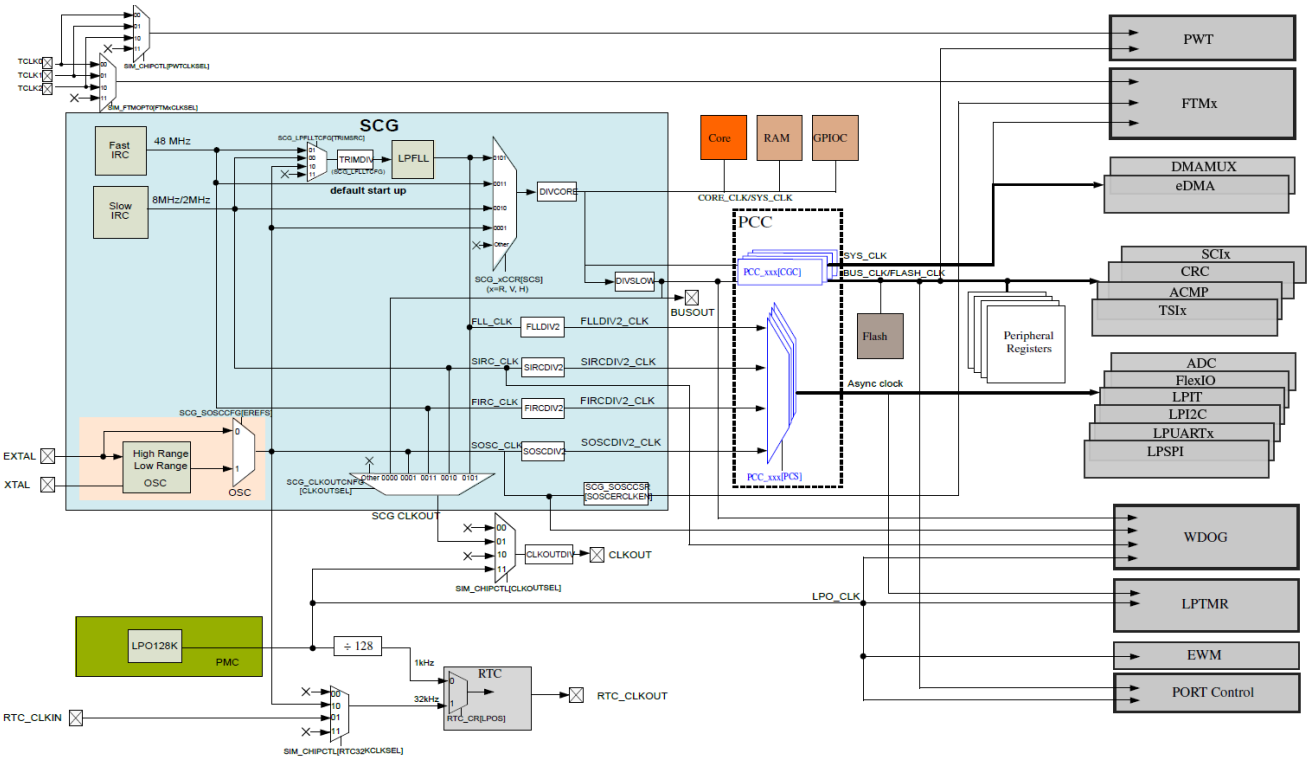

Figure 4. KE17Z512 clocking block diagram

5 Pinouts

The pin assignments for KE17Z512 in 100LQFP and 64LQFP packages are compatible with KE15Z256.

Note: *The number and position of GPIO pins in both device packages are the same, as shown in Figure 5. However, the pin multiplexing function on some GPIO ports is different.*

Refer to the Peripheral for the pin assignment of each peripheral.

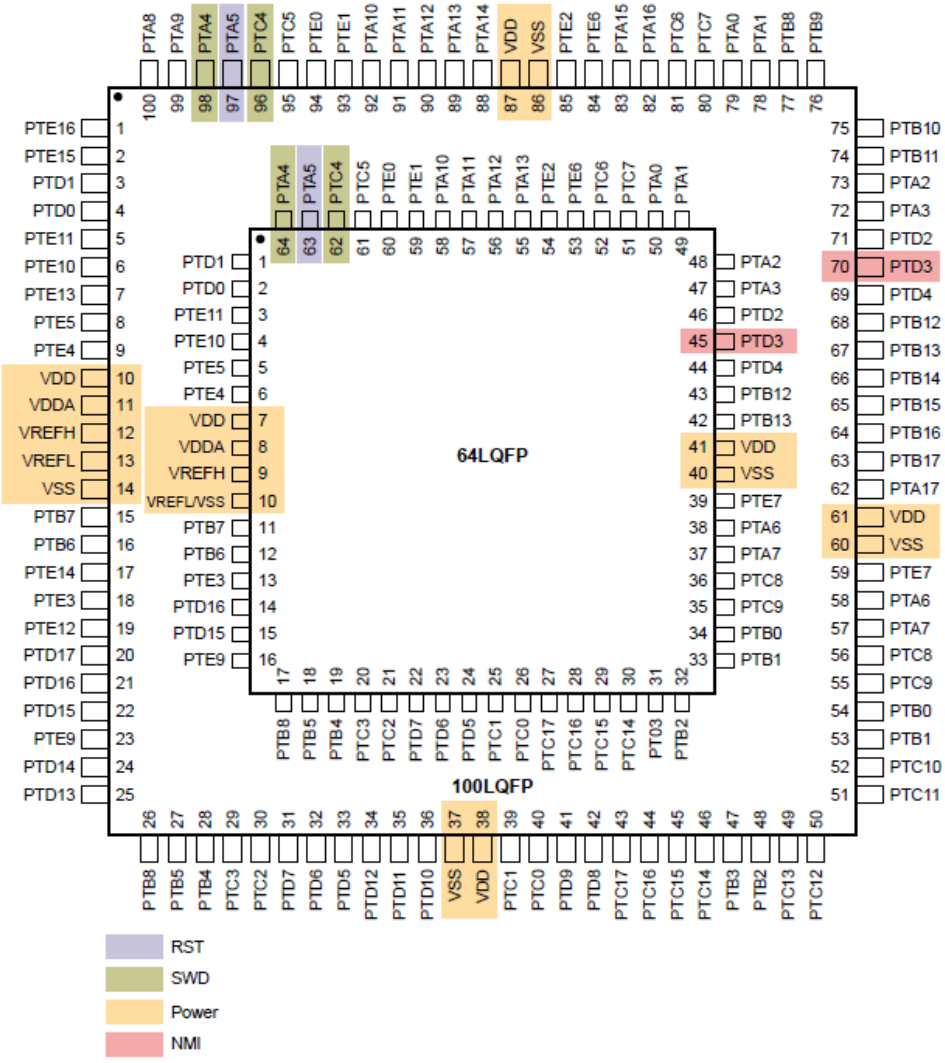

Figure 5. KE17Z512 and KE15Z256 pinouts in 100LQFP and 64LQFP packages

6 Peripherals

This section compares the differences between KE15Z256 and KE17Z512 in terms of peripherals.

6.1 Touch Sensing Input (TSI)

6.1.1 Pin assignments for KE17Z512 and KE15Z256 parts

KE17Z512 has two TSI modules. Each module has 25 TSI channels, a total of 50 TSI channels. In TSI self-cap mode of each TSI module, any one or a group of them can be configured as the shield electrode. The more shield channels are used, the bigger is the shield driver strength. In all the 25 channels of each TSI module, channel 4, channel 12, channel 21, and channel 24 are designed stronger. If fewer shield pins are needed, these channels mentioned above are recommended to be used.

KE15Z256 has only one TSI module, a total of 25 TSI channels, and only one shield channel. For the TSI0 module, the TSI channel assignment of KE17Z512 and KE15Z256 is also very different. Table 5 shows the pin assignments of the KE15Z TSI module.

Note: *In the Table 5 and Table 6 below, the pins marked with an asterisk symbol (*) can be used as TSI channels in both KE15Z256 and KE17Z512, but the mapped channel numbers are different.*

Table 5. Pin assignments of the KE15Z256 TSI module

KE15Z (100LQFP)	KE15Z (64LQFP)	Pin name	ALT0	HD pins
3	1	PTD1*	TSI0_CH5*	HD pin*
4	2	PTD0*	TSI0_CH4*	HD pin*
5	3	PTE11*	TSI0_CH3*	
6	4	PTE10*	TSI0_CH2*	
8	5	PTE5*	TSI0_CH0*	
9	6	PTE4*	TSI0_CH1*	
18	13	PTE3*	TSI0_CH24*	
26	17	PTE8*	ACMP0_IN3/TSI0_CH11*	
27	18	PTB5*	TSI0_CH9*	HD pin*
28	19	PTB4*	ACMP1_IN2/TSI0_CH8*	HD pin*
31	22	PTD7*	TSI0_CH10*	
32	23	PTD6*	TSI0_CH7*	
33	24	PTD5*	TSI0_CH6*	
39	25	PTC1*	ADC0_SE9/ACMP1_IN3/TSI0_CH23*	
40	26	PTC0*	ADC0_SE8/ACMP1_IN4/TSI0_CH22*	
47	31	PTB3*	ADC0_SE7/TSI0_CH21*	
48	32	PTB2*	ADC0_SE6/TSI0_CH20*	
78	49	PTA1*	ADC0_SE1/ACMP0_IN1/TSI0_CH18*	
79	50	PTA0*	ADC0_SE0/ACMP0_IN0/TSI0_CH17*	
80	51	PTC7*	ADC1_SE5/TSI0_CH16*	
81	52	PTC6*	ADC1_SE4/TSI0_CH15*	

Table 5. Pin assignments of the KE15Z256 TSI module*...continued*

KE15Z (100LQFP)	KE15Z (64LQFP)	Pin name	ALT0	HD pins
85	54	PTE2*	ADC1_SE10/TSI0_CH19*	
93	59	PTE1*	TSI0_CH14*	HD pin*
94	60	PTE0*	TSI0_CH13*	HD pin*
95	61	PTC5*	TSI0_CH12*	

Table 6 shows the pin assignment of the KE17Z512 TSI module.

Table 6. Pin assignments of KE17Z512 TSI module

KE17Z512 (100QFP)	KE17Z512 (64LQFP)	Pin name	ALT0	HD pins
1		PTE16	TSI0_CH13	
2		PTE15	TSI0_CH14	
3	1	PTD1*	TSI0_CH11*	HD pin*
4	2	PTD0*	TSI0_CH12*	HD pin*
5	3	PTE11*	TSI0_CH9*	
6	4	PTE10*	TSI0_CH10*	
7		PTE13	TSI0_CH15	
8	5	PTE5*	TSI0_CH16*	
9	6	PTE4*	TSI0_CH17*	
18	13	PTE3	ADC0_SE6/TSI0_CH18	
21	14	PTD16	ADC0_SE4/TSI0_CH19	HD pin
22	15	PTD15	ADC0_SE2/TSI0_CH20	HD pin
23	16	PTE9	ADC0_SE0/TSI0_CH21	
26	17	PTE8*	ACMP0_IN3/ADC0_SE1/TSI0_CH22*	
27	18	PTB5*	ADC0_SE3/TSI0_CH23*	HD pin*
28	19	PTB4*	ADC0_SE5/TSI0_CH24*	HD pin*
39	25	PTC1*	ADC0_SE8/TSI1_CH24*	
40	26	PTC0*	ADC0_SE10/TSI1_CH23*	
43	27	PTC17	ADC0_SE12/TSI1_CH22	
44	28	PTC16	ADC0_SE14/TSI1_CH21	
45	29	PTC15	TSI1_CH20	
46	30	PTC14	TSI1_CH19	
47	31	PTB3*	TSI1_CH18*	
48	32	PTB2*	TSI1_CH17*	
53	33	PTB1	TSI1_CH16	
54	34	PTB0	TSI1_CH15	
55	35	PTC9	TSI1_CH14	

Table 6. Pin assignments of KE17Z512 TSI module*...continued*

KE17Z512 (100QFP)	KE17Z512 (64LQFP)	Pin name	ALT0	HD pins
56	36	PTC8	TSI1_CH13	
57	37	PTA7	TSI1_CH12	
58	38	PTA6	TSI1_CH11	
59	39	PTE7	TSI1_CH10	
67	42	PTB13	TSI1_CH9	
68	43	PTB12	TSI1_CH8	
69	44	PTD4	TSI1_CH7	
71	46	PTD2	TSI1_CH6	
72	47	PTA3	TSI1_CH5	
73	48	PTA2	TSI1_CH4	
78	49	PTA1*	ACMP0_IN1/TSI1_CH3*	
79	50	PTA0*	ACMP0_IN0/TSI1_CH2*	
80	51	PTC7*	TSI1_CH1*	
81	52	PTC6*	TSI1_CH0*	
84	53	PTE6	TSI0_CH0	
85	54	PTE2	TSI0_CH1*	
89	55	PTA13	TSI0_CH2	
90	56	PTA12	TSI0_CH3	
91	57	PTA11	TSI0_CH4	
92	58	PTA10	TSI0_CH5	
93	59	PTE1	TSI0_CH6	HD pin
94	60	PTE0	TSI0_CH7	HD pin
95	61	PTC5	TSI0_CH8	

6.1.2 TSI model comparison for KE17Z512 and KE15Z256 parts

Table 7 shows the TSI model comparison between KE17Z512 and KE15Z256 parts.

Table 7. TSI model comparison for KE17Z512 and KE15Z256 parts

		KE17Z512 series				KE15Z256/128 series
		KE17Z512 100LQFP	KE17Z612 64LQFP	KE13Z512 100LQFP	KE13Z512 64LQFP	KE15Z 100/64 LQFP
Part Number		MKE17Z512 VLL9	MKE17Z512 VLH9	MKE13Z512 VLL9	MKE13Z512 VLH9	MKE15Z256 VLL7 MKE15 Z128VLL7 MKE15Z256 VLH7 MKE15 Z128VLH7
Frequency		96 MHz	96 MHz	96 MHz	96 MHz	72 MHz
Flash		512 KB	512 KB	512 KB	512 KB	256 KB/128 KB
Total TSI channels	Self-cap mode	50 channels (TSI0:25-ch, TSI1:25-ch)	47 channels (TSI0:22-ch, TSI1:25-ch)	25 channels (TSI0:25-ch)	22 channels (TSI0:22-ch)	25 channels (TSI0:25-ch)
	Mutual-cap mode	24 channels (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	24 channels (TSI0: TX/6-ch, RX/6-ch; TSI1:TX/6-ch, RX/6-ch)	12 channels (TSI0: TX/6-ch, RX/6-ch)	12 channels (TSI0: TX/6-ch, RX/6-ch)	12 channels (TSI0: TX/6-ch, RX/6-ch)
TSI0	Self-cap channel	25 channels (TSI0[0:24])	22 channels (TSI0[0:12], [16:24])	25 channels (TSI0[0:24])	22 channels (TSI0[0:12], [16:24])	25 channels (TSI0[0:24])
	Mutual-cap channel	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]
	Shield channel	Up to 25 shield channels; CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 22 shield channels CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 22 shield channels CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	One shield channel: CH12
	Comment	-	No CH13, CH14, CH15	-	No CH13, CH14, CH15	-
TSI1	Self-cap channel	25-ch TSI0[0:24]	25-ch TSI1[0:24]	Not Supported	Not Supported	Not Supported
	Mutual-cap channel	TX[0:5], RX[6:11]	TX[0:5], RX[6:11]			
	Shield channel	Up to 25 shield channels: CH4, CH12, CH21, CH24 are enhanced TSI channels than others.	Up to 25 shield channels; CH4, CH12, CH21, CH24 are enhanced TSI channels than others.			

6.2 PDB

The Programmable Delay Block (PDB) module is not present in KE17Z512 device (unlike KE15Z).

6.3 ADC

KE15Z256 has two ADC modules, and each module has two data registers. For different packages, the number of external channels supported by each module is also different, as shown in Table 8.

KE17Z512 has only one ADC module ADC0 and four data registers. The ADC0 external channel assignment is also different from KE15Z, which is shown in Table 9.

For the 100LQFP package, the ADC module of KE15Z has 28 single-ended input pins, and KE17Z512 has 24 single-ended input pins.

Note: *In tables Table 8 and Table 9, the pins marked with a * can be used as ADC channels in KE15 and KE17Z512, but the mapped channel numbers are different.*

In addition to the different pin assignments, the ADC trigger source is also different. KE17Z512 does not have a PDB module. Therefore, the ADC does not have a trigger source from the PDB module, and the SIM_ADCOPT[ADCxTRGSEL] bit does not exist.

Table 8. Pin assignment of KE15Z ADC module

KE15Z 100LQFP	KE15Z 64LQFP	Pin Name	ALT0
29	20	PTC3*	ADC0_SE11/ACMP0_IN4/EXTAL32*
30	21	PTC2*	ADC0_SE10/ACMP0_IN5/XTAL32*
39	25	PTC1*	ADC0_SE9/ACMP1_IN3/TSI0_CH23*
40	26	PTC0*	ADC0_SE8/ACMP1_IN4/TSI0_CH22*
43	27	PTC17*	ADC0_SE15*
44	28	PTC16*	ADC0_SE14*
45	29	PTC15*	ADC0_SE13*
46	30	PTC14*	ADC0_SE12*
47	31	PTB3*	ADC0_SE7/TSI0_CH21*
48	32	PTB2*	ADC0_SE6/TSI0_CH20*
53	33	PTB1*	ADC0_SE5*
54	34	PTB0*	ADC0_SE4*
57	37	PTA7	ADC0_SE3/ACMP1_IN1
58	38	PTA6	ADC0_SE2/ACMP1_IN0
66	-	PTB14	ADC1_SE9
67	42	PTB13	ADC1_SE8
68	43	PTB12	ADC1_SE7
69	44	PTD4	ADC1_SE6
70	45	PTD3	ADC1_SE3
71	46	PTD2	ADC1_SE2
72	47	PTA3	ADC1_SE1
73	48	PTA2	ADC1_SE0

Table 8. Pin assignment of KE15Z ADC module*...continued*

78	49	PTA1	ADC0_SE1/ACMP0_IN1/TSI0_CH18
79	50	PTA0	ADC0_SE0/ACMP0_IN0/TSI0_CH17
80	51	PTC7	ADC1_SE5/TSI0_CH16
81	52	PTC6	ADC1_SE4/TSI0_CH15
84	53	PTE6	ADC1_SE11
85	54	PTE2	ADC1_SE10/TSI0_CH19

Table 9. Pin assignment of KE17Z512 ADC module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin Name	ALT0
18	13	PTE3	ADC0_SE6/TSI0_CH18
21	14	PTD16	ADC0_SE4/TSI0_CH19
22	15	PTD15	ADC0_SE2/TSI0_CH20
23	16	PTE9	ADC0_SE0/TSI0_CH21
26	17	PTE8	ACMP0_IN3/ADC0_SE1/TSI0_CH22
27	18	PTB5	ADC0_SE3/TSI0_CH23
28	19	PTB4	ADC0_SE5/TSI0_CH24
29	20	PTC3*	ADC0_SE7/ACMP0_IN4*
30	21	PTC2*	ADC0_SE15/ACMP0_IN5*
31	22	PTD7	ADC0_SE13
32	23	PTD6	ADC0_SE11
33	24	PTD5	ADC0_SE9
39	25	PTC1*	ADC0_SE8/TSI1_CH24*
40	26	PTC0*	ADC0_SE10/TSI1_CH23*
43	27	PTC17*	ADC0_SE12/TSI1_CH22*
44	28	PTC16*	ADC0_SE14/TSI1_CH21*
45	29	PTC15*	ADC0_SE16/TSI1_CH20*
46	30	PTC14*	ADC0_SE17/TSI1_CH19*
47	31	PTB3*	ADC0_SE18/TSI1_CH18*
48	32	PTB2*	ADC0_SE19/TSI1_CH17*
53	33	PTB1*	ADC0_SE20/TSI1_CH16*
54	34	PTB0*	ADC0_SE21/TSI1_CH15*
55	35	PTC9	ADC0_SE22/TSI1_CH14
56	36	PTC8	ADC0_SE24/TSI1_CH13

6.4 CMP

The comparator module is referred to as ACMP in KE15Z and CMP in KE17Z512. KE15Z has two ACMP modules. Each ACMP module supports 6 external analog inputs, and each ACMP module has a built-in 8-bit DAC. ACMP0 also has a DAC buffer, through which the output of DAC0 can be connected to an external pin, as shown in Figure 6.

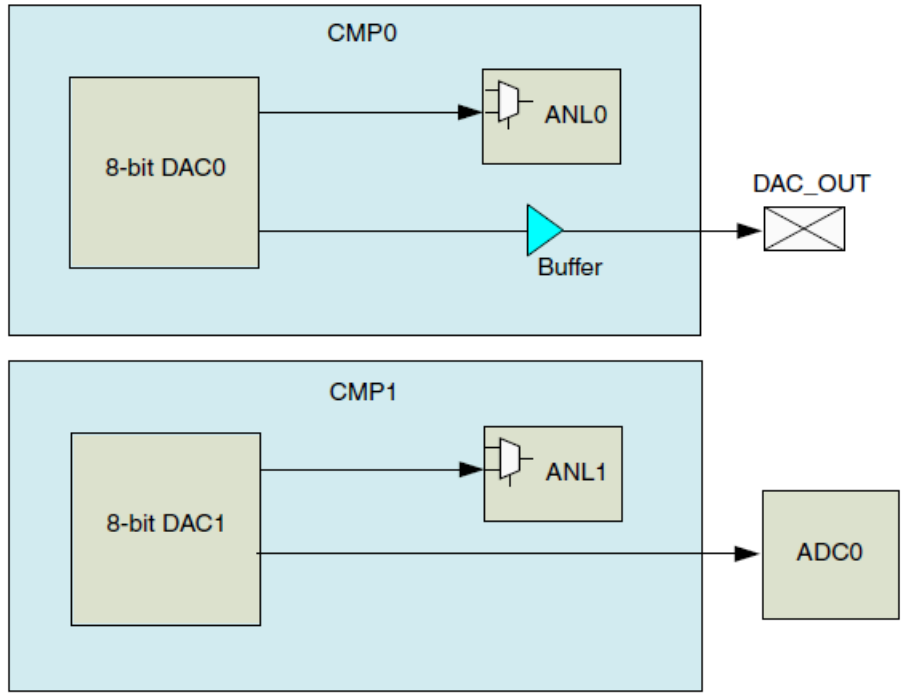

Figure 6. KE15Z ACMP module

KE17Z512 has only one CMP module and does not support DAC buffer, so the output of DAC cannot be connected to external pins.

Note: *In tables Table 10 and Table 12, the pins marked with a * can be used either in KE15Z or KE17Z512.*

The pin assignment of KE15Z ACMP module is shown in Table 10 and DAC output pin is shown in Table 11.

Table 10. Pin assignments of KE15Z ACMP module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT0	HD Pins
26	17	PTE8*	ACMP0_IN3/TSI0_CH11*	
28	19	PTB4	ACMP1_IN2/TSI0_CH8	HD Pin
29	20	PTC3*	ADC0_SE11/ACMP0_IN4/EXTAL32*	
30	21	PTC2*	ADC0_SE10/ACMP0_IN5/XTAL32*	
39	25	PTC1	ADC0_SE9/ACMP1_IN3/TSI0_CH23	
40	26	PTC0	ADC0_SE8/ACMP1_IN4/TSI0_CH22	
41	-	PTD9	ACMP1_IN5	
57	37	PTA7	ADC0_SE3/ACMP1_IN1	
58	38	PTA6	ADC0_SE2/ACMP1_IN0	

Table 10. Pin assignments of KE15Z ACMP module*...continued*

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT0	HD Pins
78	49	PTA1*	ADC0_SE1/ACMP0_IN1/TSI0_CH18*	
79	50	PTA0*	ADC0_SE0/ACMP0_IN0/TSI0_CH17*	
96	62	PTC4*	ACMP0_IN2*	

Table 11. DAC output pin assignment of KE15Z ACMP module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT0
23	16	PTE9	DAC0_OUT

The pin assignments of KE17Z512 CMP module are shown in Table 12. KE17Z512 has no CMP1 module. The pin assignment of KE17Z512 CMP0 is same as KE15Z ACMP0.

Table 12. Pin assignments of KE17Z CMP module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT0
26	17	PTE8*	CMP0_IN3*/ADC0_SE1/TSI0_CH22
29	20	PTC3*	ADC0_SE7/CMP0_IN4*
30	21	PTC2*	ADC0_SE15/CMP0_IN5*
78	49	PTA1*	CMP0_IN1*/TSI1_CH3
79	50	PTA0*	CMP0_IN0*/TSI1_CH2
96	62	PTC4*	CMP0_IN2*

6.5 FlexTimer

Table 13 displays the features supported by the FlexTimer (FTM) module in KE17Z512.

Table 13. Features of the KE17Z512 FTM module

FTM Instance	Number of channels	Feature/usage	GTB_EN	Deadtime	Fault control	Quadrature decoder
FTM0	8	FTM enhanced features	Yes	Yes	Yes	No
FTM1	4	FTM basic features	Yes	Yes	No	No
FTM2	4	FTM basic features	Yes	Yes	No	No

The three FTM modules of KE15Z support all the features listed in Table 13, while the three FTM modules of KE17Z512 do not have the function of quadrature decoder. In addition, FTM1 and FTM2 do not have the function of fault control.

The pin assignments of FTM, based on KE15Z, are shown in Table 14.

The pins marked with an asterisk (*) are FTM pins with the same functionality in both KE15Z and KE17Z512.

Table 14. Pin assignments of KE15Z FTM modules

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	ALT4	ALT5	ALT6	HD pins
3	1	PTD1*	FTM0_CH3*					HD pin*
4	2	PTD0*	FTM0_CH2*					HD pin*
8	5	PTE5	-	FTM2_ QD_PHA	FTM2_CH3			
9	6	PTE4	-	FTM2_ QD_PHB	FTM2_CH2			
17		PTE14*	FTM0_FLT1*					
18	13	PTE3*	FTM0_FLT0*					
19		PTE12*	FTM0_FLT3*					
20		PTD17*	FTM0_FLT2*					
21	14	PTD16*	FTM0_CH1*					HD pin*
22	15	PTD15*	FTM0_CH0*					HD pin*
23	16	PTE9*	FTM0_CH7*					
26	17	PTE8*	FTM0_CH6*					
27	18	PTB5*	FTM0_CH5*					HD pin*
28	19	PTB4*	FTM0_CH4*					HD pin*
29	20	PTC3*	FTM0_CH3*					
30	21	PTC2*	FTM0_CH2*					
33	24	PTD5*	FTM2_CH3*					
34		PTD12*	FTM2_CH2*					
35		PTD11*	FTM2_CH1*	FTM2_ QD_PHA				
36		PTD10*	FTM2_CH0*	FTM2_ QD_PHB				
39	25	PTC1*	FTM0_CH1*					
40	26	PTC0*	FTM0_CH0*					
43	27	PTC17	FTM1_FLT3					
44	28	PTC16	FTM1_FLT2					
45	29	PTC15*	FTM1_CH3*					
46	30	PTC14*	FTM1_CH2*					
47	31	PTB3*	FTM1_CH1*					
48	32	PTB2*	FTM1_CH0*					
57	37	PTA7*	FTM0_FLT2*					
58	38	PTA6*	FTM0_FLT1*					
59	39	PTE7*	FTM0_CH7*					
62		PTA17*	FTM0_CH6*					
63		PTB17*	FTM0_CH5*					

Table 14. Pin assignments of KE15Z FTM modules*...continued*

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	ALT4	ALT5	ALT6	HD pins
64		PTB16*	FTM0_CH4*					
65		PTB15*	FTM0_CH3*					
66		PTB14*	FTM0_CH2*					
67	42	PTB13*	FTM0_CH1*					
68	43	PTB12*	FTM0_CH0*					
69	44	PTD4*	FTM0_FLT3*					
78	49	PTA1*	FTM1_CH1*			FTM1_ QD_PHA		
79	50	PTA0*	FTM2_CH1*			FTM2_ QD_PHA		
82		PTA16*	FTM1_CH3*					
83		PTA15*	FTM1_CH2*					
88		PTA14*	FTM0_FLT0*					
94	60	PTE0	-				FTM1_ FLT2	
95	61	PTC5*	FTM2_CH0*				FTM2_ QD_PHB	
96	62	PTC4*	FTM1_CH0*				FTM1_ QD_PHB	
99		PTA9	-				FTM1_ FLT3	

The 100-pin KE17Z512 package adds three pins that can be used as FTM output. The newly added pins are PTD8, PTB11, and PTB10 as shown in Table 15.

Table 15. Pin assignments of KE17Z512 FTM modules

KE17Z512100 LQFP	KE17Z51264 LQFP	Pin name	ALT2	ALT4	HD pins
3	1	PTD1*	FTM0_CH3*	FTM2_CH1	HD pin*
4	2	PTD0*	FTM0_CH2*	FTM2_CH0	HD pin*
8	5	PTE5*	-	FTM2_CH3	
9	6	PTE4*	-	FTM2_CH2	
17		PTE14*	FTM0_FLT1*		
18	13	PTE3*	FTM0_FLT0*		
19		PTE12*	FTM0_FLT3*		
20		PTD17*	FTM0_FLT2*		
21	14	PTD16*	FTM0_CH1*		HD pin*
22	15	PTD15*	FTM0_CH0*		HD pin*
23	16	PTE9*	FTM0_CH7*		
26	17	PTE8*	FTM0_CH6*		

Table 15. Pin assignments of KE17Z512 FTM modules*...continued*

KE17Z512100 LQFP	KE17Z51264 LQFP	Pin name	ALT2	ALT4	HD pins
27	18	PTB5*	FTM0_CH5*		HD pin*
28	19	PTB4*	FTM0_CH4*		HD pin*
29	20	PTC3*	FTM0_CH3*		
30	21	PTC2*	FTM0_CH2*		
33	24	PTD5*	FTM2_CH3*		
34		PTD12*	FTM2_CH2*		
35		PTD11*	FTM2_CH1*		
36		PTD10*	FTM2_CH0*		
39	25	PTC1*	FTM0_CH1*		
40	26	PTC0*	FTM0_CH0*		
42		PTD8	FTM0_CH7		
45	29	PTC15	FTM1_CH3*		
46	30	PTC14	FTM1_CH2*		
47	31	PTB3	FTM1_CH1*		
48	32	PTB2	FTM1_CH0*		
57	37	PTA7	FTM0_FLT2*		
58	38	PTA6	FTM0_FLT1*		
59	39	PTE7*	FTM0_CH7*		
62		PTA17*	FTM0_CH6*		
63		PTB17*	FTM0_CH5*		
64		PTB16*	FTM0_CH4*		
65		PTB15*	FTM0_CH3*		
66		PTB14*	FTM0_CH2*		
67	42	PTB13*	FTM0_CH1*		
68	43	PTB12*	FTM0_CH0*		
69	44	PTD4*	FTM0_FLT3*		
74		PTB11	FTM0_CH1		
75		PTB10	FTM0_CH0		
78	49	PTA1*	FTM1_CH1*		
79	50	PTA0*	FTM2_CH1*		
82		PTA16*	FTM1_CH3*		
83		PTA15*	FTM1_CH2*		
88		PTA14*	FTM0_FLT0*		
95	61	PTC5*	FTM2_CH0*		
96	62	PTC4*	FTM1_CH0*		

6.6 FlexIO

The TRGMUX module configures the trigger source of the FlexIO module of KE15Z. Alternatively, the trigger source of the FlexIO module of KE17Z512 can also be from two independent asynchronous clocks. The trigger source is determined by SIM_CHIPCTL[FLEXIOTRIGSEL] register. See Figure 7.

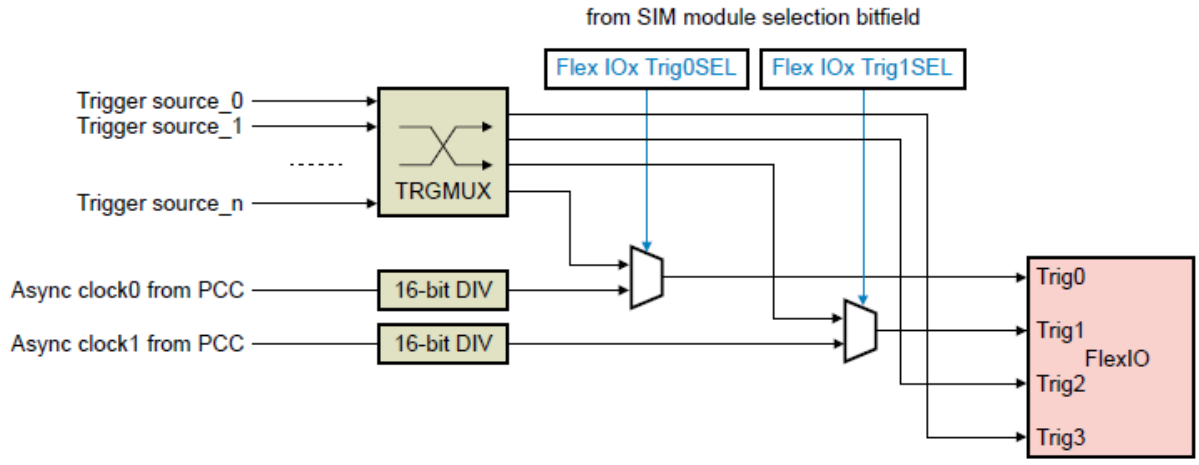

Figure 7. Trigger source selection of KE17Z512 FlexIO module

In addition to the option of configuring trigger source selection, the pin assignments for KE15Z and KE17Z512 FlexIO module are also different. The pins that can be used as FlexIO functions on KE15Z and KE17Z512 are shown in below Table 16.

The KE17Z512 in the 100LQFP package has 8 more FlexIO pins than KE15Z.

Note: *The pins marked with a * in Table 17are FlexIO pins in both KE15Z and KE17Z512. The newly added FlexIO pins are those unmarked in Table 17.*

Table 16 shows the pin assignment of KE15Z FlexIO module

Table 16. Pin assignments of the KE15Z FlexIO module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT4	ALT6	HD Pins
1	-	PTE16	-	FXIO_D3	-
2	-	PTE15	-	FXIO_D2	-
3	1	PTD1	-	FXIO_D1	HD Pin
4	2	PTD0	-	FXIO_D0	HD Pin
5	3	PTE11	-	FXIO_D5	-
6	4	PTE10	-	FXIO_D4	-
8	5	PTE5	-	FXIO_D7	-
9	6	PTE4	-	FXIO_D6	-
70	45	PTD3	FXIO_D5	-	-
71	46	PTD2	FXIO_D4	-	-
78	49	PTA1	FXIO_D3	-	-
79	50	PTA0	FXIO_D2	-	-
91	57	PTA11	FXIO_D1	-	-

Table 16. Pin assignments of the KE15Z FlexIO module*...continued*

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT4	ALT6	HD Pins
92	58	PTA10	FXIO_D0	-	-
99		PTA9	FXIO_D7	-	-
100		PTA8	FXIO_D6	-	-

Table 17 shows the pin assignment of KE17Z512 FlexIO module.

Table 17. Pin assignment of KE17Z512 FlexIO module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT4	ALT6	HD pins
1	-	PTE16*	-	FXIO_D3*	
2	-	PTE15*	-	FXIO_D2*	
3	1	PTD1*	-	FXIO_D1*	HD pin*
4	2	PTD0*	-	FXIO_D0*	HD pin*
5	3	PTE11*	-	FXIO_D5*	-
6	4	PTE10*	-	FXIO_D4*	-
8	5	PTE5*	-	FXIO_D7*	-
9	6	PTE4*	-	FXIO_D6*	-
29	20	PTC3	-	FXIO_D7	-
30	21	PTC2	-	FXIO_D6	-
33	24	PTD5	FXIO_D3	-	-
41	-	PTD9	-	FXIO_D2	-
70	45	PTD3*	FXIO_D5*	-	-
71	46	PTD2*	FXIO_D4*	-	-
74	-	PTB11	-	FXIO_D1	-
75	-	PTB10	-	FXIO_D0	-
76	-	PTB9	-	FXIO_D5	-
77	-	PTB8	-	FXIO_D4	-
78	49	PTA1*	FXIO_D3*	-	-
79	50	PTA0*	FXIO_D2*	-	-
91	57	PTA11*	FXIO_D1*	-	-
92	58	PTA10*	FXIO_D0*	-	-
99	-	PTA9*	FXIO_D7*	-	-
100	-	PTA8*	FXIO_D6*	-	

6.7 LPUART

Both KE17Z512 and KE15Z have three LPUART modules, which are identical in function, but their pin assignments are different. The pin assignment of the LPUART module in KE15Z is shown in Table 18.

Table 18. Pin assignment of KE15Z LPUART module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	ALT6
18	13	PTE3		LPUART2_RTS	
19		PTE12		LPUART2_TX	
20		PTD17		LPUART2_RX	
23	16	PTE9		LPUART2_CTS	
31	22	PTD7	LPUART2_TX		
32	23	PTD6	LPUART2_RX		
34	29	PTD12			LPUART2_RTS
35	30	PTD11			LPUART2_CTS
53	33	PTB1	LPUART0_TX		
54	34	PTB0	LPUART0_RX		
55	35	PTC9	LPUART1_TX		LPUART0_RTS
56	36	PTC8	LPUART1_RX		LPUART0_CTS
57	45	PTA7			LPUART1_RTS
58	46	PTA6			LPUART1_CTS
72	59	PTA3			LPUART0_TX
73	60	PTA2			LPUART0_RX
78	61	PTA1			LPUART0_RTS
79	62	PTA0			LPUART0_CTS
80	51	PTC7	LPUART1_TX		
81	52	PTC6	LPUART1_RX		
84	67	PTE6			LPUART1_RTS
85	68	PTE2			LPUART1_CTS
91	57	PTA11		LPUART0_RX	
92	58	PTA10		LPUART0_TX	

The pin assignment of KE17Z512 LPUART module is shown in Table 19. All pins that can be used as LPUART function in KE15Z in Table 18 also have the same function in KE17Z512 (marked with an asterisk). In addition, there are 9 other pins in KE17Z512 that can be used as LPUART function pins. These pins are not marked with an asterisk in Table 19.

Table 19. Pin assignment of KE17Z512 LPUART module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin Name	ALT2	ALT3	ALT5	ALT6	ALT7
15	11	PTB7		LPUART0_TX			
16	12	PTB6		LPUART0_RX			
18	13	PTE3*		LPUART2_ RTS*			
19		PTE12*		LPUART2_TX*			
20		PTD17*		LPUART2_RX*			

Table 19. Pin assignment of KE17Z512 LPUART module*...continued*

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin Name	ALT2	ALT3	ALT5	ALT6	ALT7
23	16	PTE9*		LPUART2_ CTS*			
24		PTD14		LPUART1_TX			
25		PTD13		LPUART1_RX			
31	22	PTD7*	LPUART2_ TX				
32	23	PTD6*	LPUART2_ RX				
33	24	PTD5					LPUART2_ CTS
34		PTD12*				LPUART2_ RTS*	
35		PTD11*				LPUART2_ CTS*	
53	33	PTB1*	LPUART0_ TX				
54	34	PTB0*	LPUART0_ RX				
55	35	PTC9*	LPUART1_ TX			LPUART0_ RTS*	
56	36	PTC8*	LPUART1_ RX			LPUART0_ CTS*	
57	37	PTA7*				LPUART1_ RTS*	
58	38	PTA6*				LPUART1_ CTS*	
72	47	PTA3*				LPUART0_TX*	
73	48	PTA2*				LPUART0_RX*	
78	49	PTA1*				LPUART0_ RTS*	
79	50	PTA0*				LPUART0_ CTS*	
80	51	PTC7*	LPUART1_ TX				
81	52	PTC6*	LPUART1_ RX				
84	53	PTE6*				LPUART1_ RTS*	
85	54	PTE2*				LPUART1_ CTS*	
89	55	PTA13			LPUART0_ RX		

Table 19. Pin assignment of KE17Z512 LPUART module*...continued*

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin Name	ALT2	ALT3	ALT5	ALT6	ALT7
90	56	PTA12			LPUART0_ TX		
91	57	PTA11*		LPUART0_RX*			
92	58	PTA10*		LPUART0_TX*			
96	62	PTC4		LPUART1_RX			
98	64	PTA4		LPUART1_TX			

6.8 SCI/UART

KE17Z512 adds two SCI module to increase the UART interface. The pins assignments of SCI0 and SCI1 are shown in Section 6.8 "SCI/UART".

Table 20. Pin assignment of SCI modules

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT4	ALT6
39	25	PTC1	SCI0_TX	-
40	26	PTC0	SCI0_RX	-
43	27	PTC17	-	SCI1_TX
44	28	PTC16	-	SCI1_RX
45	29	PTC15	SCI0_TX	-
46	30	PTC14	SCI0_RX	-
67	42	PTB13	-	SCI1_TX
68	43	PTB12	-	SCI1_RX

6.9 LPSPI

Both KE15Z256 and KE17Z512 have two LPSPI modules.

KE17Z512 has increased the max transmit frequency to 48 MHz, but the SCK, SOUT, and PCS pins of LPSPI0 and LPSPI1 are specified to achieve 48 MHz transmit. Refer to the Table 21 for the specified pins.

Table 21. LPSPI pins of KE17Z512 can achieve a 48 MHz transmit

Module	Pin name	Pin type
LPSPI1	PTD0/LPSPI1_SCK	HD pin
	PTD3/LPSPI1_PSC0	
	PTD2/LPSPI1_SOUT	
	PTA16/LPSPI1_PCS2	
LPSPI0	PTE0/LPSPI0_ SCK	HD pin
	PTE6/LPSPI0_PCS2	
	PTE2/LPSPI0_SOUT	

The pin assignment of the LPSPI module of KE15Z is shown in the Table 22. All pins used as LPSPI in KE15Z can also be used for LPSPI functions in KE17Z512. The pins marked with an asterisk symbol (*) in Table 22 are LPSPI pins present in both KE15Z256 and KE17Z512.

Table 22. Pin assignments of KE15Z LPSPI module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	HD pin
3	1	PTD1*		LPSPI1_SIN*	HD pin*
4	2	PTD0*		LPSPI1_SCK*	HD pin*
27	18	PTB5*		LPSPI0_PCS1*	HD pin*
28	19	PTB4*		LPSPI0_SOUT*	HD pin*
47	31	PTB3*		LPSPI0_SIN*	
48	32	PTB2*		LPSPI0_SCK*	
53	33	PTB1*		LPSPI0_SOUT*	
54	34	PTB0*		LPSPI0_PCS0*	
58	38	PTA6*		LPSPI1_PCS1*	
63		PTB17*		LPSPI1_PCS3*	
64		PTB16*		LPSPI1_SOUT*	
65		PTB15*		LPSPI1_SIN*	
66		PTB14*		LPSPI1_SCK*	
70	45	PTD3*		LPSPI1_PCS0*	
71	46	PTD2*		LPSPI1_SOUT*	
82		PTA16*		LPSPI1_PCS2*	
83		PTA15*		LPSPI0_PCS3*	
84	53	PTE6*	LPSPI0_PCS2*		
85	54	PTE2*	LPSPI0_SOUT*		
93	59	PTE1*	LPSPI0_SIN*		HD pin*
94	60	PTE0*	LPSPI0_SCK*		HD pin*

The pin assignments of the LPSPI module of KE17Z512 are shown in the Table 23. KE17Z512 has 6 more pins for LPSPI0 than KE15Z. These pins are shown marked in **bold font** .

Table 23. Pin assignments of KE17Z512 LPSPI module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT2	ALT3	ALT5	HD pins
3	1	PTD1		LPSPI1_SIN		HD
4	2	PTD0		LPSPI1_SCK		HD
27	18	PTB5		LPSPI0_PCS1		HD
28	19	PTB4		LPSPI0_SOUT		HD
42		**PTD8**			**LPSPI0_PCS1**	
47	31	PTB3		LPSPI0_SIN		
48	32	PTB2		LPSPI0_SCK		
49		**PTC13**			**LPSPI0_PCS0**	

Table 23. Pin assignments of KE17Z512 LPSPI module*...continued*

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT2	ALT3	ALT5	HD pins
50		**PTC12**			**LPSPI0_SOUT**	
51		**PTC11**			**LPSPI0_SIN**	
52		**PTC10**			**LPSPI0_SCK**	
53	33	PTB1		LPSPI0_SOUT		
54	34	PTB0		LPSPI0_PCS0		
57	37	**PTA7**		**LPSPI0_PCS3**		
58	38	PTA6		LPSPI1_PCS1		
63		PTB17		LPSPI1_PCS3		
64		PTB16		LPSPI1_SOUT		
65		PTB15		LPSPI1_SIN		
66		PTB14		LPSPI1_SCK		
70	45	PTD3		LPSPI1_PCS0		
71	46	PTD2		LPSPI1_SOUT		
82		PTA16		LPSPI1_PCS2		
83		PTA15		LPSPI0_PCS3		
84	53	PTE6	LPSPI0_PCS2			
85	54	PTE2	LPSPI0_SOUT			
93	59	PTE1	LPSPI0_SIN			HD
94	60	PTE0	LPSPI0_SCK			HD

6.10 LPI2C

Both KE15Z256 and KE17Z512 have two LPI2C modules. But there are some differences in the pin assignments of these two LP12C modules.

PTD9 and PTD8 can be configured as LPI2C1 pins for KE17Z512 and KE15Z256. To configure these two pins as LPI2C1 pins for KE15Z256, users must select pin mux ALT2. To configure these two pins as LPI2C1 pins for KE17Z512, users must select pin mux ALT3.

The pins with the same functions for KE17Z512 and KE15Z256 are marked with an asterisk (*).

Table 24 shows the pin assignments of the KE15Z LP12C module.

Table 24. Pin assignment of KE15Z LP12C module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	ALT4	HD pin
15	11	PTB7*	LPI2C0_SCL*			
16	12	PTB6*	LPI2C0_SDA*			
34		PTD12*		LPI2C1_HREQ*		
41		PTD9*	LPI2C1_SCL*			
42		PTD8*	LPI2C1_SDA*			

Table 24. Pin assignment of KE15Z LP12C module*...continued*

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT2	ALT3	ALT4	HD pin
43	27	PTC17*			LPI2C1_SCLS*	
44	28	PTC16*			LPI2C1_SDAS*	
72	47	PTA3*		LPI2C0_SCL*		
73	48	PTA2*		LPI2C0_SDA*		
74		PTB11*		LPI2C0_HREQ*		
75		PTB10*		LPI2C0_SDAS*		
76		PTB9*		LPI2C0_SCLS*		
78	49	PTA1*		LPI2C0_SDAS*		
79	50	PTA0*		LPI2C0_SCLS*		
89	55	PTA13*			LPI2C1_SCLS*	
90	56	PTA12*			LPI2C1_SDAS*	
93	59	PTE1*		LPI2C0_HREQ*	LPI2C1_SCL*	HD Pin
94	60	PTE0*			LPI2C1_SDA*	HD Pin
95	61	PTC5*			LPI2C1_HREQ*	

Table 25 shows the pin assignments of the KE17Z512 LPI2C module. KE17Z512 has two more LPI2C0 pins than KE15Z. These pins (PTD3 and PTD2) are marked in bold font in Table 25.

Table 25. Pin assignment of the KE17Z512 LPI2C module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT2	ALT3	ALT4	ALT5	HD pins
15	11	PTB7*	LPI2C0_SCL*				
16	12	PTB6*	LPI2C0_SDA*				
34		PTD12*		LPI2C1_HREQ*			
41		PTD9*		**LPI2C1_SCL**			
42		PTD8*		**LPI2C1_SDA**			
43	27	PTC17*			LPI2C1_SCLS*		
44	28	PTC16*			LPI2C1_SDAS*		
70	45	**PTD3**				**LPI2 C0_SCL**	
71	46	**PTD2**				**LPI2C0_ SDA**	
72	47	PTA3*		LPI2C0_SCL*			
73	48	PTA2*		LPI2C0_SDA*			
74		PTB11*		LPI2C0_HREQ*			
75		PTB10*		LPI2C0_SDAS*			
76		PTB9*		LPI2C0_SCLS*			
78	49	PTA1*		LPI2C0_SDAS*			

Table 25. Pin assignment of the KE17Z512 LPI2C module*...continued*

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin name	ALT2	ALT3	ALT4	ALT5	HD pins
79	50	PTA0*		LPI2C0_SCLS*			
89	55	PTA13*			LPI2C1_SCLS*		
90	56	PTA12*			LPI2C1_SDAS*		
93	59	PTE1*		LPI2C0_HREQ*	LPI2C1_SCL*		HD*
94	60	PTE0*			LPI2C1_SDA*		HD*
95	61	PTC5*			LPI2C1_HREQ*		

6.11 Trigger Mux

Compared with KE15Z, due to the different peripheral resources, the number of trigger controllers of the peripherals in the Trigger Mux (TRGMUX) module is also different. KE17Z512 does not have the trigger controllers listed in Table 26.

Table 26. Trigger controllers not available in KE17Z512

TRGMUX_ADC1
TRGMUX_CMP1
TRGMUX_PDB0

Since there are two TSI modules in KE17Z512, the TRGMUX_TSI1 register is added to the TRGMUX module. Also, the TRGMUX_LPUART2 register is added to KE17Z512.

The external input and output pins of the TRGMUX module in KE17Z512 and KE15Z are also different.

Table 27 shows the pin assignments of the TRGMUX in KE15Z256. The KE15Z TRGMUX module has 8 external input pins and 8 TRGMUX_OUT pins.

Table 27. Pin assignment of KE15Z256 TRGMUX module

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT6	ALT7	HD pins
1	-	PTE16	-	TRGMUX_OUT7	-
2	-	PTE15	-	TRGMUX_OUT6	-
3	1	PTD1	-	TRGMUX_OUT2	HD
4	2	PTD0	-	TRGMUX_OUT1	HD
5	3	PTE11	-	TRGMUX_OUT5	-
6	4	PTE10	-	TRGMUX_OUT4	-
18	13	PTE3	TRGMUX_IN6	-	-
27	18	PTB5	TRGMUX_IN0	-	HD
28	19	PTB4	TRGMUX_IN1	-	HD
33	24	PTD5	TRGMUX_IN7	-	-
47	31	PTB3	TRGMUX_IN2	-	-
48	32	PTB2	TRGMUX_IN3	-	-
70	45	PTD3	TRGMUX_IN4	-	-

Table 27. Pin assignment of KE15Z256 TRGMUX module*...continued*

KE15Z 100LQFP	KE15Z 64LQFP	Pin name	ALT6	ALT7	HD pins
71	46	PTD2	TRGMUX_IN5	-	-
78	49	PTA1	-	TRGMUX_OUT0	-
79	50	PTA0	-	TRGMUX_OUT3	-

Table 28 shows the pin assignment of KE17Z512 TRGMUX module.

KE17Z512 has 6 TRGMUX_OUT pins more than KE15Z256. These pins are marked in **bold font** in Table 28.

Table 28. Pin assignment of KE17Z512 TRGMUX module

KE17Z512 100LQFP	KE17Z512 64LQFP	Pin Name	ALT6	ALT7	HD pins
1	-	PTE16	-	TRGMUX_OUT7	-
2	-	PTE15	-	TRGMUX_OUT6	-
3	1	PTD1	-	TRGMUX_OUT2	HD
4	2	PTD0	-	TRGMUX_OUT1	HD
5	3	PTE11	-	TRGMUX_OUT5	-
6	4	PTE10	-	TRGMUX_OUT4	-
7	-	**PTE13**	-	**TRGMUX_OUT5**	-
17	-	**PTE14**	-	**TRGMUX_OUT4**	-
18	13	PTE3	TRGMUX_IN6		-
19	-	**PTE12**	-	**TRGMUX_OUT3**	-
20	-	**PTD17**	-	**TRGMUX_OUT2**	-
27	18	PTB5	TRGMUX_IN0	-	HD
28	19	PTB4	TRGMUX_IN1	-	HD
33	24	PTD5	TRGMUX_IN7	-	-
47	31	PTB3	TRGMUX_IN2	-	-
48	32	PTB2	TRGMUX_IN3	-	-
70	45	PTD3	TRGMUX_IN4	-	-
71	46	PTD2	TRGMUX_IN5	-	-
78	49	PTA1	-	TRGMUX_OUT0	-
79	50	PTA0	-	TRGMUX_OUT3	-
99	-	**PTA9**	-	**TRGMUX_OUT1**	-
100	-	**PTA8**	-	**TRGMUX_OUT0**	-

6.12 Real time Clock (RTC)

Both KE15Z and KE17Z512 have an RTC module. As there is no 32K oscillator in KE17Z512, the RTC 32 kHz clock is selected from the RTC clock input (RTC_CLKIN) and System Oscillator clock (SOSC_CLK). For KE15Z, the RTC 32 kHZ clock is selected from RTC clock input (RTC_CLKIN) and the 32K oscillator in the device.

KE15Z RTC supports the access control function. However, RTC of KE17Z512 does not support the access control function. Therefore, the RTC_WAR and RTC_RAR registers only exist in KE15Z.

Table 29 shows the pin assignments of KE15Z RTC clock input and output pins. KE15Z has one more RTC clock output pin than KE17Z512.

Note: *The pins marked with an asterisk are RTC clock input or output pins present in both KE15Z and KE17Z512.*

Table 29. Pin assignments of KE15Z RTC clock input and output pins

KE15Z (100LQFP)	KE15Z (64LQFP)	Pin name	ALT3	ALT4	ALT7
25		PTD13*			RTC_CLKOUT*
57	37	PTA7*		RTC_CLKIN*	
95	61	PTC5*	RTC_CLKOUT*		
96	62	PTC4	RTC_CLKOUT		

Table 30 shows the pin assignment of KE17Z512 RTC clock input and output pins.

Table 30. Pin assignments of KE17Z512 RTC clock input and output pins

KE17Z512 (100LQFP)	KE17Z512 (64LQFP)	Pin Name	ALT3	ALT4	ALT7
25		PTD13*			RTC_CLKOUT*
57	37	PTA7*		RTC_CLKIN*	
95	61	PTC5*	RTC_CLKOUT*		

6.13 Pulse Width Timer (PWT) module

Both KE15Z and KE17Z512 devices have a Pulse Width Timer (PWT) module. The function and PWT input channels are same. PWT input channels are from TRGMUX output and PWT input pins. Table 31 shows the pin assignment of KE17Z512 and KE15Z PWT.

Table 31. Pin assignments of KE17Z512 and KE15Z PWT

KE15Z KE17Z512 (100LQFP)	KE15Z KE17Z512 (64LQFP)	Pin name	ALT2	ALT5
5	3	PTE11	PWT_IN1	
33	24	PTD5		PWT_IN2
54	34	PTB0		PWT_IN3
85	54	PTE2		PWT_IN3

6.14 Clock pins

The pin assignments of BUSOUT, CLKOUT, TCLK0, TCLK1, and TCLK2 pins are the same in KE15Z and KE17Z512 devices. Table 32 shows the clock pin assignments of KE15Z and KE17Z512 100LQFP and 64LQFP packages.

Table 32. Pin assignments of KE15Z and KE17Z512 clock pins

KE15Z KE17Z512 (100LQFP)	KE15Z KE17Z512 (64LQFP)	Pin name	ALT2	ALT3	ALT4	ALT7	HD pins
6	4	PTE10	CLKOUT	-	-	-	-
8	5	PTE5	TCLK2	-	-	-	-
9	6	PTE4	BUSOUT	-	-	-	-
24		PTD14	-	-	-	CLKOUT	-
53	33	PTB1	-	-	TCLK0	-	-
88		PTA14	-	-	-	BUSOUT	-
94	60	PTE0	-	TCLK1	-	-	HD
97	63	PTA5	-	TCLK1	-	-	-

7 System

7.1 Reset and Boot

Unlike KE15Z, KE17Z512 only supports booting from Flash, not ROM. There is no ROM in KE17Z512 device. Therefore, the definition of Flash Option Register (FTFE_FOPT) is different. The definition of FTFE_FOPT of KE17Z512 is shown in the Table 33.

Table 33. KE17Z512 Flash Option Register (FTFE_FOPT) definition

Bit Num	Field	Value	Definition
7	Reserved	Reserved for future expansion.	
6	Reserved	Reserved for future expansion.	
5-4	Reserved	Reserved for future expansion.	
3	RESET_PIN_CFG	Enables/disables control for the RESET pin.	
		0	RESET_b pin is disabled following a POR and cannot be enabled as a reset function. When this option is selected, there can be a short period of contention. This occurs during a POR ramp where the device drives the pin low prior to establishing the setting of this option and releasing the reset function on the pin. When the RESET pin is disabled and configured as a GPIO output, it operates as a pseudo open drain output. This bit is preserved through system resets and low-power modes. When the RESET_b pin function is disabled, it cannot be used as a source for low-power mode wake-up. ***Note:*** *When the reset pin is disabled and security is enabled by using the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MDM-AP register.*
		1	RESET_b pin is dedicated. The port is configured with pull-up enabled, open drain, passive filter enabled.
2	NMI_DIS	Enables/disables control for the NMI function.	
		0	NMI interrupts are always blocked. The associated pin continues to default to NMI_b pin controls with internal pullup enabled. When the NMI_b pin function is disabled, it cannot be used as a source for low-power mode wake-up. If the NMI function is not required, either for an interrupt or wake-up source, it is recommended to disable the NMI function by clearing NMI_DIS.
		1	NMI_b pin/interrupts reset default to enabled.
1	Reserved	Reserved for future expansion.	
0	LPBOOT	Controls the reset value of the clock divider of IRC48M to feed the core clock. Larger divide value selections produce lower average power consumption during POR and reset sequencing and after reset exit.	
		0	Low-power boot: Core and system clock divider (DIVCORE) is 0x1 (divide by 2)
		1	Normal boot: Core and system clock divider (DIVCORE) is 0x0 (divide by 1).

In KE15Z, bit 1 of FTFA is BOOTPIN_OPT, bit [6: 7] is BOOTSRC_SEL. These bits are not used in KE17Z512.

7.2 MMDVSQ

There is no MMDVSQ module in KE17Z512, so it does not support hardware integer division operations, including 32/32 signed (SDIV) and unsigned (UDIV) calculations.

7.3 BME

KE17Z512 has no bit manipulation engine (BME) module.

8 Software

This section describes the process to easily port applications from the KE15Z platform to the KE17Z512 platform from the software aspect.

8.1 SDK driver

As compared to KE15Z, the KE17Z512 does not have Programmable Delay Block (PDB) and Memory-Mapped Divide and Square Root module (MMDVSQ) modules. Therefore, the KE17Z512 SDK does not provide the driver files for these modules.

8.1.1 Start up file

As compared with KE15Z, KE17Z512 lacks some peripheral modules. Therefore, their interrupt vector table is different. The difference is marked in bold font in Table 34.

Table 34. Interrupt vector table comparison

Address	Vector	IRQ	NVIC IPR Register number	KE15Z256 source module	KE17Z512 source module
Arm Core System Handler Vectors					
0x0000_0000	0	–	–	CSTACK	CSTACK
0x0000_0004	1	–	–	Reset_Handler	Reset_Handler
0x0000_0008	2	–	–	NMI	NMI
0x0000_000C	3	–	–	Hardfault	Hardfault
0x0000_0010	4	–	–	—	—
0x0000_0014	5	–	–	—	—
0x0000_0018	6	–	–	—	—
0x0000_001C	7	–	–	—	—
0x0000_0020	8	–	–	—	—
0x0000_0024	9	–	–	—	—
0x0000_0028	10	–	–	—	—
0x0000_002C	11	–	–	SVCall	SVCall
0x0000_0030	12	–	–	—	—
0x0000_0034	13	–	–	—	—
0x0000_0038	14	–	–	PendSV	PendSV
0x0000_003C	15	–	–	Systick	Systick
Non-Core On Platform Vectors					
0x0000_0040	16	0	0	DMA_04	DMA_04
0x0000_0044	17	1	0	DMA_15	DMA_15
0x0000_0048	18	2	0	DMA_26	DMA_26
0x0000_004C	19	3	0	DMA_37	DMA_37
0x0000_0050	20	4	1	DMA_Error	DMA_Error

Table 34. Interrupt vector table comparison*...continued*

Address	Vector	IRQ	NVIC IPR Register number	KE15Z256 source module	KE17Z512 source module
Off Platform IRQ Vectors					
0x0000_0054	21	5	1	Flash Memory	Flash Memory
0x0000_0058	22	6	1	PMC	PMC
0x0000_005C	23	7	1	PORTAE	PORTAE
0x0000_0060	24	8	2	LPI2C0	LPI2C0
0x0000_0064	25	—	—	LPI2C1	LPI2C1
0x0000_0068	26	10	2	LPSPI0	LPSPI0
0x0000_006C	27	—	—	LPSPI1	LPSPI1
0x0000_0070	28	12	3	LPUART0	LPUART0
0x0000_0074	29	13	3	LPUART1	LPUART1
0x0000_0078	30	14	3	LPUART2	LPUART2
0x0000_007C	31	15	3	ADC0	ADC0
0x0000_0080	32	16	4	CMP0	CMP0
0x0000_0084	33	17	4	FTM0	FTM0
0x0000_0088	34	18	4	FTM1	FTM1
0x0000_008C	35	19	4	FTM2	FTM2
0x0000_0090	36	—	—	RTC	RTC
0x0000_0094	37	—	—	**CMP1**	**SCI0**
0x0000_0098	38	22	5	LPIT	LPIT
0x0000_009C	39	23	5	FlexIO	FlexIO
0x0000_00A0	40	24	6	TSI	TSI0
0x0000_00A4	41	25	6	**PDB0**	**TSI1**
0x0000_00A8	42	26	6	PORTBCD	PORTBCD
0x0000_00AC	43	27	6	SCG	SCG
0x0000_00B0	44	28	7	WDOG_EWM	WDOG_EWM
0x0000_00B4	45	29	7	PWT_ LPTMR	PWT_ LPTMR
0x0000_00B8	46	—	—	**ADC1**	**SCI1**
0x0000_00BC	47	31	7	RCM	RCM

The interrupt vector table is defined in the startup files (`startup_MKE15Z7.s` and `startup_MKE17Z9.s`). Therefore, when migrating from the KE15Z256 platform to the KE17Z512 platform, users must replace the startup file.

8.1.2 Linker file

The SRAM size and flash size of KE15Z and KE17Z512 devices are different. Therefore, the address range of the usable SRAM and flash in the linker file is different. Therefore, when porting the code, the linker file of KE17Z512 must be used to replace the linker file of KE15Z.

9 Conclusion

This application note compares the differences in system resources and software between KE15Z and KE17Z512. Users can refer to this document to easily migrate projects from KE15Z256 to KE17Z512.

10 References

For more information, refer to the following:

1. KE17Z512 Reference Manual (*KE1XZP100M96SF0RM*)
2. KE15Z Reference Manual (*KE1xZP100M72SF0RM*)
3. KE17Z datasheet (*KE1xZP100M96SF0*)
4. KE15Z datasheet (*KE1xZP100M72SF0*)
5. Documents available at the URL: https://www.nxp.com/design/design-center/development-boards-and-designs/general-purpose-mcus/frdm-development-board-for-96-mhz-ke17z-ke13z-ke12z-with-512-kb-flash-mcus:FRDM-KE17Z512#documentation

11 Acronyms

Table 35 lists and explains the acronyms and abbreviations used in this document.

Table 35. Acronyms

Term	Description
AWIC	Asynchronous Wake-up Interrupt Controller
ADC	Analog-to-digital converter
BME	Bit manipulation engine
CLK	Clock
DIO	Data input/output
FAC	Flash access control
FMC	Flash memory controller
FTM	FlexTimer
LPI2C	Low-power Inter-Integrated Circuit (I2C)
LPUART	Low-power Universal Asynchronous Receiver Transmitter
MCU	Microcontroller Unit
MMDVSQ	Memory-Mapped Divide and Square Root module
NMI	Non-maskable interrupt
MCU-Link	The NXP single, unified debug probe architecture for all NXP general-purpose Arm Cortex-M based MCUs.
PDB	Programmable Delay Block
PWM	Pulse Width Modulation
PWT	Pulse Width Timer
RTC	Real Time Clock
SWD	Serial Wire Debug
TSI	Touch Sensing Input
UART	Universal Asynchronous Receiver Transmitter
DNP	Do not populate

12 Revision history

Table 36 summarizes the revisions to this document.

Table 36. Revision history

Document ID	Release date	Description
AN14202 V1.0	7 May 2024	Initial public release

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