AN13429

Migration Guide from KE15Z256 to KE17Z256

Rev. 0 — 02 November 2021 Application Note

Contents

1 Introduction

NXP® KE17Z is a new product of NXP Kinetis E Series after the KE18F, KE15Z, KE16Z, and has many similarities with KE15Z Series. It has the upgraded TSI function, which can realize more complex touch solutions. This application note compares the differences between KE17Z256 and KE15Z256, and aims to provide customers with a migration guide between the two platforms.

There are four parts in the KE15Z256 Series, see Table 1.

Table 1. KE15Z256 Series

Device	Frequency (MHz)	Flash (KB)	SRAM (KB)	FlexMem (KB)	TSI (Ch)	GPIO	ADC (Ch)	Package (LQFP)
MKE15Z256VLL7	72	256	32	32	25	89	16	100
MKE15Z256VLH7	72	256	32	32	-	58	16	64
MKE15Z128VLL7	72	128	16	32	25	89	16	100
MKE15Z128VLH7	72	128	16	32	-	58	16	64

The KE17Z256 Series currently has four parts, see Table 2.

Table 2. KE17Z256 Series

Device	Frequency (MHz)	Flash (KB)	SRAM (KB)	TSI (Ch)	GPIO	ADC (Ch)	Package
MKE17Z256VLL7	72	256	**48**	**50**	89	16	100
MKE17Z256VLH7	72	256	**48**	**47**	58	16	64
MKE17Z128VLL7	72	128	**32**	**50**	89	16	100
MKE17Z128VLH7	72	128	**32**	**47**	58	16	64

NOTE

In the KE17Z256 Series, there will be a 48LQFP package part in the future.

In the following, if there is no special description, KE15Z and KE17Z are KE15Z256 and KE17Z256 respectively.

For KE17Z system block diagram, see Figure 1.

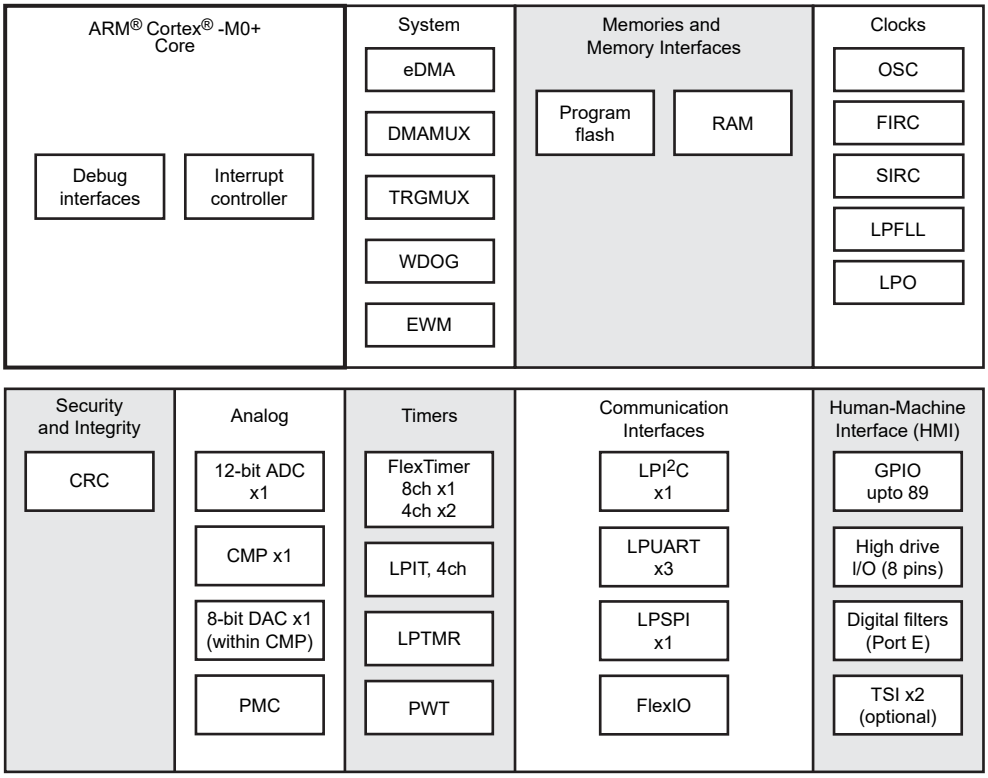

Figure 1. KE17Z system block diagram

For the comparison of KE15Z and KE17Z (in terms of system resources), see Table 3.

Table 3. Comparison of system resources between KE17Z and KE15Z

System resource	KE15Z256	KE17Z256
Core	72 MHz Arm Cortex-M0+	72 MHz Arm Cortex-M0+
Flash	256 KB	256 KB
RAM	32 KB	48 KB
EEPROM / FlexMemory	2 KB / 32 KB	-
Boot ROM	Yes	-
eDMA	8 ch	8 ch
HW Acceleration	MMDVSQ+BME	-
RWW	Yes	-
Clock System	IRC48M (±1 %) + IRC8M (±3 %) + LPFLL + LPO + OSC32K + OSC4-40M	IRC48M (±1 %) + IRC8M (±3 %) + LPFLL + LPO + OSC4-40M
ADC	2x 12bit ADC, 1 Msps	1x 12bit ADC, 1 Msps
ACMP / DAC buffer	2 / 1	1 / 0
FlexTimers	1x 8ch + 2x 4ch FTM	1x 8ch + 2x 4ch FTM (removed deadtime and quadrature decode)

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Table 3. Comparison of system resources between KE17Z and KE15Z (continued)

System resource	KE15Z256	KE17Z256
General Timers	4ch 32-bit LPIT + 16-bit LPTMR + PDB	4ch 32-bit LPIT + 16-bit LPTMR
PWT	1	1
RTC	Yes	No
UART / SPI / I2C	3 / 2 / 2	3 / 1 / 1
FlexIO	Yes (4 timers + 4 shifters)	Yes (4 timers + 4 shifters)
TSI	1 x 25ch (each TSI have 1 shield channel)	2 x 25ch (each TSI have 3 shield channels)
Package	100LQFP, 64LQFP	100LQFP, 64LQFP, 48LQFP (TBD)

The following section of this document provides the comparison and differences between KE15Z and KE17Z in terms of memory, clock, and peripherals.

2 Memory

This section compares the differences between KE15Z256 and KE17Z256 in terms of memory.

2.1 Flash memory

The flash size of KE15Z256 and KE17Z256 is 256 KB, but KE17Z does not have FlexMemory. FlexMemory on KE15Z can be used as 32 KB flash or 2 KB EEPROM. KE17Z also has no boot ROM. When operating the flash of KE17Z, only one array is accessible at a time through the platform slave port, so Read-While-Write (RWW) is not supported.

KE17Z also has no Flash Access Control (FAC) function. FAC is a configurable memory protection scheme designed to allow end users to utilize software libraries while offering programmable restrictions to these libraries. This allows NXP or third-party vendors to pre-program software libraries into a chip and distribute parts to end customers who can use the pre-programmed software libraries.

2.2 SRAM memory

The SRAM size of KE15Z is 32 KB and the SRAM size of KE17Z is 48 KB. For the memory comparison of KE15Z and KE17Z, see Table 4.

Table 4. KE17Z and KE15Z memory comparison

Memory	KE15Z256	KE17Z256
Flash	256 KB (0x0000_0000–0x0003_FFFF)	256 KB (0x0000_0000–0x0003_FFFF)
FlexNVM	32 KB (0x1000_0000–0x1000_7FFF)	No
FlexRAM	2 KB (0x1400_0000–0x1400_07FF)	No
SRAM	32 KB	48 KB

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Table 4. KE17Z and KE15Z memory comparison (continued)

Memory	KE15Z256	KE17Z256
	(0x1FFF_E000-0x2000_5FFF)	(0x1FFF_C000-0x2000_7FFF)
Boot ROM	16 KB (0x1C00_0000-0x1C00_3FFF)	No

3 Clock distribution

See Figure 2 for the clock distribution of KE17Z.

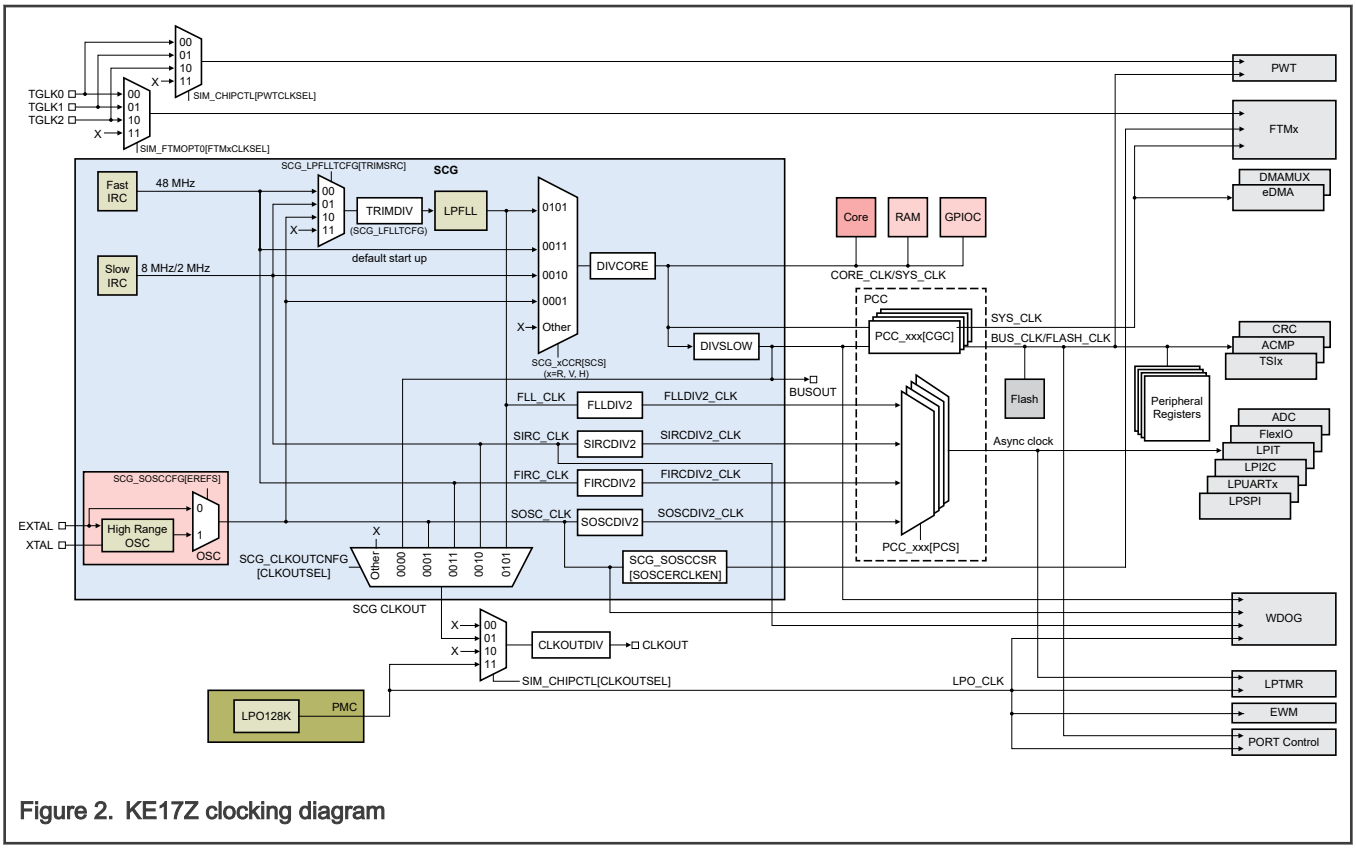

Figure 2. KE17Z clocking diagram

Compared with the KE15Z clock system, there is no OSC32 module on the KE17Z, so the LPTMR cannot choose `OSC32_CLK` as the clock source. The KE17Z also does not have RTC module.

4 Pinout

For the KE17Z in 100LQFP and 64LQFP packages, its pin assignment is compatible with the KE15Z, that is, the number and position of GPIO pins are the same, see Figure 3, but the pin multiplexing function on some GPIO ports is different. For the pin assignment of each peripheral, see Peripheral.

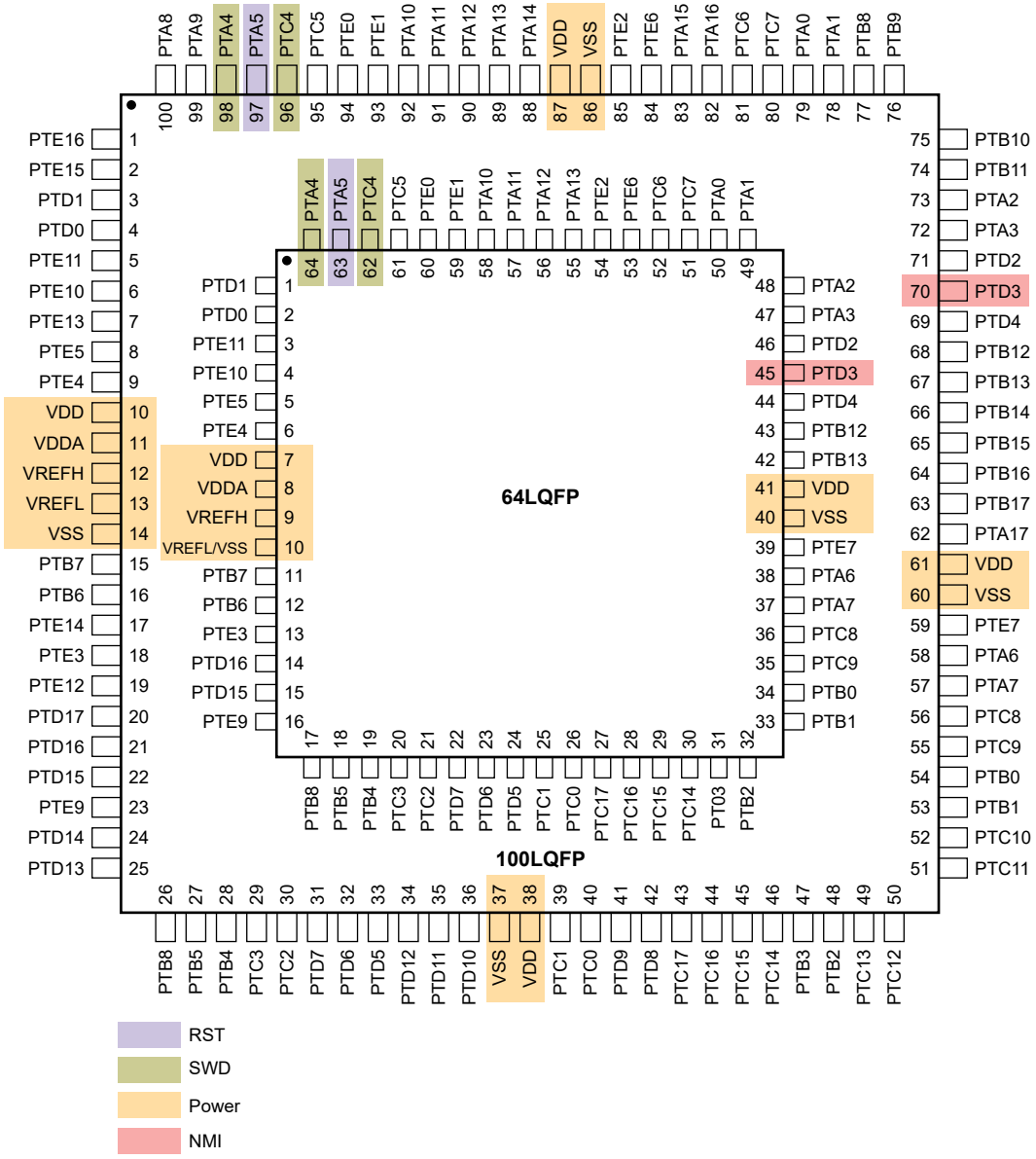

Figure 3. KE17Z pinout in 100LQFP and 64LQFP packages

5 Peripheral

This section compares the differences between KE15Z256 and KE17Z256 in terms of peripherals.

5.1 Touch Sensing Input (TSI)

The KE17Z has two TSI modules, each module has 25 TSI channels, a total of 50 TSI channels, and each TSI module has three shield channels, the shield channels are CH4, CH12, and CH21. The KE15Z has only one TSI module, a total of 25 TSI channels, and only one shield channel. For the TSI0 module, the TSI channel assignment of KE17Z and KE15Z is also very different. For the TSI channel assignment of the KE15Z, see Table 5.

Table 5. Pin assignment of the KE15Z TSI module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	HD pins
3	1	1	PTD1	**TSI0_CH5**	PTD1	HD pin
4	2	2	PTD0	**TSI0_CH4**	PTD0	HD pin
5	3	3	PTE11	**TSI0_CH3**	PTE11	-
6	4	4	PTE10	**TSI0_CH2**	PTE10	-
8	6	5	PTE5	**TSI0_CH0**	PTE5	-
9	7	6	PTE4	**TSI0_CH1**	PTE4	-
18	15	13	PTE3	**TSI0_CH24**	PTE3	-
26	21	17	PTE8	**ACMP0_IN3/TSI0_CH11**	PTE8	-
27	22	18	PTB5	**TSI0_CH9**	PTB5	HD pin
28	23	19	PTB4	**ACMP1_IN2/TSI0_CH8**	PTB4	HD pin
31	26	22	PTD7	*TSI0_CH10*	PTD7	-
32	27	23	PTD6	*TSI0_CH7*	PTD6	-
33	28	24	PTD5	*TSI0_CH6*	PTD5	-
39	31	25	PTC1	**ADC0_SE9/ACMP1_IN3/TSI0_CH23**	PTC1	-
40	32	26	PTC0	**ADC0_SE8/ACMP1_IN4/TSI0_CH22**	PTC0	-
47	39	31	PTB3	**ADC0_SE7/TSI0_CH21**	PTB3	-
48	40	32	PTB2	**ADC0_SE6/TSI0_CH20**	PTB2	-
78	61	49	PTA1	**ADC0_SE1/ACMP0_IN1/TSI0_CH18**	PTA1	-
79	62	50	PTA0	**ADC0_SE0/ACMP0_IN0/TSI0_CH17**	PTA0	-
80	63	51	PTC7	**ADC1_SE5/TSI0_CH16**	PTC7	-
81	64	52	PTC6	**ADC1_SE4/TSI0_CH15**	PTC6	-
85	68	54	PTE2	**ADC1_SE10/TSI0_CH19**	PTE2	-
93	75	59	PTE1	**TSI0_CH14**	PTE1	HD pin
94	76	60	PTE0	**TSI0_CH13**	PTE0	HD pin
95	77	61	PTC5	**TSI0_CH12**	PTC5	-

The pins corresponding to the "Bold" text can be used as TSI pins in both chips, but their corresponding TSI channels may be different. The pin corresponding to the "italic" text is the unique pin of the current chip that can be used as a TSI pin.

For the pin assignment of the TSI module of the KE17Z, see Table 6.

Table 6. Pin assignment of the KE17Z TSI module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	HD pins
1	-	-	PTE16	*TSI0_CH13*	PTE16	-
2	-	-	PTE15	*TSI0_CH14*	PTE15	-
3	1	1	PTD1	**TSI0_CH11**	PTD1	HD pin
4	2	2	PTD0	**TSI0_CH12**	PTD0	HD pin
5	3	3	PTE11	**TSI0_CH9**	PTE11	-
6	4	4	PTE10	**TSI0_CH10**	PTE10	-
7	-	-	PTE13	*TSI0_CH15*	PTE13	-
8	5	5	PTE5	**TSI0_CH16**	PTE5	-
9	6	6	PTE4	**TSI0_CH17**	PTE4	-
18	13	13	PTE3	**ADC0_SE6/TSI0_CH18**	PTE3	-
21	14	-	PTD16	*ADC0_SE4/TSI0_CH19*	PTD16	HD pin
22	15	-	PTD15	*ADC0_SE2/TSI0_CH20*	PTD15	HD pin
23	16	-	PTE9	*ADC0_SE0/TSI0_CH21*	PTE9	-
26	17	14	PTE8	**ACMP0_IN3/ADC0_SE1/TSI0_CH22**	PTE8	-
27	18	15	PTB5	**ADC0_SE3/TSI0_CH23**	PTB5	HD pin
28	19	16	PTB4	**ADC0_SE5/TSI0_CH24**	PTB4	HD pin
39	25	22	PTC1	**ADC0_SE8/TSI1_CH24**	PTC1	-
40	26	23	PTC0	**ADC0_SE10/TSI1_CH23**	PTC0	-
43	27	-	PTC17	*ADC0_SE12/TSI1_CH22*	PTC17	-
44	28	-	PTC16	*ADC0_SE14/TSI1_CH21*	PTC16	-
45	29	-	PTC15	*TSI1_CH20*	PTC15	-
46	30	-	PTC14	*TSI1_CH19*	PTC14	-
47	31	24	PTB3	**TSI1_CH18**	PTB3	-

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Table 6. Pin assignment of the KE17Z TSI module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	HD pins
48	32	25	PTB2	**TSI1_CH17**	PTB2	_
53	33	26	PTB1	*TSI1_CH16*	PTB1	_
54	34	27	PTB0	*TSI1_CH15*	PTB0	_
55	35	_	PTC9	*TSI1_CH14*	PTC9	_
56	36	_	PTC8	*TSI1_CH13*	PTC8	_
57	37	28	PTA7	*TSI1_CH12*	PTA7	_
58	38	29	PTA6	*TSI1_CH11*	PTA6	_
59	39	_	PTE7	*TSI1_CH10*	PTE7	_
67	42	_	PTB13	*TSI1_CH9*	PTB13	_
68	43	_	PTB12	*TSI1_CH8*	PTB12	_
69	44	32	PTD4	*TSI1_CH7*	PTD4	_
71	46	34	PTD2	*TSI1_CH6*	PTD2	_
72	47	35	PTA3	*TSI1_CH5*	PTA3	_
73	48	36	PTA2	*TSI1_CH4*	PTA2	_
78	49	37	PTA1	**ACMP0_IN1/TSI1_CH3**	PTA1	_
79	50	38	PTA0	**ACMP0_IN0/TSI1_CH2**	PTA0	_
80	51	39	PTC7	**TSI1_CH1**	PTC7	_
81	52	40	PTC6	**TSI1_CH0**	PTC6	_
84	53	41	PTE6	*TSI0_CH0*	PTE6	_
85	54	42	PTE2	**TSI0_CH1**	PTE2	_
89	55	_	PTA13	*TSI0_CH2*	PTA13	_
90	56	_	PTA12	*TSI0_CH3*	PTA12	_
91	57	_	PTA11	*TSI0_CH4*	PTA11	_
92	58	_	PTA10	*TSI0_CH5*	PTA10	_
93	59	43	PTE1	**TSI0_CH6**	PTE1	HD pin

Table continues on the next page...

Table 6. Pin assignment of the KE17Z TSI module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	HD pins
94	60	44	PTE0	**TSI0_CH7**	PTE0	HD pin
95	61	45	PTC5	**TSI0_CH8**	PTC5	-

The pins corresponding to the "Bold" text can be used as TSI pins in both chips, but their corresponding TSI channels may be different. The pin corresponding to the "italic" text is the unique pin of the current chip that can be used as a TSI pin.

5.2 Programmable Delay Block (PDB)

The KE17Z256 has no PDB module.

5.3 Analog-to-Digital Converter (ADC)

The KE15Z256 has two ADC modules, and each module has two data registers. For different packages, the number of external channels supported by each module is also different, see Table 7. The KE17Z256 has only one ADC module `ADC0`, but it has four result registers, and the `ADC0` external channel assignment is also different from the KE15Z, see Table 8.

Table 7. Pin assignment of the KE15Z ADC module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1
29	24	20	PTC3	**ADC0_SE11/ACMP0_IN4/EXTAL32**	PTC3
30	25	21	PTC2	**ADC0_SE10/ACMP0_IN5/XTAL32**	PTC2
39	31	25	PTC1	**ADC0_SE9/ACMP1_IN3/TSI0_CH23**	PTC1
40	32	26	PTC0	**ADC0_SE8/ACMP1_IN4/TSI0_CH22**	PTC0
43	35	27	PTC17	*ADC0_SE15*	PTC17
44	36	28	PTC16	**ADC0_SE14**	PTC16
45	37	29	PTC15	*ADC0_SE13*	PTC15
46	38	30	PTC14	*ADC0_SE12*	PTC14
47	39	31	PTB3	*ADC0_SE7/TSI0_CH21*	PTB3
48	40	32	PTB2	*ADC0_SE6/TSI0_CH20*	PTB2
53	41	33	PTB1	*ADC0_SE5*	PTB1
54	42	34	PTB0	*ADC0_SE4*	PTB0
57	45	37	PTA7	*ADC0_SE3/ACMP1_IN1*	PTA7
58	46	38	PTA6	*ADC0_SE2/ACMP1_IN0*	PTA6

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Table 7. Pin assignment of the KE15Z ADC module (continued)

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1
66	53		PTB14	*ADC1_SE9*	PTB14
67	54	42	PTB13	*ADC1_SE8*	PTB13
68	55	43	PTB12	*ADC1_SE7*	PTB12
69	56	44	PTD4	*ADC1_SE6*	PTD4
70	57	45	PTD3	*ADC1_SE3*	PTD3
71	58	46	PTD2	*ADC1_SE2*	PTD2
72	59	47	PTA3	*ADC1_SE1*	PTA3
73	60	48	PTA2	*ADC1_SE0*	PTA2
78	61	49	PTA1	*ADC0_SE1/ACMP0_IN1/TSI0_CH18*	PTA1
79	62	50	PTA0	*ADC0_SE0/ACMP0_IN0/TSI0_CH17*	PTA0
80	63	51	PTC7	*ADC1_SE5/TSI0_CH16*	PTC7
81	64	52	PTC6	*ADC1_SE4/TSI0_CH15*	PTC6
84	67	53	PTE6	*ADC1_SE11*	PTE6
85	68	54	PTE2	*ADC1_SE10/TSI0_CH19*	PTE2

The pins corresponding to the "Bold" text can be used as ADC pins in both chips, but their corresponding ADC channels may be different. The pin corresponding to the "italic" text is the unique pin of the current chip that can be used as an ADC pin.

Table 8. Pin assignment of the KE17Z ADC module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1
18	13	13	PTE3	*ADC0_SE6/TSI0_CH18*	PTE3
21	14		PTD16	*ADC0_SE4/TSI0_CH19*	PTD16
22	15		PTD15	*ADC0_SE2/TSI0_CH20*	PTD15
23	16		PTE9	*ADC0_SE0/TSI0_CH21*	PTE9
26	17	14	PTE8	*ACMP0_IN3/ADC0_SE1/TSI0_CH22*	PTE8
27	18	15	PTB5	*ADC0_SE3/TSI0_CH23*	PTB5
28	19	16	PTB4	*ADC0_SE5/TSI0_CH24*	PTB4

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Table 8. Pin assignment of the KE17Z ADC module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1
29	20	17	PTC3	**ADC0_SE7/ACMP0_IN4**	PTC3
30	21	18	PTC2	**ADC0_SE15/ACMP0_IN5**	PTC2
31	22	19	PTD7	*ADC0_SE13*	PTD7
32	23	20	PTD6	*ADC0_SE11*	PTD6
33	24	21	PTD5	*ADC0_SE9*	PTD5
39	25	22	PTC1	**ADC0_SE8/TSI1_CH24**	PTC1
40	26	23	PTC0	**ADC0_SE10/TSI1_CH23**	PTC0
43	27	-	PTC17	*ADC0_SE12/TSI1_CH22*	PTC17
44	28	-	PTC16	**ADC0_SE14/TSI1_CH21**	PTC16

The pins corresponding to the "Bold" text can be used as ADC pins in both chips, but their corresponding ADC channels may be different. The pin corresponding to the "italic" text is the unique pin of the current chip that can be used as an ADC pin.

For the 100LQFP package, the ADC module of the KE15Z has 28 single-ended input pins, and KE17Z has 16 single-ended input pins. In addition to the different pin assignments, the ADC trigger source is also different. The KE17Z does not have a PDB module, so the ADC does not have a trigger source from the PDB module, and the `SIM_ADCOPT[ADCxTRGSEL]` bit does not exist.

5.4 Analog Comparator (ACMP)

The KE15Z has two ACMP modules, each ACMP module supports 6 external analog inputs, and each ACMP module has a built-in 8-bit DAC. `ACMP0` also has a DAC buffer through which the output of `DAC0` can be connected to an external pin, see Figure 4.

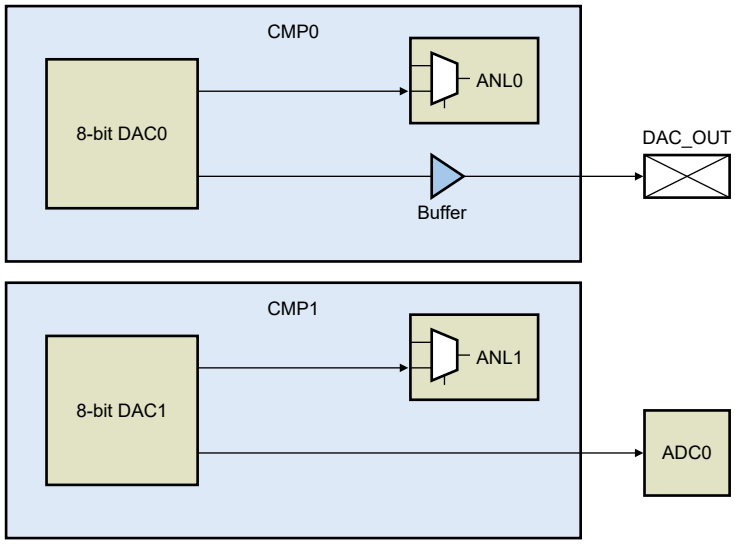

Figure 4. KE15Z ACMP module

The KE17Z has only one ACMP module and does not support DAC buffer, so the output of DAC cannot be connected to external pins.

For the pin assignment of KE15Z ACMP module, see Table 9.

Table 9. Pin assignment of the KE15Z ACMP module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	HD pins
26	21	17	PTE8	**ACMP0_IN3/TSI0_CH11**	PTE8	_
28	23	19	PTB4	*ACMP1_IN2/TSI0_CH8*	PTB4	HD pin
29	24	20	PTC3	**ADC0_SE11/ACMP0_IN4/EXTAL32**	PTC3	_
30	25	21	PTC2	**ADC0_SE10/ACMP0_IN5/XTAL32**	PTC2	_
39	31	25	PTC1	*ADC0_SE9/ACMP1_IN3/TSI0_CH23*	PTC1	_
40	32	26	PTC0	*ADC0_SE8/ACMP1_IN4/TSI0_CH22*	PTC0	_
41	33	_	PTD9	*ACMP1_IN5*	PTD9	_
57	45	37	PTA7	*ADC0_SE3/ACMP1_IN1*	PTA7	_
58	46	38	PTA6	*ADC0_SE2/ACMP1_IN0*	PTA6	_
78	61	49	PTA1	**ADC0_SE1/ACMP0_IN1/TSI0_CH18**	PTA1	_
79	62	50	PTA0	**ADC0_SE0/ACMP0_IN0/TSI0_CH17**	PTA0	_
96	78	62	PTC4	**ACMP0_IN2**	PTC4	_

NOTE

The functions listed in Table 9 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

For the pin assignment of the KE17Z ACMP module, see Table 10.

Table 10. Pin assignment of the KE17Z ACMP module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	HD pins
26	17	14	PTE8	**ACMP0_IN3/ADC0_SE1/TSI0_CH22**	PTE8	_
29	20	17	PTC3	**ADC0_SE7/ACMP0_IN4**	PTC3	_
30	21	18	PTC2	**ADC0_SE15/ACMP0_IN5**	PTC2	_
78	49	37	PTA1	**ACMP0_IN1/TSI1_CH3**	PTA1	_

Table continues on the next page...

Table 10. Pin assignment of the KE17Z ACMP module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	HD pins
79	50	38	PTA0	**ACMP0_IN0/TSI1_CH2**	PTA0	-
96	62	46	PTC4	**ACMP0_IN2**	PTC4	-

NOTE

The functions listed in Table 10 are as follows:

- The function in "**Bold**" text is common to the two chips.

The KE17Z has no `ACMP1` module. The pin assignment of `ACMP0` is the same as KE15Z.

5.5 FlexTimer (FTM)

The features supported by the FTM module in the KE17Z, see Table 11.

Table 11. The features of the KE17Z FTM module

FTM instance	Number of channels	Feature / usage	GTB_EN	Deadtime	Fault control	Quadrature decoder
FTM0	8	FTM enhanced features	YES	YES	YES	NO
FTM1	4	FTM basic features	YES	YES	NO	NO
FTM2	4	FTM basic features	YES	YES	NO	NO

The three FTM modules of the KE15Z support all the features listed in Table 11, while the three FTM modules of the KE17Z do not have the function of quadrature decoder. In addition, FTM1 and FTM2 do not have the function of fault control.

For the pin assignment of FTM, KE17Z in the 100 LQPF package adds three pins that can be used as FTM output. For the newly added pins, see Table 12.

Table 12. Newly added pins on the KE17Z that can be used as FTM channels

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	DEFAULT	ALT0	ALT1	ALT2
42	-	-	PTD8	DISABLED	-	PTD8	FTM0_CH7
74	-	-	PTB11	DISABLED	-	PTB11	FTM0_CH1
75	-	-	PTB10	DISABLED	-	PTB10	FTM0_CH0

5.6 Flexible I/O (FlexIO)

The trigger source of the KE15Z FlexIO module comes from the TRGMUX module. The trigger source of the FlexIO module of KE17Z cannot only come from the TRGMUX module but also from two independent asynchronous clocks. The trigger source is determined by `SIM_CHIPCTL[FLEXIOTRIGSEL]`. For details, see Figure 5.

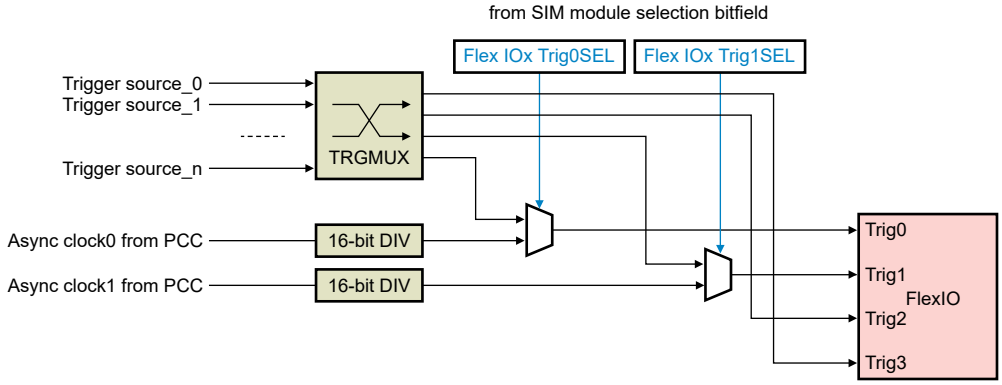

Figure 5. Trigger source selection of the KE17Z FlexIO module

In addition to the different trigger source selection, the pin assignments are also different. The pins that can be used as FlexIO functions on the KE15Z are listed in Table 13.

Table 13. Pin assignment of the KE15Z FlexIO module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	ALT4	ALT6	HD pins
1	-	-	PTE16	-	PTE16	-	**FXIO_D3**	-
2	-	-	PTE15	-	PTE15	-	**FXIO_D2**	-
3	1	1	PTD1	TSI0_CH5	PTD1	FTM2_CH1	**FXIO_D1**	HD pin
4	2	2	PTD0	TSI0_CH4	PTD0	FTM2_CH0	**FXIO_D0**	HD pin
5	3	3	PTE11	TSI0_CH3	PTE11	-	**FXIO_D5**	-
6	4	4	PTE10	TSI0_CH2	PTE10	-	**FXIO_D4**	-
8	6	5	PTE5	TSI0_CH0	PTE5	FTM2_CH3	**FXIO_D7**	-
9	7	6	PTE4	TSI0_CH1	PTE4	FTM2_CH2	**FXIO_D6**	-
29	24	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	-	-	-
30	25	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	-	-	-
33	28	24	PTD5	TSI0_CH6	PTD5	-	TRGMUX_IN7	-
41	33		PTD9	ACMP1_IN5	PTD9	FTM2_FLT3	-	-
70	57	45	PTD3	ADC1_SE3	PTD3	**FXIO_D5**	TRGMUX_IN4	-
71	58	46	PTD2	ADC1_SE2	PTD2	**FXIO_D4**	TRGMUX_IN5	-
74	-	-	PTB11	-	PTB11	-	-	-

Table continues on the next page...

Table 13. Pin assignment of the KE15Z FlexIO module (continued)

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	ALT4	ALT6	HD pins
75	-	-	PTB10	-	PTB10	-	-	-
76	-	-	PTB9	-	PTB9	-	-	-
77	-	-	PTB8	-	PTB8	-	-	-
78	61	49	PTA1	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	PTA1	**FXIO_D3**	LPUART0_RTS	-
79	62	50	PTA0	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	PTA0	**FXIO_D2**	LPUART0_CTS	-
91	73	57	PTA11	-	PTA11	**FXIO_D1**	-	-
92	74	58	PTA10	-	PTA10	**FXIO_D0**	-	-
99	-	-	PTA9	-	PTA9	**FXIO_D7**	FTM1_FLT3	-
100	-	-	PTA8	-	PTA8	**FXIO_D6**	-	-

NOTE

The functions listed in Table 13 are as follows:

- The function in "**Bold**" text is common to the two chips.

For pin assignment of the KE17Z FlexIO, see Table 14.

Table 14. Pin assignment of the KE17Z FlexIO module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT4	ALT6	HD pins
1	-	-	PTE16	TSI0_CH13	PTE16	-	**FXIO_D3**	-
2	-	-	PTE15	TSI0_CH14	PTE15	-	**FXIO_D2**	-
3	1	1	PTD1	TSI0_CH11	PTD1	FTM2_CH1	**FXIO_D1**	HD pin
4	2	2	PTD0	TSI0_CH12	PTD0	FTM2_CH0	**FXIO_D0**	HD pin
5	3	3	PTE11	TSI0_CH9	PTE11	-	**FXIO_D5**	-
6	4	4	PTE10	TSI0_CH10	PTE10	-	**FXIO_D4**	-
8	5	5	PTE5	TSI0_CH16	PTE5	FTM2_CH3	**FXIO_D7**	-
9	6	6	PTE4	TSI0_CH17	PTE4	FTM2_CH2	**FXIO_D6**	-
29	20	17	PTC3	ADC0_SE7/ ACMP0_IN4	PTC3	-	*FXIO_D7*[1]	-

Table continues on the next page...

Table 14. Pin assignment of the KE17Z FlexIO module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT4	ALT6	HD pins
30	21	18	PTC2	ADC0_SE15/ ACMP0_IN5	PTC2	-	*FXIO_D6*[1]	-
33	24	21	PTD5	ADC0_SE9	PTD5	*FXIO_D3*[1]	TRGMUX_IN7	-
41			PTD9	DISABLED	PTD9	-	*FXIO_D2*[1]	-
70	45	33	PTD3	DISABLED	PTD3	**FXIO_D5**	TRGMUX_IN4	-
71	46	34	PTD2	TSI1_CH6	PTD2	**FXIO_D4**	TRGMUX_IN5	-
74	-	-	PTB11	-	PTB11	-	*FXIO_D1*[1]	-
75	-	-	PTB10	-	PTB10	-	*FXIO_D0*[1]	-
76	-	-	PTB9	-	PTB9	-	*FXIO_D5*[1]	-
77	-	-	PTB8	-	PTB8	LPI2C0_SCL	*FXIO_D4*[1]	-
78	49	37	PTA1	ACMP0_IN1/ TSI1_CH3	PTA1	**FXIO_D3**	LPUART0_RTS	-
79	50	38	PTA0	ACMP0_IN0/ TSI1_CH2	PTA0	**FXIO_D2**	LPUART0_CTS	-
91	57	-	PTA11	TSI0_CH4	PTA11	**FXIO_D1**	-	-
92	58	-	PTA10	TSI0_CH5	PTA10	**FXIO_D0**	-	-
99	-	-	PTA9	-	PTA9	**FXIO_D7**	-	-
100	-	-	PTA8	-	PTA8	**FXIO_D6**	-	-

1. New pins

NOTE

The functions listed in Table 14 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

The KE17Z of 100LQFP package has eight more FlexIO pins than KE15Z, see Table 14.

5.7 Low-Power Universal Asynchronous Receiver / Transmitter (LPUART)

Both KE17Z and KE15Z have three LPUART modules, which are identical in function, but their pin assignments are different. For the pin assignment of the LPUART module in KE15Z, see Table 15.

Table 15. Pin assignment of the KE15Z LPUART module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT1	ALT2	ALT3	ALT5	ALT6
15	13	11	PTB7	PTB7	LPI2C0_SCL	-	-	-

Table continues on the next page...

Table 15. Pin assignment of the KE15Z LPUART module (continued)

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT1	ALT2	ALT3	ALT5	ALT6
16	14	12	PTB6	PTB6	LPI2C0_SDA	-	-	-
18	15	13	PTE3	PTE3	FTM0_FLT0	**LPUART2_RTS**	-	TRGMUX_IN6
19	16	-	PTE12	PTE12	FTM0_FLT3	**LPUART2_TX**	-	-
20	17	-	PTD17	PTD17	FTM0_FLT2	**LPUART2_RX**	-	-
23	20	16	PTE9	PTE9	FTM0_CH7	**LPUART2_CTS**	-	-
24		-	PTD14	PTD14	-	-	-	-
25		-	PTD13	PTD13	-	-	-	-
31	26	22	PTD7	PTD7	**LPUART2_TX**	-	-	-
32	27	23	PTD6	PTD6	**LPUART2_RX**	-	-	-
33	28	24	PTD5	PTD5	FTM2_CH3	LPTMR0_ALT2	PWT_IN2	TRGMUX_IN7
34	29	-	PTD12	PTD12	FTM2_CH2	LPI2C1_HREQ	-	**LPUART2_RTS**
35	30	-	PTD11	PTD11	FTM2_CH1	FTM2_QD_PHA	-	**LPUART2_CTS**
53	41	33	PTB1	PTB1	**LPUART0_TX**	LPSPI0_SOUT	-	-
54	42	34	PTB0	PTB0	**LPUART0_RX**	LPSPI0_PCS0	PWT_IN3	-
55	43	35	PTC9	PTC9	**LPUART1_TX**	-	-	**LPUART0_RTS**
56	44	36	PTC8	PTC8	**LPUART1_RX**	-	-	**LPUART0_CTS**
57	45	37	PTA7	PTA7	FTM0_FLT2	-	-	**LPUART1_RTS**
58	46	38	PTA6	PTA6	FTM0_FLT1	LPSPI1_PCS1	-	**LPUART1_CTS**
72	59	47	PTA3	PTA3	-	LPI2C0_SCL	-	**LPUART0_TX**
73	60	48	PTA2	PTA2	-	LPI2C0_SDA	-	**LPUART0_RX**
78	61	49	PTA1	PTA1	FTM1_CH1	LPI2C0_SDAS	FTM1_QD_PHA	**LPUART0_RTS**
79	62	50	PTA0	PTA0	FTM2_CH1	LPI2C0_SCLS	FTM2_QD_PHA	**LPUART0_CTS**
80	63	51	PTC7	PTC7	**LPUART1_TX**	-	-	-
81	64	52	PTC6	PTC6	**LPUART1_RX**	-	-	-
84	67	53	PTE6	PTE6	LPSPI0_PCS2	-	-	**LPUART1_RTS**
85	68	54	PTE2	PTE2	LPSPI0_SOUT	LPTMR0_ALT3	PWT_IN3	**LPUART1_CTS**
89	71	55	PTA13	PTA13	-	-	-	-
90	72	56	PTA12	PTA12	-	-	-	-
91	73	57	PTA11	PTA11	-	**LPUART0_RX**	-	-
92	74	58	PTA10	PTA10	-	**LPUART0_TX**	-	-

Table continues on the next page...

Table 15. Pin assignment of the KE15Z LPUART module (continued)

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT1	ALT2	ALT3	ALT5	ALT6
96	78	62	PTC4	PTC4	FTM1_CH0	RTC_CLKOUT	EWM_IN	FTM1_QD_PHB
98	80	64	PTA4	PTA4	-	-	EWM_OUT_b	-

NOTE

The functions listed in Table 15 are as follows:

- The function in "**Bold**" text is common to the two chips.

For the pin assignment of KE17Z LPUART module, see Table 16.

Table 16. Pin assignment of the KE17Z LPUART module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT1	ALT2	ALT3	ALT5	ALT6	ALT7
15	11	11	PTB7	PTB7	LPI2C0_SCL	*LPUART0_TX*[1]	-	-	-
16	12	12	PTB6	PTB6	LPI2C0_SDA	*LPUART0_RX*[1]	-	-	-
18	13	13	PTE3	PTE3	FTM0_FLT0	**LPUART2_RTS**	-	TRGMUX_IN6	-
19	-	-	PTE12	PTE12	FTM0_FLT3	**LPUART2_TX**	-	-	TRGMUX_OUT3
20	-	-	PTD17	PTD17	FTM0_FLT2	**LPUART2_RX**	-	-	TRGMUX_OUT2
23	16	-	PTE9	PTE9	FTM0_CH7	**LPUART2_CTS**	-	-	-
24	-	-	PTD14	PTD14	-	*LPUART1_TX*[1]	-	-	CLKOUT
25	-	-	PTD13	PTD13	-	*LPUART1_RX*[1]	-	-	-
31	22	19	PTD7	PTD7	**LPUART2_TX**	-	-	-	-
32	23	20	PTD6	PTD6	**LPUART2_RX**	-	-	-	-
33	24	21	PTD5	PTD5	FTM2_CH3	LPTMR0_ALT2	PWT_IN2	TRGMUX_IN7	*LPUART2_CTS*[1]
34	-	-	PTD12	PTD12	FTM2_CH2	-	-	**LPUART2_RTS**	-
35	-	-	PTD11	PTD11	FTM2_CH1	-	-	**LPUART2_CTS**	-
53	33	26	PTB1	PTB1	**LPUART0_TX**	LPSPI0_SOUT	-	-	-
54	34	27	PTB0	PTB0	**LPUART0_RX**	LPSPI0_PCS0	PWT_IN3	-	-
55	35	-	PTC9	PTC9	**LPUART1_TX**	-	-	**LPUART0_RTS**	-

Table continues on the next page...

Table 16. Pin assignment of the KE17Z LPUART module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT1	ALT2	ALT3	ALT5	ALT6	ALT7
56	36	-	PTC8	PTC8	**LPUART1_RX**	-	-	**LPUART0_CTS**	-
57	37	28	PTA7	PTA7	FTM0_FLT2	LPSPI0_PCS3	-	**LPUART1_RTS**	-
58	38	29	PTA6	PTA6	FTM0_FLT1	-	-	**LPUART1_CTS**	-
72	47	35	PTA3	PTA3	-	LPI2C0_SCL	-	**LPUART0_TX**	-
73	48	36	PTA2	PTA2	-	LPI2C0_SDA	-	**LPUART0_RX**	-
78	49	37	PTA1	PTA1	FTM1_CH1	LPI2C0_SDAS	-	**LPUART0_RTS**	TRGMUX_OUT 0
79	50	38	PTA0	PTA0	FTM2_CH1	LPI2C0_SCLS	-	**LPUART0_CTS**	TRGMUX_OUT 3
80	51	39	PTC7	PTC7	**LPUART1_TX**	-	-	-	-
81	52	40	PTC6	PTC6	**LPUART1_RX**	-	-	-	-
84	53	41	PTE6	PTE6	LPSPI0_PCS2	-	-	**LPUART1_RTS**	-
85	54	42	PTE2	PTE2	LPSPI0_SOUT	LPTMR0_ALT3	PWT_IN3	**LPUART1_CTS**	-
89	55	-	PTA13	PTA13	-	-	*LPUART0_RX*[1]	-	-
90	56	-	PTA12	PTA12	-	-	*LPUART0_TX*[1]	-	-
91	57	-	PTA11	PTA11	-	**LPUART0_RX**	-	-	-
92	58	-	PTA10	PTA10	-	**LPUART0_TX**	-	-	-
96	62	46	PTC4	PTC4	FTM1_CH0	*LPUART1_RX*[1]	EWM_IN	-	SWD_CLK
98	64	48	PTA4	PTA4	-	*LPUART1_TX*[1]	EWM_OUT_b	-	SWD_DIO

1. Nine other pins in KE17Z that can be used as LPUART function pins.

NOTE

The functions listed in Table 16 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

The pins that can be used as LPUART function in KE15Z also have the same function in KE17Z, see Table 16.

5.8 Low Power Serial Peripheral Interface (LPSPI)

The KE15Z has two LPSPI modules, while KE17Z has only one LPSPI module, so the pins can be used as SPI functions on the KE17Z and are also different from the KE15Z. For the pin assignment of the LPSPI module of KE15Z, see Table 17.

Table 17. Pin assignment of the KE15Z LPSPI module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	ALT2	ALT3	HD pins
3	1	1	PTD1	TSI0_CH5	PTD1	FTM0_CH3	**LPSPI1_SIN**	HD pin
4	2	2	PTD0	TSI0_CH4	PTD0	FTM0_CH2	**LPSPI1_SCK**	HD pin
27	22	18	PTB5	TSI0_CH9	PTB5	FTM0_CH5	**LPSPI0_PCS1**	HD pin
28	23	19	PTB4	ACMP1_IN2/ TSI0_CH8	PTB4	FTM0_CH4	**LPSPI0_SOUT**	HD pin
47	39	31	PTB3	ADC0_SE7/ TSI0_CH21	PTB3	FTM1_CH1	**LPSPI0_SIN**	-
48	40	32	PTB2	ADC0_SE6/ TSI0_CH20	PTB2	FTM1_CH0	**LPSPI0_SCK**	-
53	41	33	PTB1	ADC0_SE5	PTB1	LPUART0_TX	**LPSPI0_SOUT**	-
54	42	34	PTB0	ADC0_SE4	PTB0	LPUART0_RX	**LPSPI0_PCS0**	-
58	46	38	PTA6	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	*LPSPI1_PCS1*	-
63	50	-	PTB17	-	PTB17	FTM0_CH5	*LPSPI1_PCS3*	-
64	51	-	PTB16	-	PTB16	FTM0_CH4	*LPSPI1_SOUT*	-
65	52	-	PTB15	-	PTB15	FTM0_CH3	*LPSPI1_SIN*	-
66	53	-	PTB14	ADC1_SE9	PTB14	FTM0_CH2	*LPSPI1_SCK*	-
70	57	45	PTD3	ADC1_SE3	PTD3	-	*LPSPI1_PCS0*	-
71	58	46	PTD2	ADC1_SE2	PTD2	-	*LPSPI1_SOUT*	-
82	65	-	PTA16	-	PTA16	FTM1_CH3	*LPSPI1_PCS2*	-
83	66	-	PTA15	-	PTA15	FTM1_CH2	**LPSPI0_PCS3**	-
84	67	53	PTE6	ADC1_SE11	PTE6	**LPSPI0_PCS2**	-	-
85	68	54	PTE2	ADC1_SE10/ TSI0_CH19	PTE2	**LPSPI0_SOUT**	LPTMR0_ALT3	-
93	75	59	PTE1	TSI0_CH14	PTE1	**LPSPI0_SIN**	LPI2C0_HREQ	HD pin
94	76	60	PTE0	TSI0_CH13	PTE0	**LPSPI0_SCK**	TCLK1	HD pin

NOTE

The functions listed in Table 17 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

For the pin assignment of the LPSPI module of KE17Z, see Table 18.

Table 18. Pin assignment of the KE17Z LPSPI module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT2	ALT3	HD pins
3	1	1	PTD1	TSI0_CH11	PTD1	FTM0_CH3	-	HD pin
4	2	2	PTD0	TSI0_CH12	PTD0	FTM0_CH2	-	HD pin
27	18	15	PTB5	ADC0_SE3/ TSI0_CH23	PTB5	FTM0_CH5	**LPSPI0_PCS1**	HD pin
28	19	16	PTB4	ADC0_SE5/ TSI0_CH24	PTB4	FTM0_CH4	**LPSPI0_SOUT**	HD pin
47	31	24	PTB3	TSI1_CH18	PTB3	FTM1_CH1	**LPSPI0_SIN**	-
48	32	25	PTB2	TSI1_CH17	PTB2	FTM1_CH0	**LPSPI0_SCK**	-
53	33	26	PTB1	TSI1_CH16	PTB1	LPUART0_TX	**LPSPI0_SOUT**	-
54	34	27	PTB0	TSI1_CH15	PTB0	LPUART0_RX	**LPSPI0_PCS0**	-
58	38	29	PTA6	TSI1_CH11	PTA6	FTM0_FLT1	-	-
63	-	-	PTB17	-	PTB17	FTM0_CH5	-	-
64	-	-	PTB16	-	PTB16	FTM0_CH4	-	-
65	-	-	PTB15	-	PTB15	FTM0_CH3	-	-
66	-	-	PTB14	DISABLED	PTB14	FTM0_CH2	-	-
70	45	33	PTD3	DISABLED	PTD3	-	-	-
71	46	34	PTD2	TSI1_CH6	PTD2	-	-	-
82	-	-	PTA16	-	PTA16	FTM1_CH3	-	-
83	-	-	PTA15	-	PTA15	FTM1_CH2	**LPSPI0_PCS3**	-
84	53	41	PTE6	TSI0_CH0	PTE6	**LPSPI0_PCS2**	-	-
85	54	42	PTE2	TSI0_CH1	PTE2	**LPSPI0_SOUT**	LPTMR0_ALT3	-
93	59	43	PTE1	TSI0_CH6	PTE1	**LPSPI0_SIN**	LPI2C0_HREQ	HD pin
94	60	44	PTE0	TSI0_CH7	PTE0	**LPSPI0_SCK**	TCLK1	HD pin

NOTE

The functions listed in Table 18 are as follows:

- The function in "**Bold**" text is common to the two chips.

There are no pins used as LPSPI1 module in the KE17Z, the pin assignment of LPSPI0 module is the same as the KE15Z.

5.9 Low Power Inter-Integrated Circuit (LPI2C)

The KE15Z has two LPI2C module, while the KE17Z has only one LPI2C module, there is no LP12C1 module in the KE17Z, so there is no pin that can be used as LP12C1 function, the pin assignment of LP12C0 module is exactly the same as in the KE15Z. For more details, see Table 19 and Table 20.

Table 19. Pin assignment of the KE15Z LP12C module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin name	ALT0	ALT1	ALT2	ALT3	ALT4	HD pins
15	13	11	PTB7	EXTAL	PTB7	**LPI2C0_SCL**	-	-	-
16	14	12	PTB6	XTAL	PTB6	**LPI2C0_SDA**	-	-	-
34	29	-	PTD12	-	PTD12	FTM2_CH2	*LPI2C1_HREQ*	-	-
41	33	-	PTD9	ACMP1_IN5	PTD9	**LPI2C1_SCL**	-	FTM2_FLT3	-
42	34	-	PTD8	-	PTD8	**LPI2C1_SDA**	-	FTM2_FLT2	-
43	35	27	PTC17	ADC0_SE15	PTC17	FTM1_FLT3	-	*LPI2C1_SCLS*	-
44	36	28	PTC16	ADC0_SE14	PTC16	FTM1_FLT2	-	*LPI2C1_SDAS*	-
72	59	47	PTA3	ADC1_SE1	PTA3	-	**LPI2C0_SCL**	EWM_IN	-
73	60	48	PTA2	ADC1_SE0	PTA2	-	**LPI2C0_SDA**	EWM_OUT_b	-
74	-	-	PTB11	-	PTB11	-	**LPI2C0_HREQ**		-
75	-	-	PTB10	-	PTB10	-	**LPI2C0_SDAS**		-
76	-	-	PTB9	-	PTB9	-	**LPI2C0_SCLS**		-
78	61	49	PTA1	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	PTA1	FTM1_CH1	**LPI2C0_SDAS**	FXIO_D3	-
79	62	50	PTA0	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	PTA0	FTM2_CH1	**LPI2C0_SCLS**	FXIO_D2	-
89	71	55	PTA13	-	PTA13	-	-	*LPI2C1_SCLS*	-
90	72	56	PTA12	-	PTA12	-	-	*LPI2C1_SDAS*	-
93	75	59	PTE1	TSI0_CH14	PTE1	LPSPI0_SIN	**LPI2C0_HREQ**	*LPI2C1_SCL*	HD pin
94	76	60	PTE0	TSI0_CH13	PTE0	LPSPI0_SCK	TCLK1	*LPI2C1_SDA*	HD pin
95	77	61	PTC5	TSI0_CH12	PTC5	FTM2_CH0	RTC_CLKOUT	*LPI2C1_HREQ*	-

NOTE

The functions listed in Table 19 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

Table 20. Pin assignment of the KE17Z LPI2C module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT2	ALT3	ALT4	HD pins
15	11	11	PTB7	EXTAL	PTB7	**LPI2C0_SCL**	LPUART0_TX	-	-
16	12	12	PTB6	XTAL	PTB6	**LPI2C0_SDA**	LPUART0_RX	-	-
34	-	-	PTD12	-	PTD12	FTM2_CH2	-	-	-
41	-	-	PTD9	DISABLED	PTD9	-	-	-	-
42	-	-	PTD8	-	PTD8	FTM0_CH7	-	-	-
43	27	-	PTC17	ADC0_SE12/ TSI1_CH22	PTC17	-	-	-	-
44	28	-	PTC16	ADC0_SE14/ TSI1_CH21	PTC16	-	-	-	-
72	47	35	PTA3	TSI1_CH5	PTA3	-	**LPI2C0_SCL**	EWM_IN	-
73	48	36	PTA2	TSI1_CH4	PTA2	-	**LPI2C0_SDA**	EWM_OUT_b	-
74	-	-	PTB11	-	PTB11	FTM0_CH1	**LPI2C0_HREQ**	-	-
75	-	-	PTB10	-	PTB10	FTM0_CH0	**LPI2C0_SDAS**	-	-
76	-	-	PTB9	-	PTB9	-	**LPI2C0_SCLS**	-	-
78	49	37	PTA1	ACMP0_IN1/ TSI1_CH3	PTA1	FTM1_CH1	**LPI2C0_SDAS**	FXIO_D3	-
79	50	38	PTA0	ACMP0_IN0/ TSI1_CH2	PTA0	FTM2_CH1	**LPI2C0_SCLS**	FXIO_D2	-
80	51	39	PTC7	TSI1_CH1	PTC7	LPUART1_TX	-	-	-
90	56		PTA12	TSI0_CH3	PTA12	-	-	-	-
93	59	43	PTE1	TSI0_CH6	PTE1	LPSPI0_SIN	**LPI2C0_HREQ**	-	HD pin
94	60	44	PTE0	TSI0_CH7	PTE0	LPSPI0_SCK	TCLK1	-	HD pin
95	61	45	PTC5	TSI0_CH8	PTC5	FTM2_CH0	-	-	-

NOTE

The functions listed in Table 20 are as follows:

- The function in "**Bold**" text is common to the two chips.

5.10 Trigger Mux (TRGMUX)

Compared with the KE15Z, due to the different peripheral resources, the number of trigger controllers of the peripherals in the Trigger Mux (TRGMUX) module is also different. The KE17Z does not have the following trigger controller.

- TRGMUX_ADC1
- TRGMUX_CMP1
- TRGMUX_PDB0
- TRGMUX_LPUART1
- TRGMUX_LPI2C1
- TRGMUX_LPSPI1

Since there are two TSI modules in the KE17Z, the TRGMUX_TSI1 register is added to the TRGMUX module. The external input and output pins of the TRGMUX module in KE17Z and KE15Z are also different. For the pin assignment of the TRGMUX in KE15Z, see Table 21.

Table 21. Pin assignment of the KE15Z TRGMUX module

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin Name	ALT0	ALT1	ALT6	ALT7	HD pins
1	-	-	PTE16	-	PTE16	FXIO_D3	**TRGMUX_OUT7**	-
2	-	-	PTE15	-	PTE15	FXIO_D2	**TRGMUX_OUT6**	-
3	1	1	PTD1	TSI0_CH5	PTD1	FXIO_D1	**TRGMUX_OUT2**	HD pin
4	2	2	PTD0	TSI0_CH4	PTD0	FXIO_D0	**TRGMUX_OUT1**	HD pin
5	3	3	PTE11	TSI0_CH3	PTE11	FXIO_D5	**TRGMUX_OUT5**	-
6	4	4	PTE10	TSI0_CH2	PTE10	FXIO_D4	**TRGMUX_OUT4**	-
7	5	-	PTE13	-	PTE13	-	-	-
17	-	-	PTE14	-	PTE14	-	-	-
18	15	13	PTE3	TSI0_CH24	PTE3	**TRGMUX_IN6**	-	-
19	16	-	PTE12	-	PTE12	-	-	-
20	17	-	PTD17	-	PTD17	-	-	-
27	22	18	PTB5	TSI0_CH9	PTB5	**TRGMUX_IN0**	ACMP1_OUT	HD Pin
28	23	19	PTB4	ACMP1_IN2/ TSI0_CH8	PTB4	**TRGMUX_IN1**	-	HD Pin
33	28	24	PTD5	TSI0_CH6	PTD5	**TRGMUX_IN7**	-	-

Table continues on the next page...

Table 21. Pin assignment of the KE15Z TRGMUX module (continued)

KE15Z (100QFP)	KE15Z (80QFP)	KE15Z (64QFx)	Pin Name	ALT0	ALT1	ALT6	ALT7	HD pins
47	39	31	PTB3	ADC0_SE7/ TSI0_CH21	PTB3	**TRGMUX_IN2**	-	-
48	40	32	PTB2	ADC0_SE6/ TSI0_CH20	PTB2	**TRGMUX_IN3**	-	-
70	57	45	PTD3	ADC1_SE3	PTD3	**TRGMUX_IN4**	NMI_b	-
71	58	46	PTD2	ADC1_SE2	PTD2	**TRGMUX_IN5**	-	-
78	61	49	PTA1	ADC0_SE1/ ACMP0_IN1/ TSI0_CH18	PTA1	LPUART0_RTS	**TRGMUX_OUT0**	-
79	62	50	PTA0	ADC0_SE0/ ACMP0_IN0/ TSI0_CH17	PTA0	LPUART0_CTS	**TRGMUX_OUT3**	-
99	-	-	PTA9	-	PTA9	FTM1_FLT3	-	-
100	-	-	PTA8	-	PTA8	-	-	-

NOTE

The functions listed in Table 21 are as follows:

- The function in "**Bold**" text is common to the two chips.

For the pin assignment of the KE17Z TRGMUX module, see Table 22.

Table 22. Pin assignment of the KE17Z TRGMUX module

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT6	ALT7	HD pins
1	-	-	PTE16	TSI0_CH13	PTE16	FXIO_D3	**TRGMUX_OUT7**	-
2	-	-	PTE15	TSI0_CH14	PTE15	FXIO_D2	**TRGMUX_OUT6**	-
3	1	1	PTD1	TSI0_CH11	PTD1	FXIO_D1	**TRGMUX_OUT2**	HD pin
4	2	2	PTD0	TSI0_CH12	PTD0	FXIO_D0	**TRGMUX_OUT1**	HD pin
5	3	3	PTE11	TSI0_CH9	PTE11	FXIO_D5	**TRGMUX_OUT5**	-
6	4	4	PTE10	TSI0_CH10	PTE10	FXIO_D4	**TRGMUX_OUT4**	-
7	-	-	PTE13	TSI0_CH15	PTE13	-	*TRGMUX_OUT5*[1]	-

Table continues on the next page...

Table 22. Pin assignment of the KE17Z TRGMUX module (continued)

KE17Z (100QFP)	KE17Z (64QFx)	KE17Z (48QFx)	Pin name	ALT0	ALT1	ALT6	ALT7	HD pins
17	-	-	PTE14	-	PTE14	-	*TRGMUX_OUT4*[1]	-
18	13	13	PTE3	ADC0_SE6/ TSI0_CH18	PTE3	**TRGMUX_IN6**	-	-
19	-	-	PTE12	-	PTE12	-	*TRGMUX_OUT3*[1]	-
20	-	-	PTD17	-	PTD17	-	*TRGMUX_OUT2*[1]	-
27	18	15	PTB5	ADC0_SE3/ TSI0_CH23	PTB5	**TRGMUX_IN0**	-	HD pin
28	19	16	PTB4	ADC0_SE5/ TSI0_CH24	PTB4	**TRGMUX_IN1**	-	HD pin
33	24	21	PTD5	ADC0_SE9	PTD5	**TRGMUX_IN7**	LPUART2_CTS	-
47	31	24	PTB3	TSI1_CH18	PTB3	**TRGMUX_IN2**	-	-
48	32	25	PTB2	TSI1_CH17	PTB2	**TRGMUX_IN3**	-	-
70	45	33	PTD3	DISABLED	PTD3	**TRGMUX_IN4**	NMI_b	-
71	46	34	PTD2	TSI1_CH6	PTD2	**TRGMUX_IN5**	-	-
78	49	37	PTA1	ACMP0_IN1/ TSI1_CH3	PTA1	LPUART0_RTS	**TRGMUX_OUT0**	-
79	50	38	PTA0	ACMP0_IN0/ TSI1_CH2	PTA0	LPUART0_CTS	**TRGMUX_OUT3**	-
99	-	-	PTA9	-	PTA9	-	*TRGMUX_OUT1*[1]	-
100	-	-	PTA8	-	PTA8	-	*TRGMUX_OUT0*[1]	-

1. The KE17Z has six `TRGMUX_OUT` pins more than the KE15Z.

NOTE

The functions listed in Table 22 are as follows:

- The function in "**Bold**" text is common to the two chips.
- The function in "*italic*" text is unique to the current chip.

The TRGMUX module of the KE15Z has eight external input pins and eight `TRGMUX_OUT` pins. The KE17Z has six `TRGMUX_OUT` pins more than the KE15Z, see Table 22.

5.11 Real Time Clock (RTC)

The KE17Z does not have an RTC module, so it cannot be used as a wake-up source in `Stop/VLPS` mode.

6 System

This section compares the differences between KE15Z256 and KE17Z256 at the system level.

6.1 Reset and boot

The KE17Z only supports booting from flash, not from ROM. Therefore, the definition of Flash Option Register (FTFA_FOPT) is different. For the definition of FTFA_FOPT of the KE17Z, see Table 23.

Table 23. Flash option register (FTFA_FOPT) definition

Bit	Field	Value	Definition
7	Reserved	Reserved for future expansion	
6	Reserved	Reserved for future expansion	
5-4	Reserved	Reserved for future expansion	
3	RESET_PIN_CFG	Enables/disables control for the RESET pin.	
		0	RESET_b pin is disabled following a POR and cannot be enabled as reset function. When this option is selected, there could be a short period of contention during a POR ramp where the device drives the pin low prior to establishing the setting of this option and releasing the reset function on the pin. When the RESET pin is disabled and configured as a GPIO output, it operates as a pseudo open-drain output. This bit is preserved through system resets and low-power modes. When RESET b pin function is disabled, it cannot be used as a source for low-power mode wake-up. **NOTE** When the reset pin has been disabled and security has been enabled by means of the FSEC register, a mass erase can be performed only by setting both the Mass Erase and System Reset Request fields in the MOM-AP register.
		1	RESET_b pin is dedicated. The port is configured with pullup enabled, open-drain, passive filter enable.
2	NMI_DIS	Enables/disables control for the NMI function.	
		0	NMI interrupts are always blocked. The associated pin continues to default to NMI_b pin controls with internal pullup enabled. When NMl_b pin function is disabled, it cannot be used as a source for low-power mode wake-up. If the NMI function is not required, either for an interrupt or wake-up source, it is recommended that the NMI function be disabled by clearing NMI_DIS.
		1	NMI_b pin/interrupts reset default to enabled.
1	Reserved	Reserved for future expansion	
0	LPBOOT	Controls the reset value of clock divider of IRC48M to feed the core clock. Larger divide value selections produce lower average power consumption during POR and reset sequencing and after reset exit. The recovery times are also extended.	
		0	Low-power boot: Core and system clock divider (DIVCORE) is 0x1 (divide by 2).
		1	Normal boot: Core and system clock divider (DIVCORE) is 0x0 (divide by 1).

In the KE15Z;

- bit-1, of FTFA is `BOOTPIN_OPT`
- bit-6, and bit-7 is `BOOTSRC_SEL`

But these bits are not used in the KE17Z.

6.2 Memory-Mapped Divide and Square Root (MMDVSQ)

There is no MMDVSQ module in the KE17Z, so it does not support hardware integer division operations, including 32/32 signed (SDIV) and unsigned (UDIV) calculations.

6.3 Bit Manipulation Engine (BME)

The KE17Z has no BME module.

7 Software

The first few sections of this application note have compared the differences in KE17Z and KE15Z system resources in detail. This section introduces how to quickly port applications from the KE15Z platform to the KE17Z platform with the software aspect.

7.1 SDK driver

Since the KE17Z does not have RTC, PDB, and MMDVSQ modules, the KE17Z SDK does not provide driver files for these modules.

7.1.1 Start_up file

Compared with KE15Z, KE17Z lacks some peripheral modules, so their interrupt vector table is different, see Table 24.

Table 24. Interrupt vector table comparison

Address	Vector	IRQ	NVIC IPR register number	KE15Z source module	KE17Z source module
Arm core system handler vectors					
0x0000_0000	0	-	-	CSTACK	CSTACK
0x0000_0004	1	-	-	Reset_Handler	Reset_Handler
0x0000_0008	2	-	-	NMI	NMI
0x0000_000C	3	-	-	Hardfault	Hardfault
0x0000_0010	4	-	-	-	-
0x0000_0014	5	-	-	-	-
0x0000_0018	6	-	-	-	-
0x0000_001C	7	-	-	-	-
0x0000_0020	8	-	-	-	-
0x0000_0024	9	-	-	-	-

Table continues on the next page...

Table 24. Interrupt vector table comparison (continued)

Address	Vector	IRQ	NVIC IPR register number	KE15Z source module	KE17Z source module
0x0000_0028	10	-	-	-	-
0x0000_002C	11	-	-	SVCall	SVCall
0x0000_0030	12	-	-	-	-
0x0000_0034	13	-	-	-	-
0x0000_0038	14	-	-	PendSV	PendSV
0x0000_003C	15	-	-	Systick	Systick
Non-core on platform vectors					
0x0000_0040	16	0	0	DMA_04	DMA_04
0x0000_0044	17	1	0	DMA_15	DMA_15
0x0000_0048	18	2	0	DMA_26	DMA_26
0x0000_004C	19	3	0	DMA_37	DMA_37
0x0000_0050	20	4	1	DMA_Error	DMA_Error
OFF platform IRQ vectors					
0x0000_0054	21	5	1	Flash Memory	Flash Memory
0x0000_0058	22	6	1	PMC	PMC
0x0000_005C	23	7	1	PORTAE	PORTAE
0x0000_0060	24	8	2	LPI2C0	LPI2C0
0x0000_0064	25	-	-	LPI2C1	-
0x0000_0068	26	10	2	LPSPI0	LPSPI0
0x0000_006C	27	-	-	LPSPI1	-
0x0000_0070	28	12	3	LPUART0	LPUART0
0x0000_0074	29	13	3	LPUART1	LPUART1
0x0000_0078	30	14	3	LPUART2	LPUART2
0x0000_007C	31	15	3	ADC0	ADC0

Table continues on the next page...

Table 24. Interrupt vector table comparison (continued)

Address	Vector	IRQ	NVIC IPR register number	KE15Z source module	KE17Z source module
0x0000_0080	32	16	4	CMP0	CMP0
0x0000_0084	33	17	4	FTM0	FTM0
0x0000_0088	34	18	4	FTM1	FTM1
0x0000_008C	35	19	4	FTM2	FTM2
0x0000_0090	36	-	-	RTC	—
0x0000_0094	37	-	-	CMP1	—
0x0000_0098	38	22	5	LPIT	LPIT
0x0000_009C	39	23	5	FlexIO	FlexIO
0x0000_00A0	40	24	6	TSI	TSI0
0x0000_00A4	41	25	6	PDB0	TSI1
0x0000_00A8	42	26	6	PORTBCD	PORTBCD
0x0000_00AC	43	27	6	SCG	SCG
0x0000_00B0	44	28	7	WDOG_EWM	WDOG_EWM
0x0000_00B4	45	29	7	PWT_ LPTMR	PWT_ LPTMR
0x0000_00B8	46	-	-	ADC1	-
0x0000_00BC	47	31	7	RCM	RCM

The interrupt vector table is defined in the startup file (`startup_MKE15Z7.s`), so when migrating from the KE15Z platform to the KE17Z platform, the startup file must be replaced.

7.1.2 Linker file

As detailed in the section SRAM memory, the SRAM sizes of KE15Z and KE17Z are different, so in the linker file, the address range of the usable SRAM is also different. For details, see Table 25 and Table 26.

Table 25. SRAM address range in the linker file of the KE15Z

Define symbol	SRAM address
m_data_start	0x1FFFE000
m_data_end	0x20005FFF

Table 26. SRAM address range in the linker file of the KE17Z

Define symbol	SRAM address
m_data_start	0x1FFFC000
m_data_end	0x20007FFF

Therefore, when porting the code, the linker file of the KE17Z should be used to replace the linker file of the KE15Z.

8 Conclusion

This application note compares the differences in system resources and software between KE15Z and KE17Z. Customers can refer to this document to quickly migrate projects from KE15Z to KE17Z.

9 References

- *Kinetis KE17Z/13Z/12Z with up to 256 KB Flash Reference Manual* (document KE1xZP100M72SF1RM)
- *Kinetis KE1xZ256 Sub-Family Reference Manual* (document KE1xZP100M72SF0RM)

10 Revision history

Table 27 summarizes the changes done to this document since the initial release.

Table 27. Revision number

Revision number	Date	Substantive changes
0	02 November 2021	Initial release

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