AN13421

BTS6303U Evaluation Board Application Note

Rev. 2.2 — 15 April 2024 **Application note**

1 Introduction

This application note focuses on the BTS6303U evaluation board, the application diagram, board layout, bill of materials and control signals are described. Also some typical measurement graphs are shown, even under Digital Pre-Distortion (DPD) conditions.

Refer to the data sheet for the detailed RF performance of the BTS6303U.

The Customer Evaluation Kit contains the following items:

- BTS6303U EVB
- 5 samples

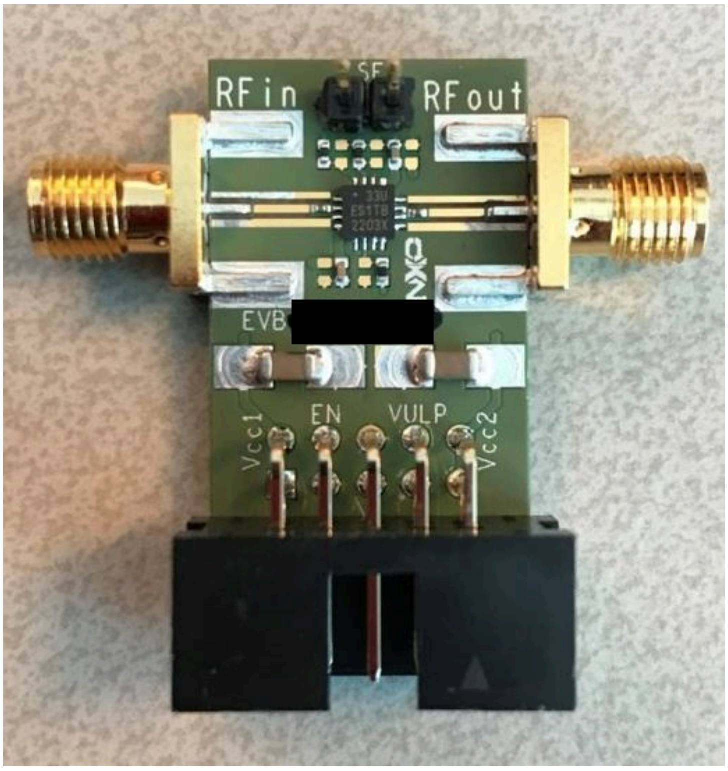

Figure 1. BTS6303U customer evaluation board (EVB)

2 Ordering information

Table 1. Ordering information

Description	Part name	Ordering 12NC
BTS6303U Customer Evaluation Kit	OM17097/BTS6303U	9354 239 88598

3 Product description

The BTS6303U is a wideband, high linearity, pre-driver amplifier for 5G massive MIMO infrastructure applications, with fast on-off switching to support TDD systems. The amplifier is designed to operate between 2.3 GHz and 4.2 GHz. It is housed in a 3 mm x 3 mm x 0.85 mm 16-terminal HVQFN package. The amplifier is ESD protected on all terminals.

- High saturated output power $P_{o(sat)}$ = 28 dBm, at 3.5 GHz
- High power gain G_p = 37 dB
- High linearity performance ACLR = -40 dBc
- Programmable bias current (via external resistor)
- Fast switching to support TDD systems
- 5 V single supply, quiescent current 67 mA
- Small 16-terminal leadless package 3 mm x 3 mm x 0.85 mm
- ESD protection on all terminals
- Moisture sensitivity level 1

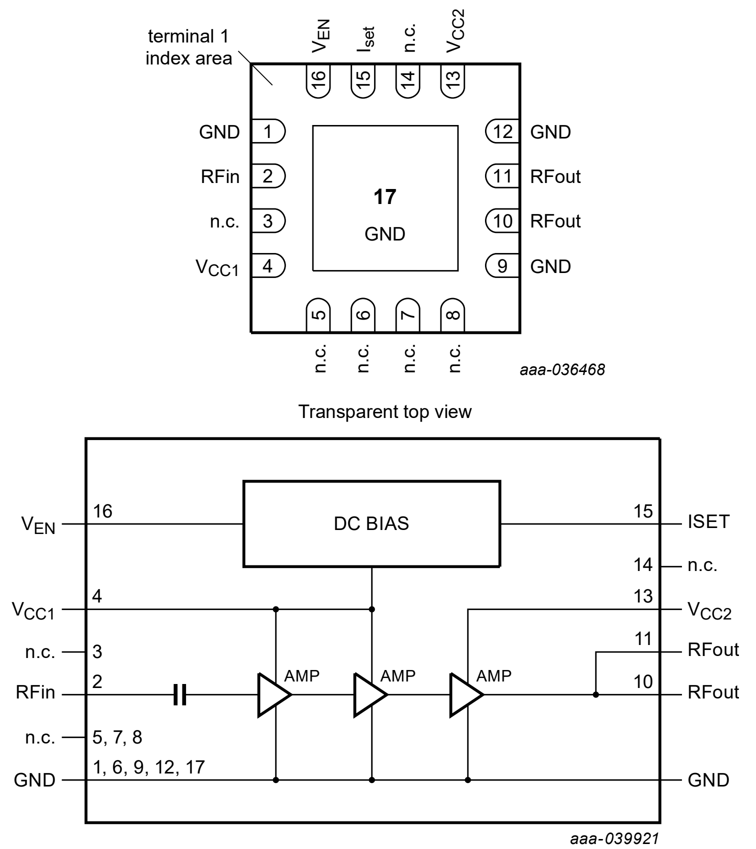

Figure 2. BTS6303U pin diagram and functional diagram

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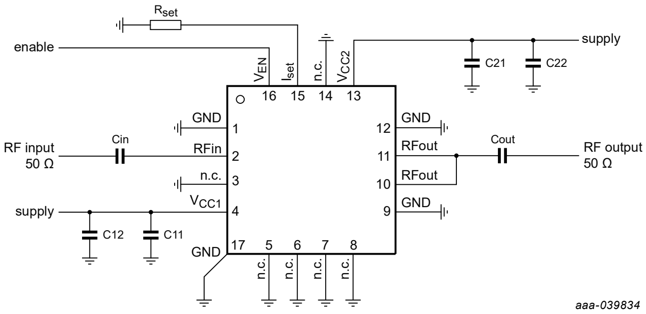
4 Application information



See Table 2 for a list of components.

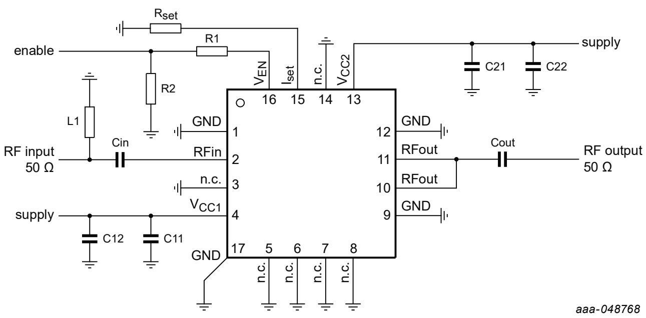
Figure 3. BTS6303U application schematic

Table 2. List of components

See Figure 3 for schematics.

Component	Description	Value	Remarks
C_{in}	capacitor	3.3 pF	for DC blocking / matching, may be tuned
C_{out}	capacitor	18 pF	for DC blocking
C11, and C21	capacitor	10 nF	must be close (< 10 mm) to the IC
C12, and C22 [1]	capacitor	1 μF	must be close (< 10 mm) to the IC
RSET	resistor	10 KΩ	if lower resistor value is applied, a stability check is required

[1] Optional



See Table 3 for a list of components.

Figure 4. BTS6303U alternative application schematic

Note: *pins n.c. (not connected) may be left floating*

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Table 3. List of components
See Figure 4 for schematics.

Component	Description	Value	Remarks
L1	inductor	3.3 nH	for optional matching / filtering
C_{in}	capacitor	3.3 pF	for DC blocking / matching
C_{out}	capacitor	18 pF	for DC blocking
C11, and C21	capacitor	10 nF	must be close (< 10 mm) to the IC
C12, and C22 [1]	capacitor	1 μF	must be close (< 10 mm) to the IC
RSET	resistor	10 KΩ	if lower resistor value is applied, a stability check is required
R1	resistor	5 KΩ	for EN pin protection
R2	resistor	100 KΩ	optional for EN pin protection

[1] Optional

Input component section:

When more gain suppression at low frequencies is required, the components L1/C1 can be applied. These components create a high pass filter.

V_{en} protection:

When there are requirements for maximum currents in the control lines (under all possible conditions), apply a series resistor in the V_{en} line to limit the maximum current. High V_{en} current may happen when V_{CC} is low (or low impedance to GND) and Ven is high (not a normal operating condition).

When a series resistor R1 is placed in the V_{en} line, the maximum current is limited. This series resistor can be necessary when V_{en} is HIGH.

If V_{CC} is low impedance to ground and V_{en} rises above one forward diode voltage (ESD protection diode), the current in the V_{en} line is unlimited.

With given value 5 kΩ, the current at any condition is limited to few mA (depending on V_{en} value). But the switching time is hardly affected.

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5 Evaluation board

The BTS6303U evaluation board simplifies the RF evaluation of this pre driver. The evaluation board enables testing the RF performance of the device, in an isolated environment. To de-embed applied RF output connector and transmission line up to the output DC blocking capacitor, de-embedding data is available on request.

The BTS6303U evaluation board is fabricated on a 26 mm x 48 mm x 1 mm thick 4 layer PCB. The 0.254 mm top layer uses R4350B for optimal RF performance. The board is fully assembled according to the schematic shown below. The board is supplied with two SMA connectors to connect input and output to the RF test equipment.

5.1 Evaluation circuit

The application board circuit diagram that is implemented on the EVB is shown in Figure 5.

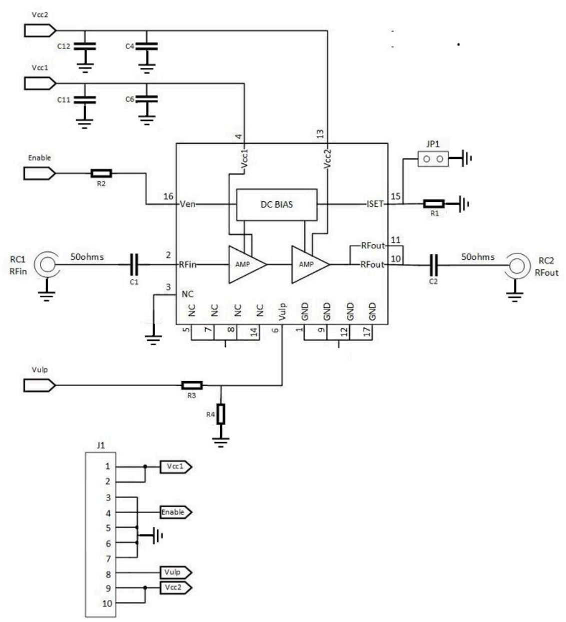

Figure 5. Evaluation board circuit diagram

5.1.1 Explanation of the connections

- V_{CC1}: supply for the first amplifiers stages and biasing / regulator circuitry. Apply at least 10 nF decoupling close to the pin and a larger value capacitor further away (depending on the supply low frequency impedance).
- V_{CC2}: supply for the last amplifier stage. Apply at least 10 nF decoupling close to the pin and a larger value capacitor further away (depending on the supply low frequency impedance).
- I_{set}: used to adjust the quiescent current. The adjustment is inversed proportional to the resistor value. NXP recommends keeping R1 10 kΩ to avoid potential stability issues.
- RFout (two pins): DC coupled RF output (parallel pins), DC blocking capacitor required.
- V_{ulp}: for internal test purposes only, connect to ground.
- RFin: AC coupled RF input, however due to internal ESD protection circuitry the amount of DC allowed to this input is limited. For this NXP recommends applying an additional DC blocking capacitor.

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- V_{en}: logic input. In the NXP EVB a series position, populated with 0 R (zero Ω), is available. When the V_{en} is logic high and V_{CC} is low impedance to ground (none standard "use case") current flows into this V_{en} pin. To limit the current, a 5.6 kΩ resistor can be used in position R2.

5.2 PCB Layout information and component selection

- A good PCB layout is an essential part of an RF circuit design. The evaluation board of the BTS6303U can serve as a guideline for laying out a board using the BTS6303U.
- The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output.
- C6, C11 and C4, C12 decoupling capacitors respectively bypass V_{CC1} and V_{CC2}. C4 and C5 preferably should be located as close as possible < 1 mm to the device, to avoid AC leakage via the bias lines. For long bias lines, it may be necessary to add decoupling capacitors along the line further away from the device.
- In this report, as well as in the data sheet the value of C1 and C2 are stated as 18 pF. The values of C1 and C2 are critical for power on/off settling time. When the value for those capacitors is increased significantly the switching speed is affected.
- Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BTS6303U evaluation board is given in Figure 6

5.2.1 Evaluation board layout

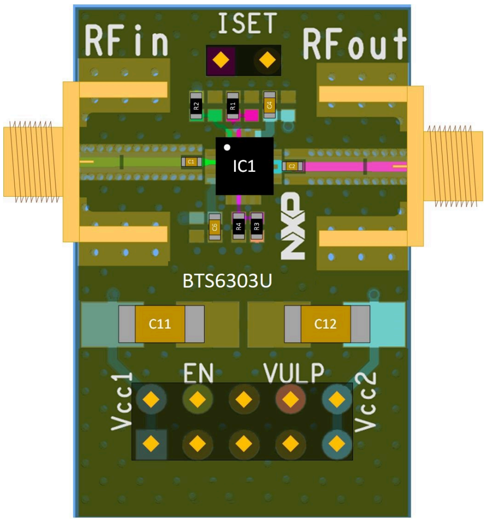

Figure 6. BTS6303U evaluation board layout and component placement

5.2.2 Bill of materials

Table 4. Evaluation board BOM

Gives the bill of materials as is used on the EVB

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
IC1	BTS6303U				
PCB	28x17x1mm				TU-862
C1, and C2	Capacitor	0201	18 pF	Various	DC block
C4, and C6	Capacitor	0402	10 nF	Various	RF decoupling

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Table 4. Evaluation board BOM*...continued*

Gives the bill of materials as is used on the EVB

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
C11, and C12	Capacitor	1206	10 µF	Various	Optional
R1	Resistor	0402	10 kΩ	Various	Quiescent current setting
R2[1], R3, and R4	Resistor	0402	0 Ω	Various	Bridge
RC1, and RC2	SMA RF connector			Johnson, End launch SMA 142-0701-841	RF connections
JP1	Jumper			Molex, PCB header,	
J1	DC header			Molex, PCB header, straight, 2 row 5 way	DC connections

[1] For advice on the value of R2, see the last bullet in section 4.1.1

5.2.3 PCB stack and recommended footprint

The material stack-up used for the pre-driver circuit is a 0.3 mm TU-862 low RF loss layer, merged with a 0.7 mm FR4 layer. See Figure 7. The official drawing of the recommended footprint can be found via following link SOT758-1.pdf. When micro strip coplanar PCB technology is used, it is recommended to use at least 12 ground-vias of 300 µm. These ground-vias are positioned in the ground plane under the device. This technique is also used on the EVBs as shown in Figure 8.

PCB stack and footprint information

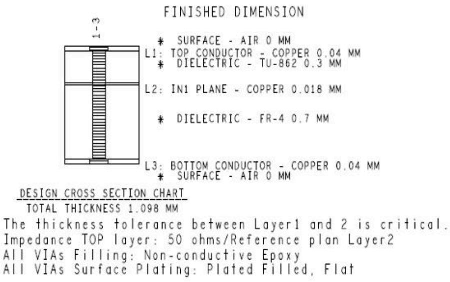

Figure 7. Cross section off the PCB layer stack

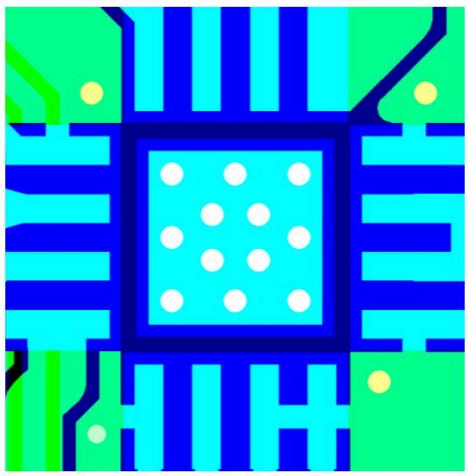

Figure 8. Recommended footprint

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6 Evaluating the BTS6303U

All RF performance results given in the next chapters are referenced to the SMA connectors on the evaluation board. In the data sheet characteristics, board connectors and PCB tracks are de-embedded up-to the product input and output DC blocking capacitors.

The typical device performance given in the data sheet is characterized on the evaluation board equal to the board described in this application note. The BTS6303U mounted on the evaluation board in the customer evaluation kit is industrially tested on the most important RF parameters. Like Gain, Noise Figure, $IP3_o$, and $P_{L(1dB)}$.

All connection names are clearly displayed on the board. See Figure 1.

Note: *Because of the standard layout, the board is used for different products. Not all connections are used, like V_{ULP}.*

6.1 Typical results

For detailed performance of the BTS6303U, we refer to the device product data sheet.

Table 5. Typical results

Unless otherwise specified, the following settings are used for measurements: f = 3.5 GHz; V_{CC} = 5 V; V_{EN} = 1.8 V; T_{amb} = 25 °C; input 100 Ω, and output 50 Ω.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	supply current	ON state, P_o = 15 dBm	-	94	116	mA
		ON state, quiescent	-	67	87	mA
		OFF state	-	1	-	mA
G_p	power gain	ON state, t_{amb} = -40 °C to 115 °C [1]				
		f = 2.6 GHz	36	37.3	37.7	dB
		f = 3.5 GHz	36.5	37.8	38.4	dB
		f = 4.2 GHz	34.3	35.7	36.1	dB
		OFF state	-	-50	-	dB
$P_{L(1dB)}$	output power at1 dB gain compression	f = 2.6 GHz	26.3	26.8	-	dBm
		f = 3.5 GHz	26.4	27	-	dBm
		f = 4.2 GHz	25.3	25.8	-	dBm
$IP3_o$	output third-order intercept point	2-tone; tone spacing = 100 MHz; P_o = 15 dBm	29	30	-	dBm

[1] These values are guaranteed via final test at t_{amb}

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6.2 Graphs

6.2.1 S-parameters

The measured S-parameters and Rollett stability factor K, are given in the graphs below. For the measurements, a typical BTS6303U EVB is used. All the S-parameter measurements have been carried out using the setup Figure 21.

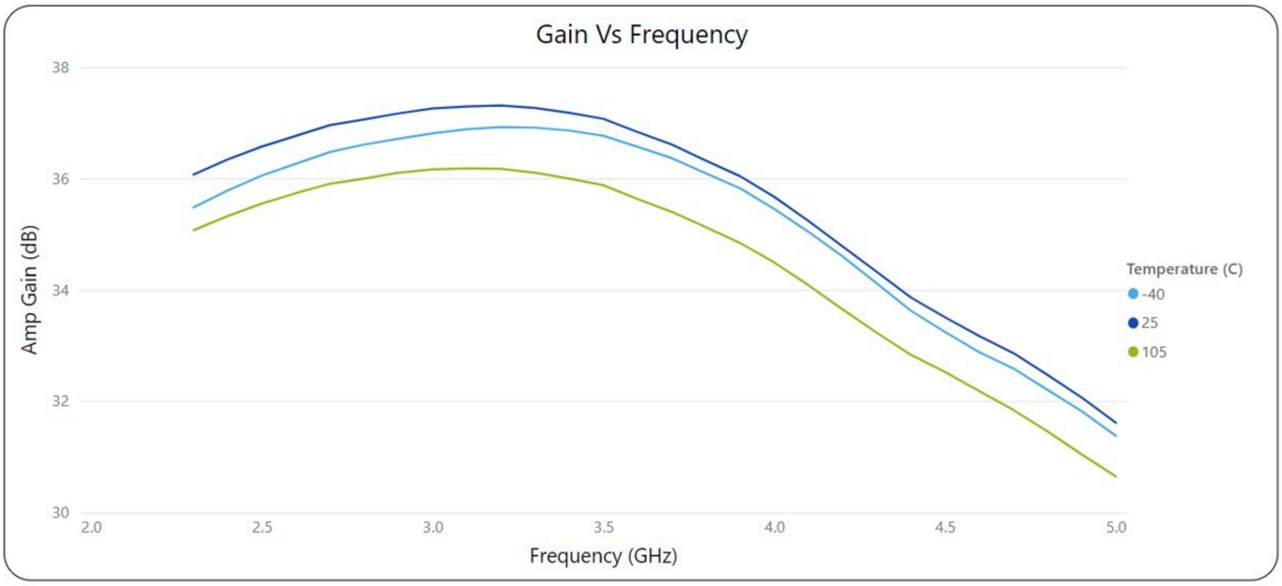

Figure 9. BTS6303U Gain versus frequency over temperature (typical values), V_{CC} = 5 V, P_i = -25 dBm

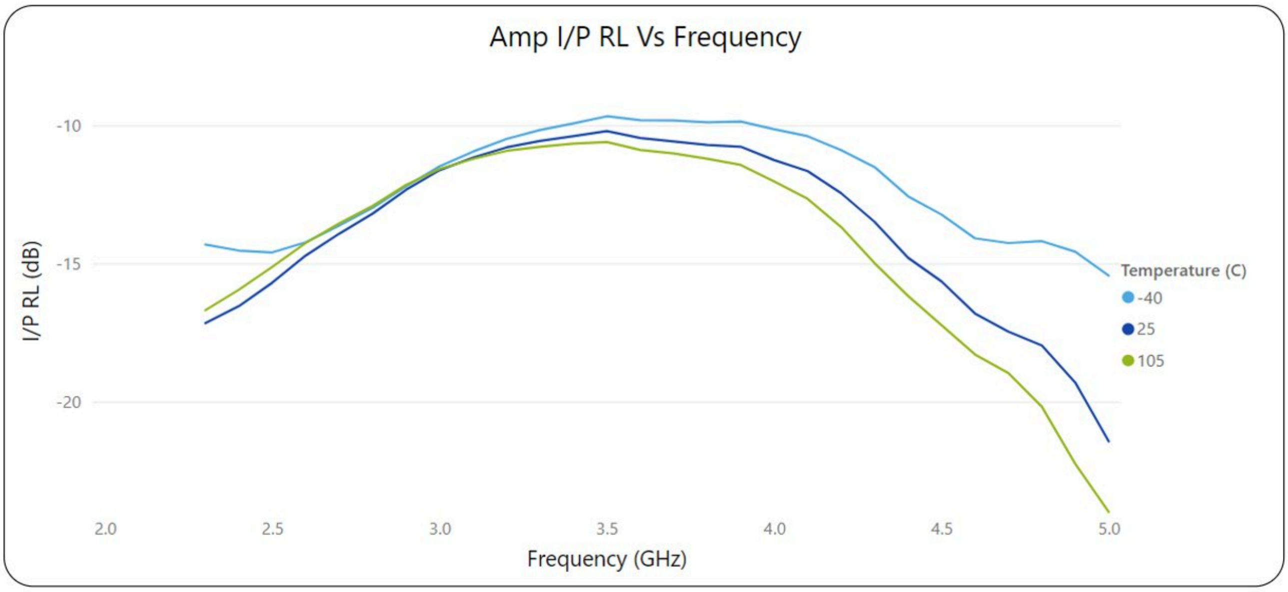

Figure 10. BTS6303U S_{11} versus frequency over temperature (typical values), V_{CC} = 5 V, P_i = -25 dBm

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6.2.1 S-parameters...*continued*

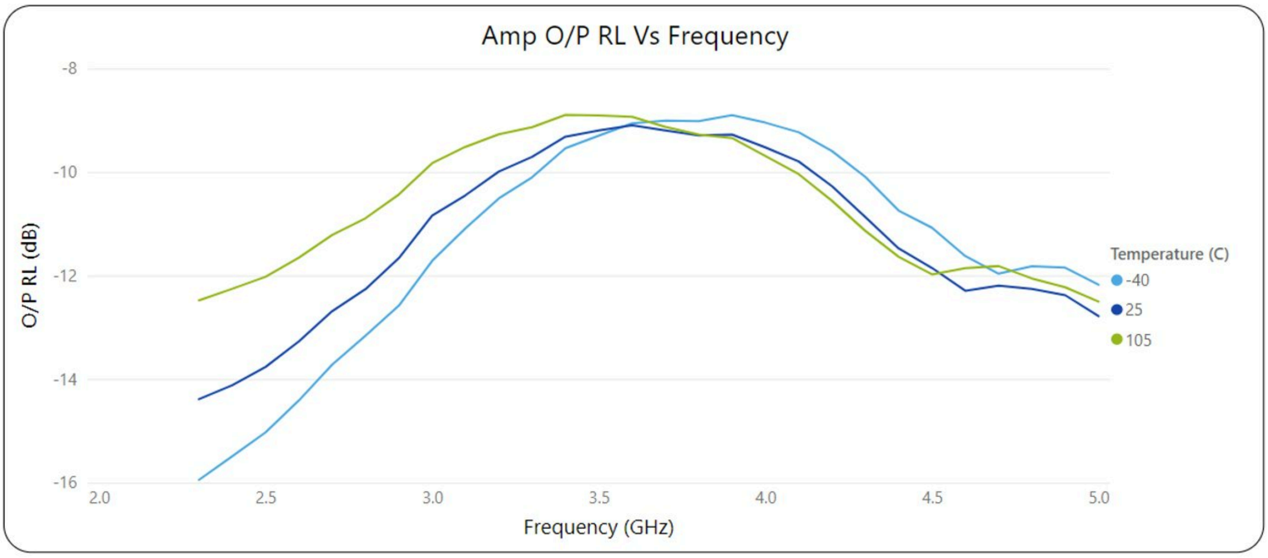

Figure 11. BTS6303U S_{22} versus frequency over temperature (typical values), V_{CC} = 5 V, P_i = -25 dBm

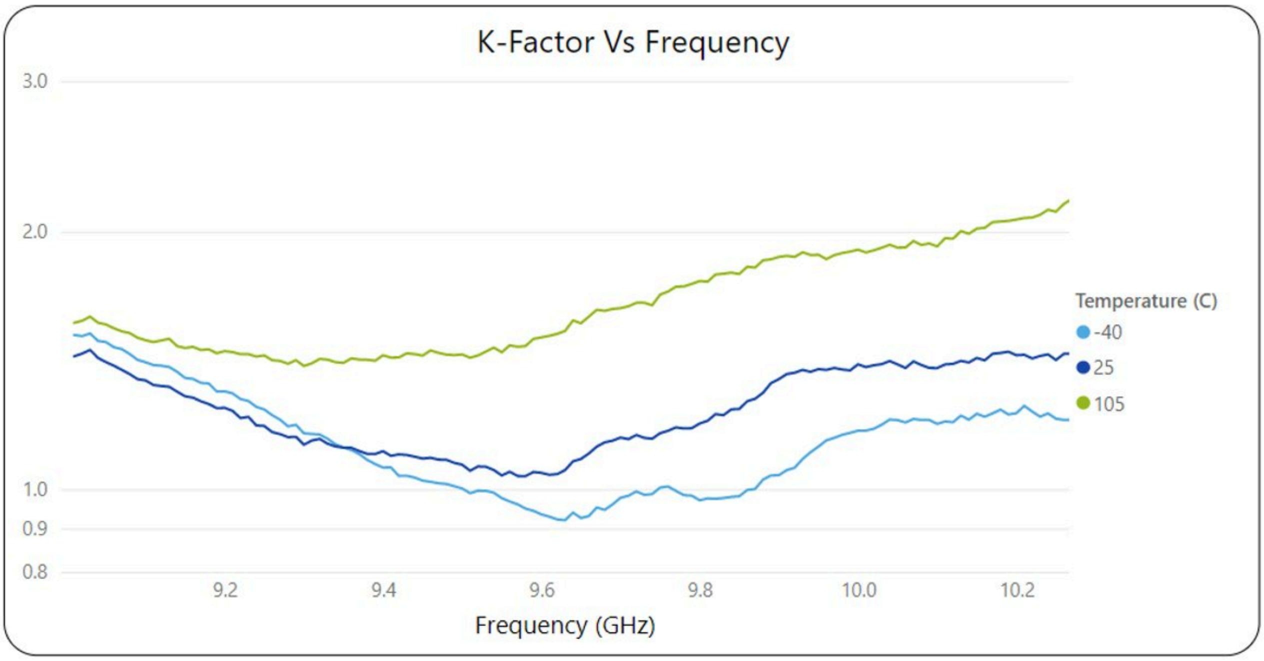

Figure 12. BTS6303U K-factor versus frequency over temperature, V_{CC} = 5 V, P_i = -25 dBm

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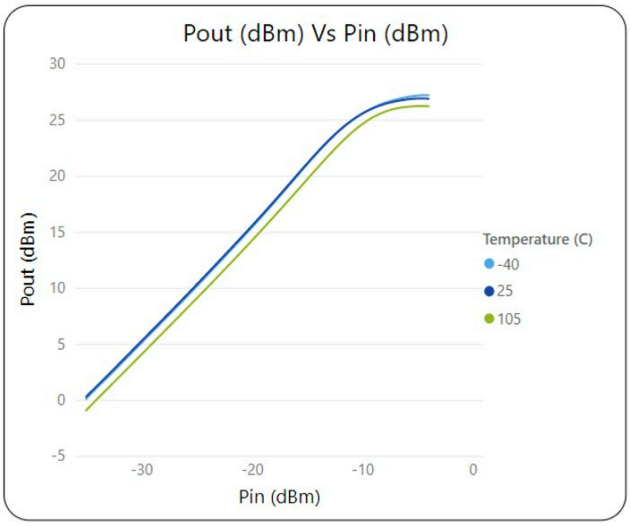
6.2.2 P_o and Gain versus P_i

The P_o and Gain are measured versus P_i using the setup shown in Figure 21.



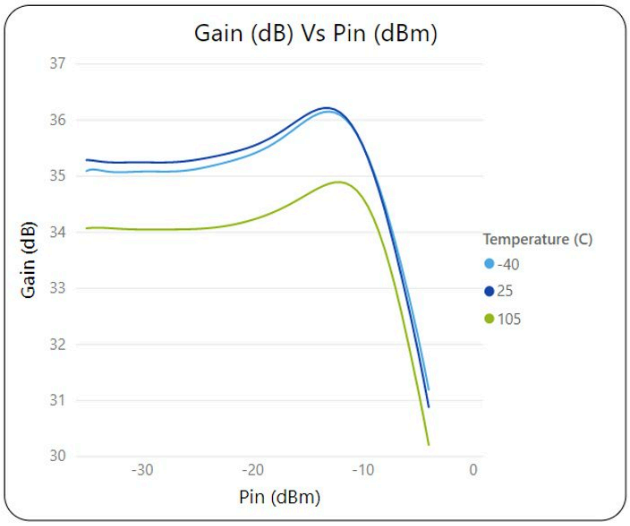


Figure 13. BTS6303U P_o and Gain versus P_i over temperature (typical values), V_{CC} = 5 V

6.2.3 Noise Figure

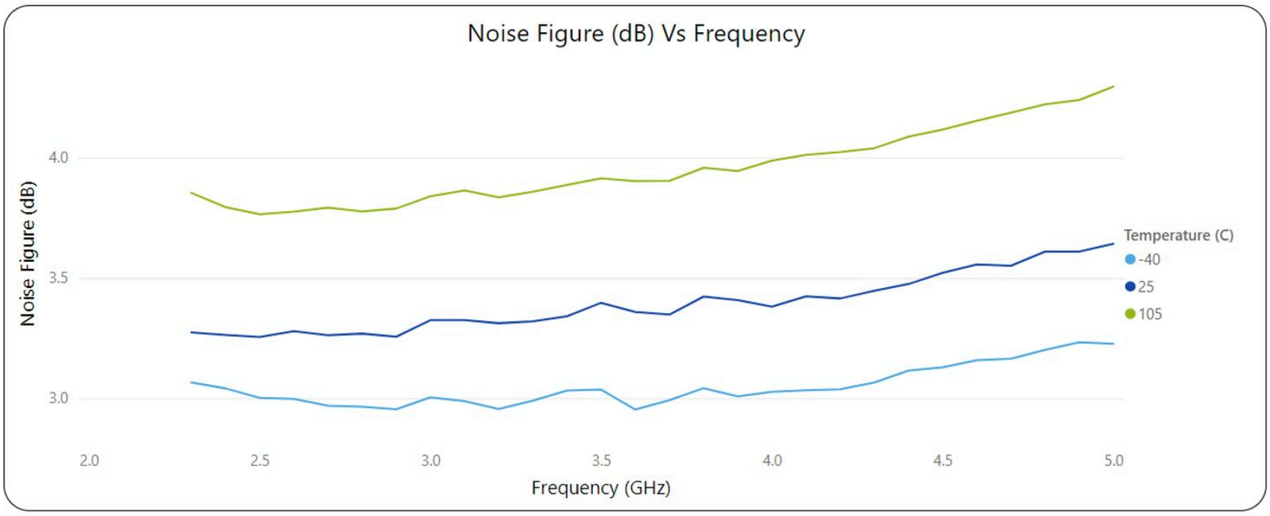


Figure 14. BTS6303U Noise Figure versus frequency over temperature (typical values), V_{CC} = 5 V

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6.2.4 Saturated output power

The saturated output power is measured using the setup shown in Figure 22.

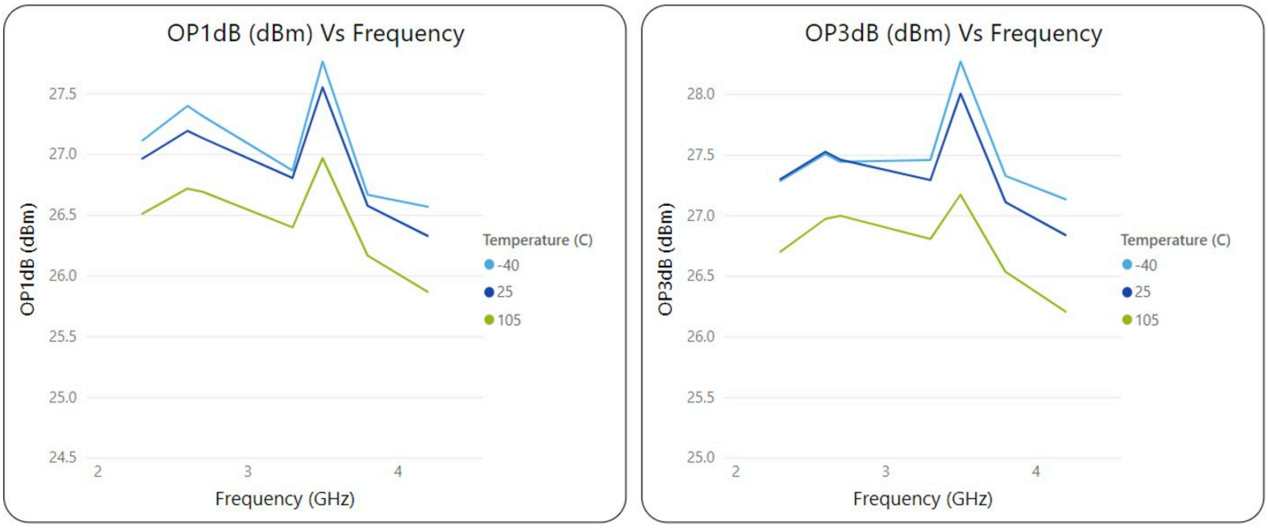

Figure 15. BTS6303U $P_{o(1dB)}$ and $P_{o(3dB)}$ versus frequency over temperature (typical values), V_{CC} = 5 V

6.2.5 Third order intercept point

$IP3_o$is measured using a setup shown in Figure 22.

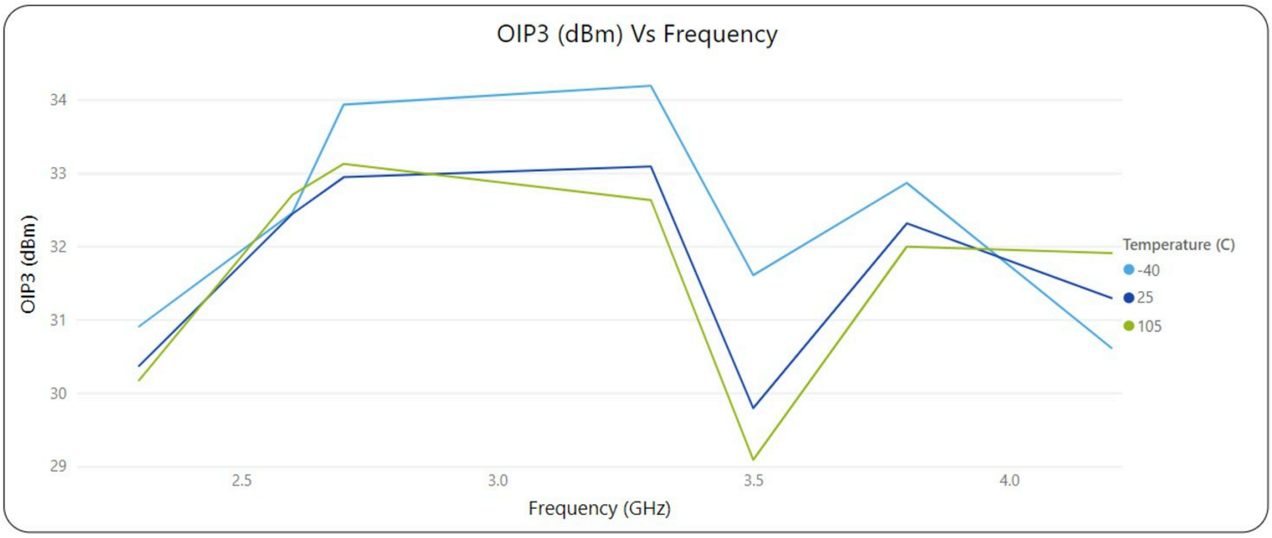

Figure 16. BTS6303U $IP3_o$ at 100 MHz tone spacing versus frequency over temperature (typical values), Tone power 15 dBm

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6.2.6 ACLR under DPD

In the TX line ups for mMIMO, Digital Pre-Distortion (DPD) is applied to linearize the final stages. So efficiency, and linearity-related parameters such as EVM are improved, after DPD is executed.

To what extend the BTS6303U must be predistorted depends on factors like, applied output power, and crest factor at the BTS6303U. As an example, the BTS6303U is measured on ALCR at given Pout with and without applying DPD to note the differences.

DPD engine is 93 coefficients internal developed platform, based on Volterra series.

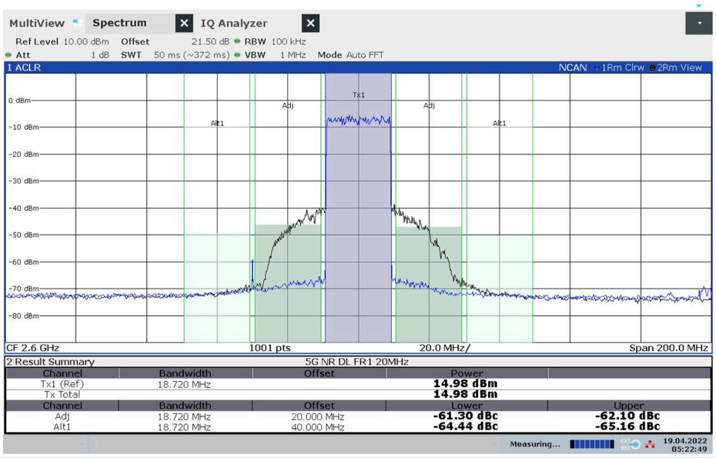

Figure 17. BTS6303U ACLR DPD versus none-DPD at 2.6 GHz center frequency and P_O = 15 dB, CF 11.7 dB

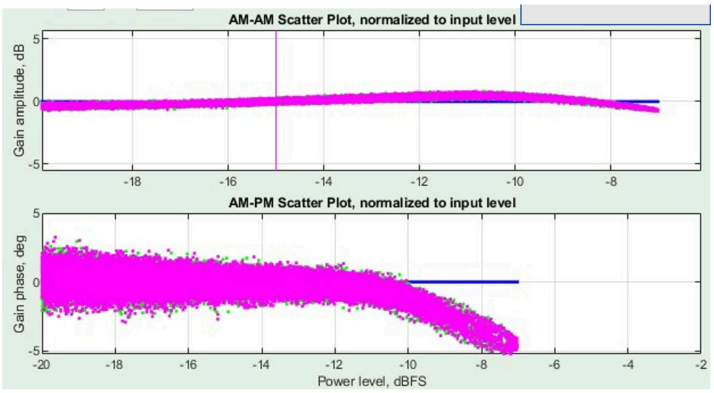

Figure 18. BTS6303U AMAM/AMPM at 2.6 GHz for 28 dBm peak P_O

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6.2.6 ACLR under DPD...*continued*

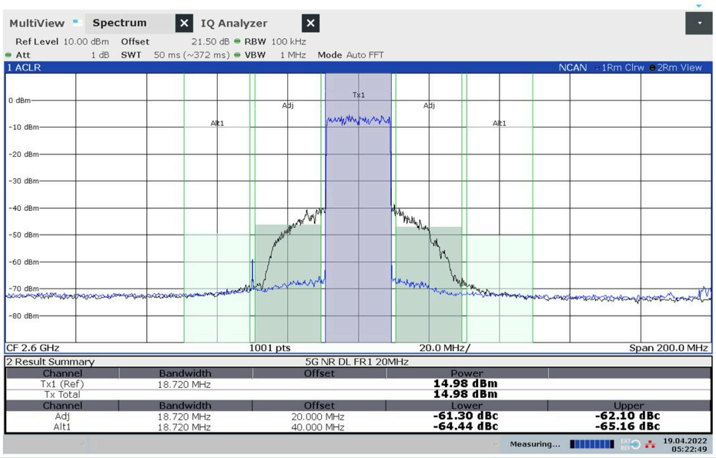

Figure 19. BTS6303U ACLR DPD versus none-DPD at 3.5 GHz center frequency and P_o = 15 dBm, CF 11.7 dB

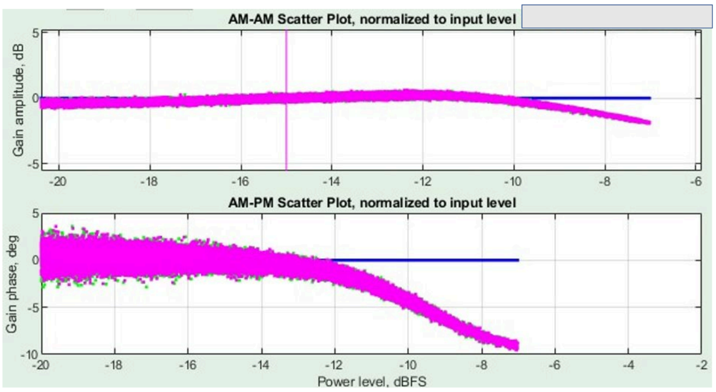

Figure 20. BTS6303U AMAM/AMPM at 3.6 GHz for 28 dBm peak P_o

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6.3 Required Equipment

For the BTS6303U evaluation, the following equipment is needed as a base-line:

- 1 DC power supply 5 V, 200 mA (V_{CC1}, and V_{CC2})
- 1 DC power supply 1.8 V, 5 mA (V_{EN}), or a pulse generator when pulsed measurements are required
- A network analyzer for S-parameter, and P_{1dB} measurements
- 2 RF generators up to 12 GHz plus a combiner for IP3 measurements
- A spectrum analyzer with NF option for IP3 and Noise figure measurements
- High Quality RF cables with SMA/3.5 mm RF connectors
- DC currents meters.

V_{CC1} and V_{CC2} can be combined and fed to the 5 V PSU. After switching on the power supply, the BTS6303U comes up in the quiescent current. 1.8 V_{EN} must be applied.

If necessary, to switch on the power supplies separately the preferable start-up sequence is as follows.

First switch on V_{CC1} second V_{CC2} and third V_{EN}.

Note: *If you want to switch on V_{CC1}, and V_{CC2} separately you need an extra 5 V, 200 mA power supply.*

The typical current at 5 V supply is 70 mA, in power down-mode V_{EN}(0 V), 0.5 mA.

6.4 Connection and setup

1. Connect the EVB to a calibrated network analyzer see Figure 21, we advise the following settings for S-parameter measurements:
    a. Port power -25 dBm
    b. IF Bandwidth 100 Hz
2. The network analyzer can also be used for the 1 dB gain compression evaluation, for this evaluation we advise the following NWA setting
    a. Port 1 power sweep -30 dBm up to -10 dBm
    b. Port 2 20 dB attenuation on the receiver port b2.
    c. IF Bandwidth 100 Hz.
3. Gain and P_{1dB} gain compression data can also be determined using an RF generator and spectrum analyzer.
4. Turn on the DC power supplies and it should read typical I_{cc} = ? mA.
5. Nonlinear distortion measurements IP3 can be performed with a set-up like is depicted in Figure 22. The following settings are recommended to perform the IP3 evaluation.
    a. -25 dBm for each fundamental tone.
    b. RBW and VBW of the spectrum analyzer 100 Hz
    c. Tone spacing 100 MHz

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Table 6. Evaluation measurement setups

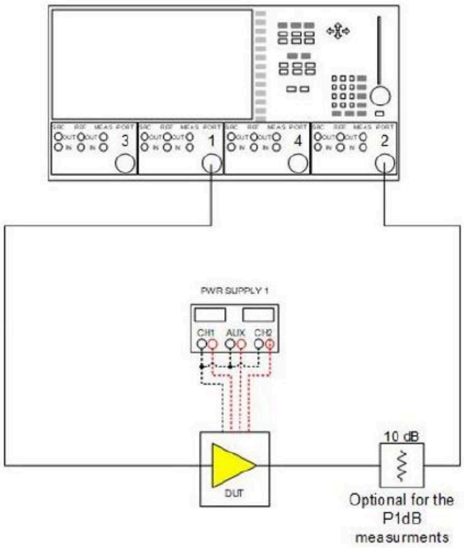

Figure 21. S-parameter and P_{1dB} gain compression setup

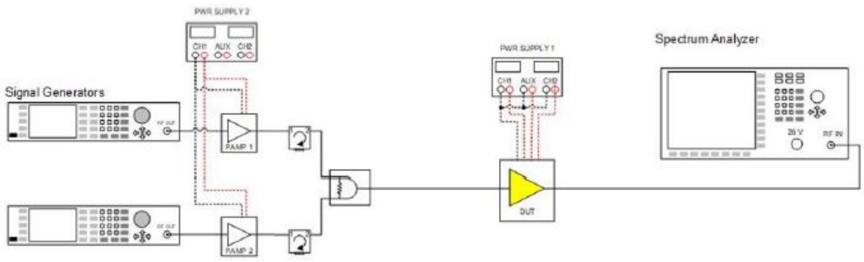

Figure 22. Third order intercept point measurement setup

7 EMC information

CAUTION

This product has not undergone formal EMC assessment. It is the responsibility of the user to ensure that any finished assembly complies with applicable regulations on EMC interference. EMC testing, and other testing requirements for CE is the responsibility of the user.

8 Revision history

Table 7. Revision history

Document ID	Release date	Description
AN13421 Rev. 2.2	15 April 2024	• Updated Legal information and brought to current standard
AN13421 Rev. 2.1	7 December 2022	• Added EMC information
AN13421 Rev. 2	21 October 2022	• Added alternative application information
AN13421 Rev. 1	2 September 2022	• Initial release of application note

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