NXP Semiconductors
Application Notes

Document Number: AN13414
Rev. 0, 10/2021

S32K1 to S32K3 Migration Guidelines

by: NXP Semiconductors

1. Introduction

This application note provides the main differences between the S32K1 and the S32K3 family, and their general considerations when migrating from S32K1 to S32K3. The focus in this document is going to be mostly on S32K3x4 devices (the 4 MB flash devices) this comparison applies to the remaining S32K3 family members (1, 2 and future 8 MB versions) preliminary information is shown for our 8 MB variants and additional details will be shared on a next revision.

For more information contact your Sale/FAE or refer to References.

Contents

2. High level change summary

Taking the S32K1 as a reference, Table 1 shows the high level changes and also shows the features for all K3 family members. This table also includes a difference column to indicate the degree of change.

This "difference" column is classified as the following:

- High: Completely new peripheral / IP block. Might require a significant change in SW.
- Mid: Major changes to an existing IP, impacting SW changes.
- Low: Minor changes to the new IP, minor or no SW changes required.

Table 1 S32K1 and S32K3 family level comparison

	Family name	S32K1	Difference	S32K3
	Safety / ASIL	B	Mid	From B to D
Memory & Security	**P-Flash [MB]**	2 MB	Low	1 to 8
	OTA (A/B swap)	Y (SW)	High	Y (HW)
	D-Flash [kB]	64	Low	64 to128
	EEEPROM [kB]	Max 4 kB (via D-Flash / FlexNVM)	High	SW EEEPROM driver
	Total RAM [kB]	19 to 256	Low	128 to 1152
	Configurable TCM of Total RAM [kB]	N/A	High	96 to 384
	Security solution	CSEc	High	HSE B
Core / Performance	**Core qty**	1xCM0+ (K11x) or 1xCM4F (K14x)	Low	1 x M7 to 3 x M7 (including lockstep configurations)
	Frequency [MHz]	48 / 112	Low	120 to 240
	DMA	4 / 16 ch	Low	12 to 32 ch
	DMIPS	130	NA	256 to 2325
Communication	**CAN FD**	1 to 3	Low	3 to 8
	Ethernet	1x100Mbps (only K148)	Low	1x100Mbps +TSN or 1 Gbps + TSN

	Family name	S32K1	Difference	S32K3
	SAI	0 to 2	Low	0 to 2
	LIN / LPUART	2 to 3	Mid	4 to 16
	SPI	1 to 3	Low	4 to 6
	I2C	1 to 2	Low	2
	I3C	0	High	0 to 1
Extensions	**FlexIO**	8ch	Low	16 to 32ch
	QSPI	1	Low	1
	SDHC	0	High	0 to 1
Analog & Timers	**12-bit ADC**	1 x 13ch to 2 x 32ch	Low	2 or 3 instances each with 24ch
	ACMP (instances)	1	Low	1 to 3
	TRGMUX, ADC cross triggering	Y	High	Y
	Timer modules / channels	2 to 8 modules / 16 to 64 ch.	High	3 modules / 24 to 72ch (only EMIOS but additional timers included)
	RTC	Y	Low	Y
Packaging	**289 MapBGA**	Not available	High	Y
	257 MapBGA	Not available	High	Y
	172 MaxQFP	176 LQFP	High	Y
	100 MaxQFP	100 LQFP	High	Not available for K3x4, but 100 MaxQFP planned for K3x1 and K3x2.
	100 MapBGA	Y	High	
	100 LQFP	Y	High	
	64 LQFP	Y	High	Not present, but 100 MaxQFP having very similar size as 64 LQFP
	48 LQFP	Y	High	Not in K3x4, but considered for K311

In summary:

- Depending on customer's specific use case, approximately 40% of IPs/modules with high reuse vs. 60% new/significantly changed in K3. However, there is extended compatibility through the SW packages delivered to the customer. See Software products available or planned from NXP at the end of this document
- Although there is a heavy reuse between S32K1 to S32K3, there is a medium compatibility between S32K1 and future S32K3 family members.
- Safety and security solutions on S32K1 differ significantly to S32K3 driven by the extended functionality provided by S32K3 with higher safety (ASILD) and security (HSE-B)
- S32K1 and S32K3 packaging is different and will required HW redesign efforts, however, pin placement and signal assignment has been made as similar as possible between platforms. Refer to References section for more information.

3. Platform architecture

The following figure shows the block diagram for S32K14X. Figure 2 shows the block diagram for S32K11X, the Figure 3 shows the block diagram of S32K3X4 and the Figure 4 shows the block diagram of S32K312. The main differences are shown in Table 1.

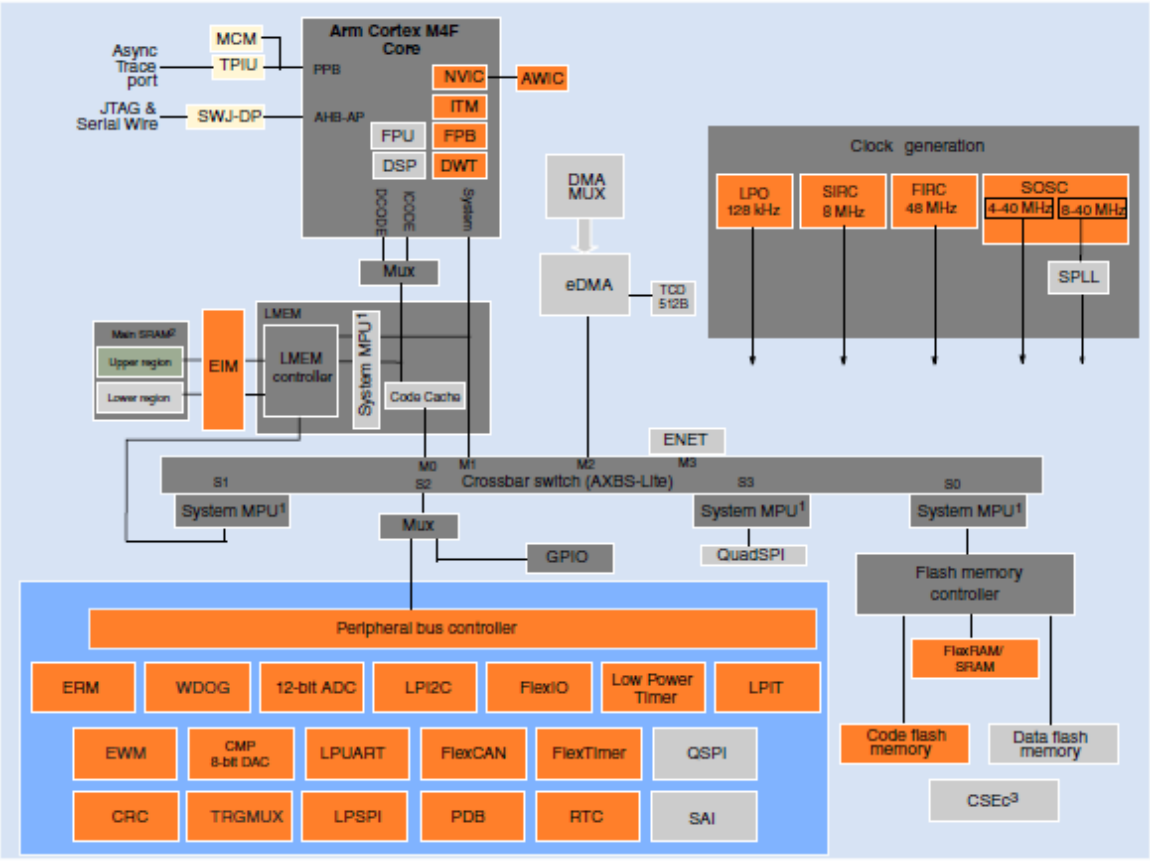


Figure 1. **S32K14X block diagram**

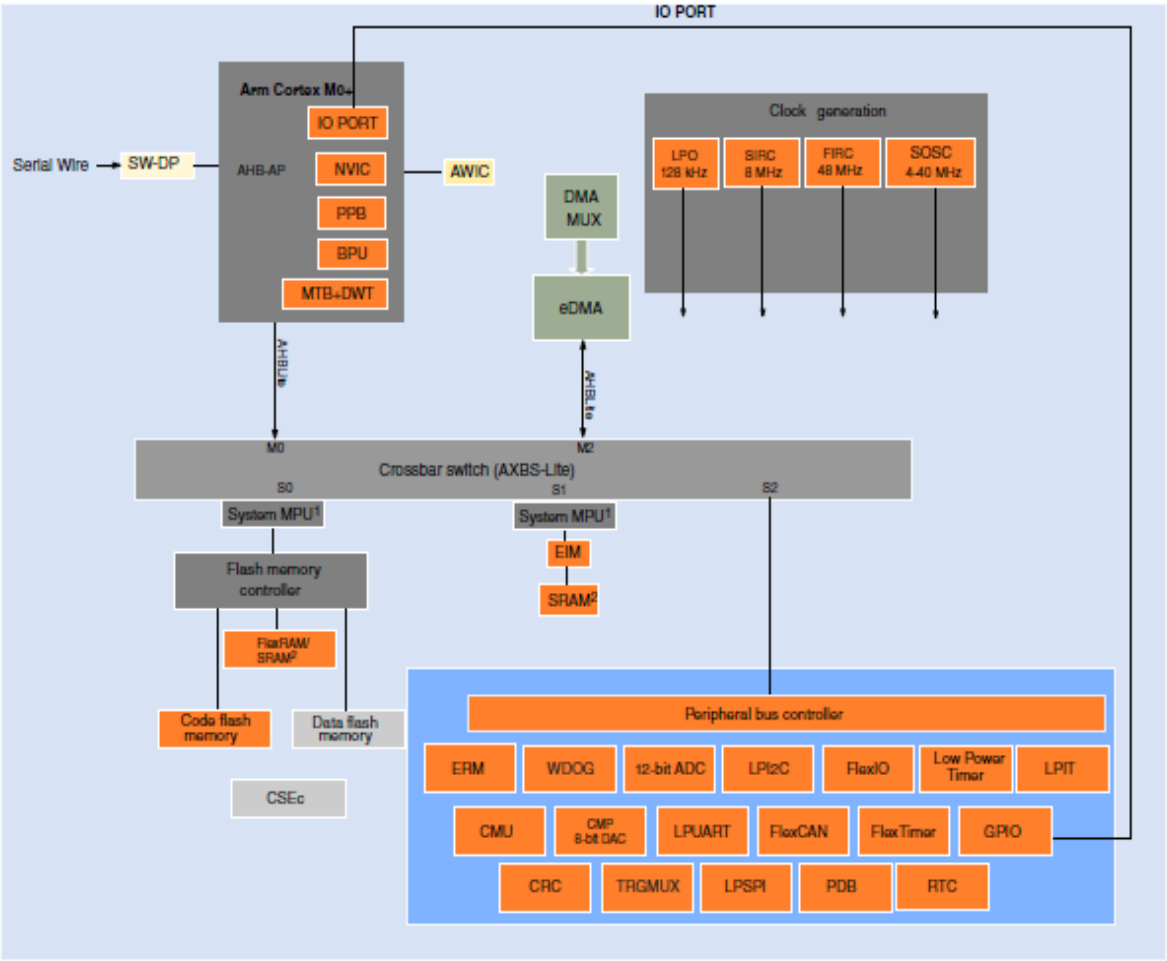


Figure 2. **S32K11X block diagram**

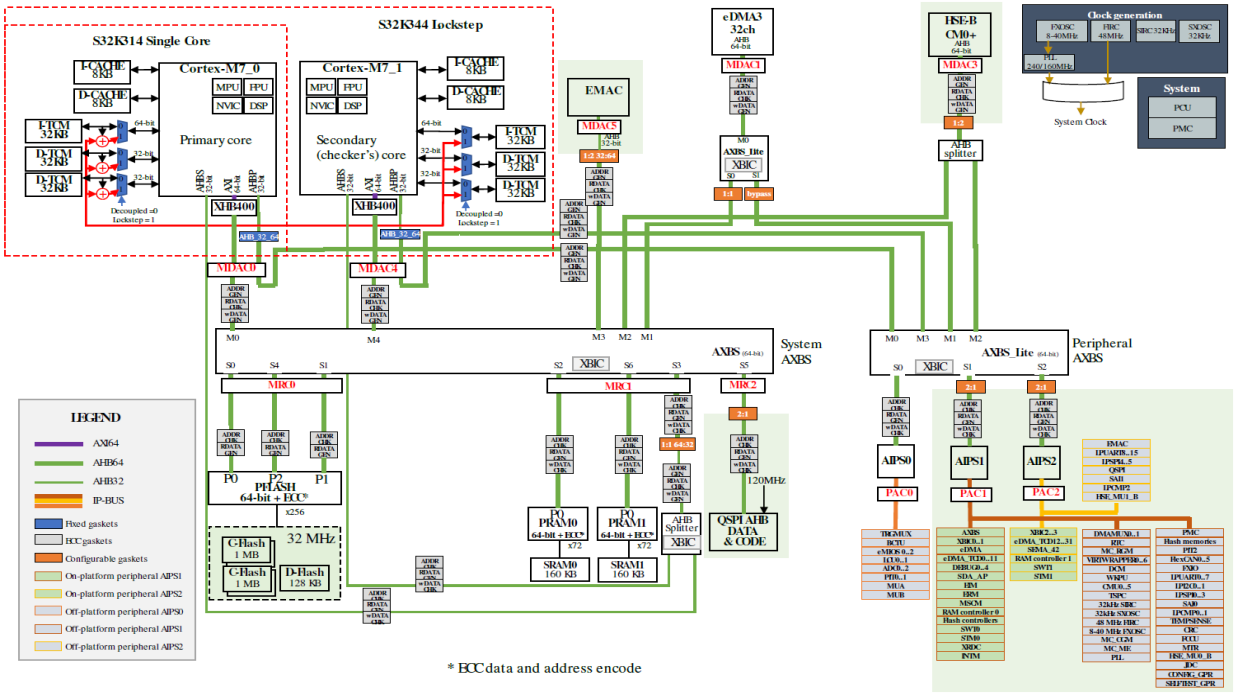


Figure 3. **S32K3x4 platform architecture block diagram**

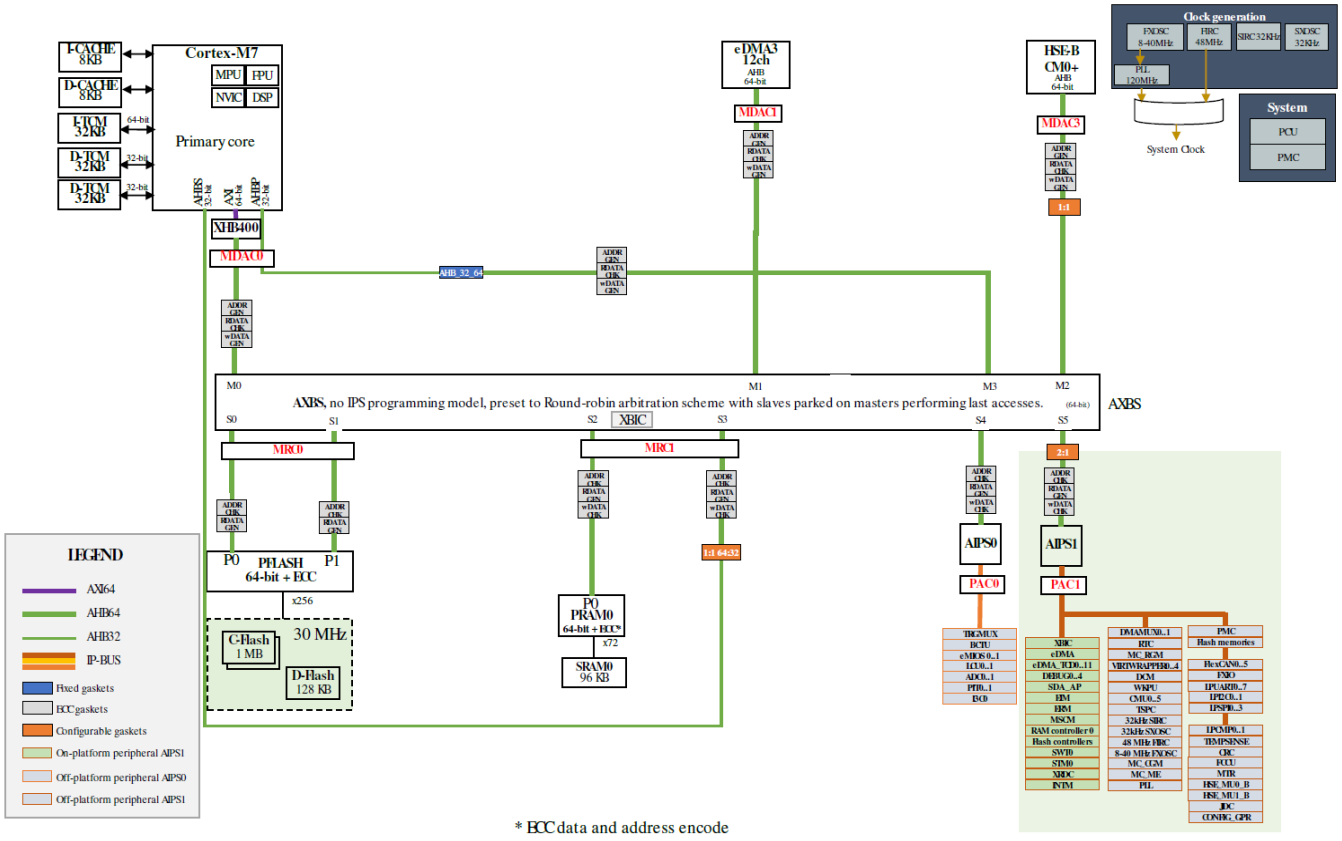


Figure 4. **S32K312 Platform architecture block diagram**

Table 2 Platform differences

Feature	S32K11x	S32K14x	S32K3xx
Cores	ARM Cortex M0+	ARM Cortex M4F	ARM Cortex M7_0/1
TCM support*	No	Yes, all RAM.	Yes
eDMA	Yes		
XBAR	Single	Single	System & Peripheral
Standby RAM	NA**	NA**	32 to 64KB
Message Unit (MU) between application cores	NA	NA	Yes
Hardware Security Engine - HSE (security core)	Custom IP	Custom IP	ARM Cortex CM0+

*TCMs of CM7_1 adds to CM7_0 TCMs in lockstep mode
**Standby RAM is not needed on S32K1XX family because on low power modes, the SRAM retain the information

After a performance comparison, the normalized value for the S32K3 M7 core is 2.4 DMIPS/MHz. The result for S32K14x core is 1.25 DMIPS/MHz. The improvements in the platform are mainly related to the usage of only CM7 cores.

3.1.1. Considerations migrating to K3

For a common application, from a core and platform point of view, there are not many topics to adjust. For K3 additional "tunning" is required if a higher level of performance, including TCM, XBAR and new security features will be leveraged.

4. Memory and OTA

The following table shows an extended comparison between the different memories and their interfaces for S32K1 and S32K3.

Table 3 Memory general differences

Feature	S32K1	S32K3
Program flash memory	Up to 2 MB	Up to 8 MB
FlexMemory	Up to 64 KB Data flash (D-flash)/emulated EEPROM 2 backup (E-Flash) memory: 4 KB additional FlexRAM supporting high-	NA. See Data Flash item

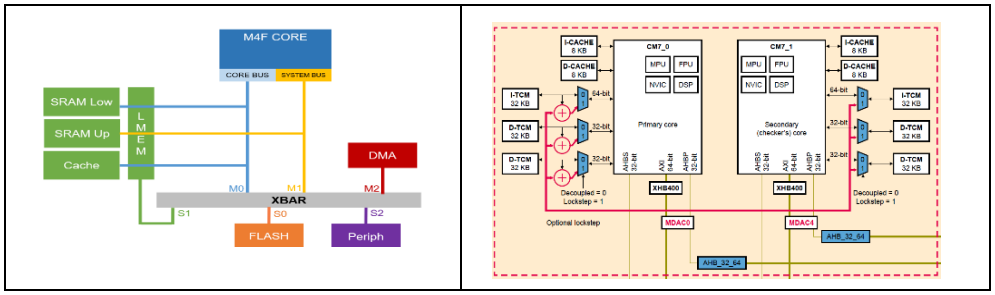
Feature	S32K1	S32K3
	endurance, non-volatile emulated EEPROM	
Data Flash	Up to 64 KB Data flash (D-flash)	Up to 128 KB*
Flash memory controller cache	Yes (single speculative prefetch buffer only)	Up to four pages of data (256-bit page size) may be buffered in each of prefetch buffer for AHP Port0, Port1, and Port2*
Random-access memory (RAM)	Up to 256 KB. 4 KB is part of the EEERAM solution	Up to 1152 KB SRAM (including 384 KB TCM)**
FlexRAM (also available as system RAM)	Up to 4 KB	NA see RAM item
Low-leakage standby memory	RAM retained in all modes	Up to 64 KB with Standby mode retention*
QuadSPI (External Memory interface)	S32K148: Supports SDR and HyperRAM modes up to 4 and 8 bidirectional data lines respectively	1 instance with up to four bidirectional data lines. SDR/DDR HyperRAM feature supported on S32K358. For more detail see QSPI section
Error Correcting Code	YES	YES
Cache	4 KB	Up to 8 KB data and 8 KB instruction cache for each CM7 Core*
EEPROM emulated by FlexRAM	Up to 4 KB (up to 512 KB D-Flash as a part of 2 MB Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash.	By Software

*Subject to change

** SRAM regions are non-cacheable

There are significant changes in memory architecture between S32K1 and S32K3 devices. The following sections describes the most important features and points to consider in detail.

4.1. RAM



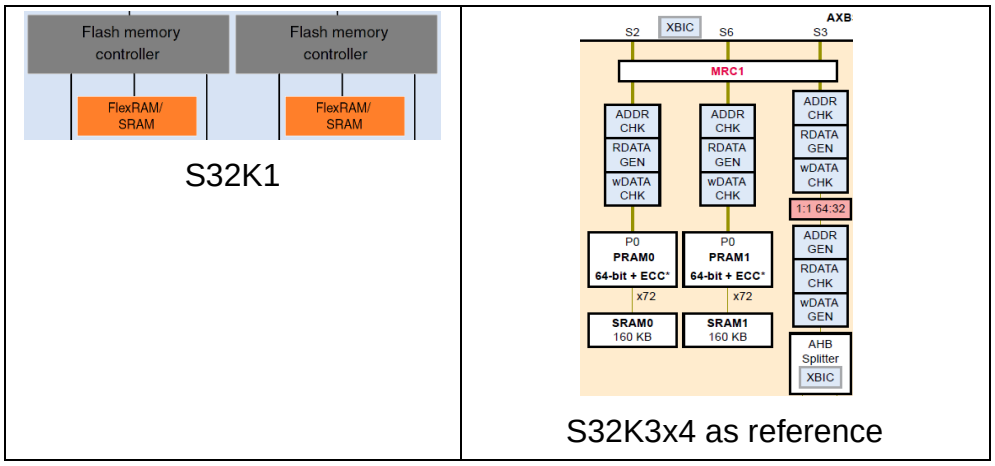


Figure 5. **Flash block diagram example**

On S32K1 RAM is split in two regions SRAM_L and SRAM_U these RAM is tightly coupled with the ARM® Cortex-M4F® and Arm Cortex-M0+® core. The S32K1 has a FlexRAM Memory that can be used as System RAM.

4.1.1. Considerations for migrating to K3

S32K3 RAM is partitioned in TCM Memory and SRAM0 - SRAM1 separated blocks. TCM (Tightly Coupled Memory) is not present in S32K1. TCM has significant application benefit because TCM is a memory accessed by a dedicated connection from the core. In S32K3 each core has a dedicated I-TCM and D-TCM, also in lockstep operation, the checker core's TCM is added to the primary core. TCM can be used as dedicated memories for cores or as a System RAM and have backdoor access for other masters like eDMA or EMAC. For detailed use and function of TCM please refer to S32K3 Reference Manual.

4.2. Flash

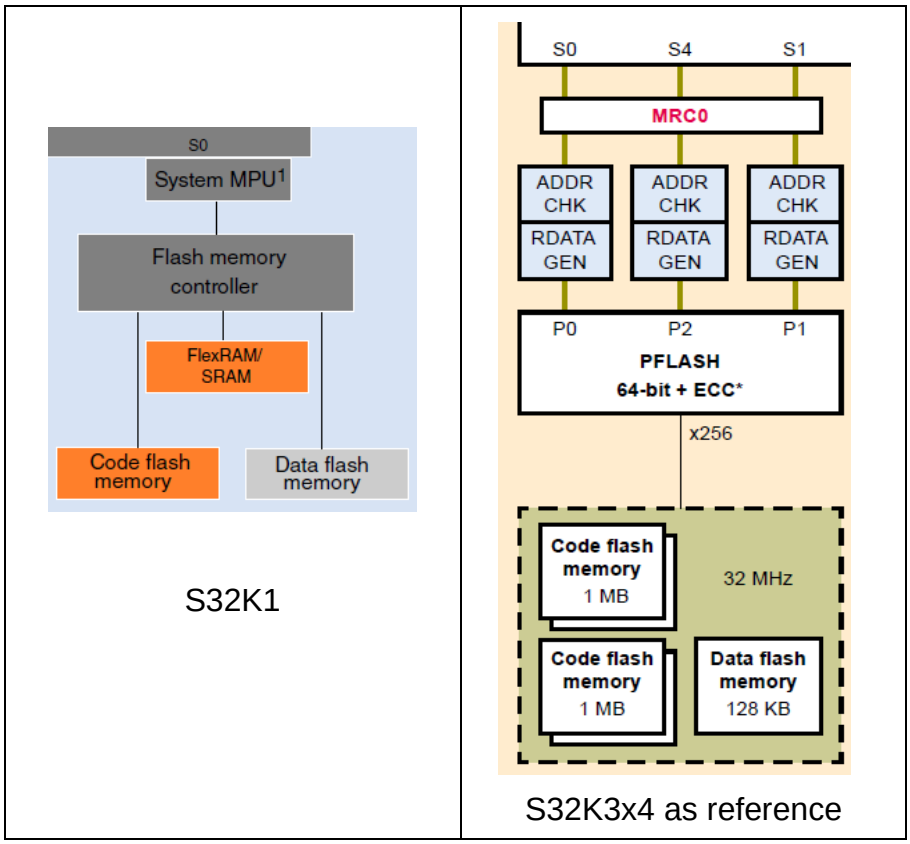


Figure 6. **Flash block difference diagram example**

The Flash memory in S32K1 devices is integrated by a Program Flash Memory and a Flex Memory. The Flex Memory include the FlexNVM and the FlexRAM. FlexNVM can execute program code, store data and functionality as Back up emulated EEPROM data and the FlexRAM can be used as SRAM or as high-endurance emulated EEPROM storage and Accelerates flash-memory programming.

4.2.1. Considerations for migrating to K3

On S32K3 the Flash memory is integrated by blocks, Code Flash 0-3, Data Flash and UTest NVM sector, some blocks are not available for some devices. The maximum number of blocks is five and the minimum is two. Blocks can consist in size from 256 KB up to 2 MB, also some regions are protected for HSE and are not accessible by the application core.

The Flash can do multiple reads in parallel (between different blocks), utilizing the quad read feature. While the embedded flash memory is performing a write (program or erase) to a given partition, it can simultaneously perform a read from any other partition. There are three program interface, Main, Alternate and Express Program to prevent denial-of-service attack.

The UTest Sector is another functionality added to S32K3, this is a dedicated nonvolatile sector with independent programming that can be used to store Test information and supports RWW.

Table 4 EEPROM Emulation Considerations

EEPROM Emulation Considerations	
S32K1	**S32K3**
• S32K1 devices includes Emulated EEPROM by Hardware • EEPROM emulation can be achieved with the Flex Memory configurations. • Flash Module FTFC hardware emulates the characteristics of an EEPROM by effectively providing a RAM buffer (FlexRAM) as virtual EEPROM as an Interface to the user/EEPROM driver. • Data is automatically programmed into the FlexNVM block using a hardware built-in filing system.	• S32K3 has not HW state machine based EEE as S32K1 • S32K3 has 128KB Data Flash Block (an individual RWW) for EEPROM emulation. • Flash blocks can be used as Active blocks to manage and swap records. • To emulate an EEPROM on S32K3 Embedded Flash, can be achieved using software drivers, strategic over-programming of double-words in the flash, some requirements, and best practices in EEPROM software drivers. • Emulation Drivers (RTD), Application notes and example codes will be provided by NXP.

In addition, in the Reference Manual can be found some good practices for the EEPROM Emulation driver. NXP provides FEE driver with the Real Time Driver (RTD) package (Included in the SW32K3_RTD package). For more information refer to AN4868.

NOTE

It is required that the EEPROM emulation driver builds in fault tolerance allowing for the ability to "skip" records. In the case of an unsuccessful program, the ability to retry programming in the next available record location (record retirement). In the case of an unsuccessful sector erase, the ability to retire a sector is required (sector retirement).

4.2.2. S32K1 vs S32K3 reliability and times specifications

Table 5 Endurance and performance

Feature	S32K1	S32K3	Units
Data retention up to 1K cycles	20	20	Years
Cycling endurance	1 K	1 K (1 MB blocks) 100 K (256 and 512 KB blocks)	Cycles
Doble word (64 bits) Program Time	90	102	µs
Page (256 bits) Program time		142	µs
Quad-Page (1024 bits) Program time	5000	314	µs
8 KB Sector Program time		19	ms
8 KB Sector Erase time		4.8	ms

Feature	S32K1	S32K3	Units
256KB Block Erase time	250	22.8	ms
1MB Block Erase time	250 (512 KB flash)	30.6	ms
Erase All Blocks	1400		ms

4.3. OTA

There are some changes between S32K1 and S32K3 devices when implementing OTA. Both devices support this feature but, S32K3 extends the hardware capabilities for OTA enabling the concept of active and passive blocks and read-while-write capability between independent memory blocks. The following table shows main differences in OTA features capabilities.

Table 6 OTA Features

OTA Feature	S32K1	S32K3
A/B Swap	No	Yes
Number of flash partition	Up to 3	Up to 4
Read while write	K146/K148: Yes Other: No	Yes
Power lost verification	Software implemented	Hardware implemented
Image verification	Software implemented, done after boot.	Hardware implemented, done before boot.
Instant switching between firmware	No, software verification required.	Yes, hardware verification implemented.
Flash remapping	No	Yes
Position independent code or linker management required	Yes	No
Lockable flash regions	Yes	Yes
Update while application running	K146/148: Yes Other: No	Yes
Secure boot	Yes	Yes
Backup firmware size	62 kB – 508 kB S32K148: up to 1M 508 kB (using QSPI)	K3x4: 2 MB K3x2: 1 MB K3x1: 512 kB
Application firmware size	62 kB – 508 kB S32K148: up to 1M 508 kB (using QSPI)	K3x4: 2 MB K3x2: 1 MB K3x1: 512 kB

4.3.1. Considerations for migrating to K3

As shown in the above table, K3 offers more functionality within the OTA solution. It includes the introduction to the concepts of active and passive blocks, flash remapping, and A/B swap; these features allow the “Backup firmware” for rollback functionality and “Seamless update” for zero downtime installation. For more details on the OTA implementation, please refer to NXP documentation about this topic.

One of the advantages when using the S32K3 is the hardware implementation of the variety of the functions that are implemented in the S32K1 by software; this eliminates the need of Linker file modification and complex memory spaces tracking.

5. Clocking, Power management, Reset and Boot

5.1. Clocking architecture

In terms of clock sources, S32K3 and S32K1 are quite similar. Ignoring a few punctual differences (regarding some configuration registers and SoC integration aspects) the clock sources comparison is shown in the following table.

Table 7 S32K1 and S32K3 clock sources

S32K1	S32K3	Key comments
Fast IRC 48 MHz	Fast IRC 48 MHz	Default clock source after reset in both architectures. K3: cannot be disabled in RUN mode.
Slow IRC 8 MHz	Slow IRC 32 KHz	K3: can no longer be selected as the system clock.
SOSC (4-40) MHz	FXOSC (8-40) MHz	K3: Two configurable params were added (amplifier transconductance and stabilization counter value). K3: can no longer be selected as the system clock.
LPO 128 KHz	SXOSC (32.768 KHz)	Intended RTC clock source for both architectures. K3: new param added (stabilization counter value). K3: SXOSC does not support trimming (as LPO).
System PLL (90-160) MHz	PLL (48-320) MHz	K3: VCO freq. up to 1280 MHz (K1 up to 320 MHz). K3: Programmable frequency modulation and Lock detection circuitry were added.

When designing with S32K1 family, after selecting the desired system clock source (PLL, FIRC, SIRC, or SOSC) the user must focus on the three main clock nodes - CORE, BUS, and FLASH.

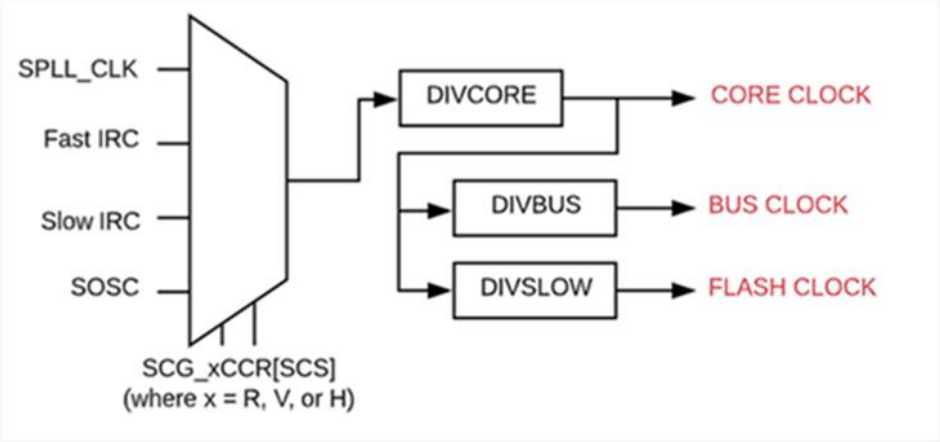


Figure 7. **S32K1 system clocking**

On the other hand, when moving forward with S32K3, there are fewer options to clock the system (PLL or FIRC), but the number of system clock nodes increases.

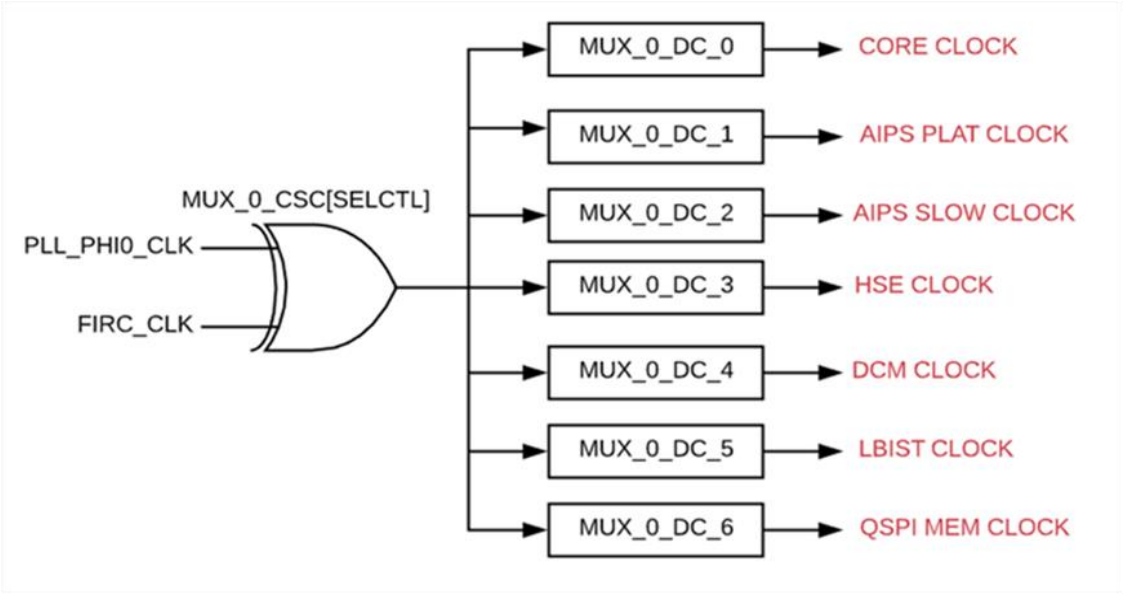


Figure 8. **S32K3 system clocking**

5.1.1. Considerations for migrating to K3

An important point to highlight is how the clocking nodes are distributed to the peripherals within each platform. For S32K1, each clock source has two divided branches, offering eight asynchronous peripheral clock sources for most peripherals.

In the S32K3 architecture, CORE_CLK, AIPS_PLAT_CLK and AIPS_SLOW_CLK nodes feed the SoC modules. Some peripheral clocking examples are compared below. For more detail please refer to the corresponding RM.

Table 8 S32K1 and S32K3 module clocking examples

IP	S32K1	S32K3
FlexCAN Protocol Engine	SOSCDIV2_CLK SYS_CLK	AIPS_PLAT_CLK FXOSC_CLK FIRC_CLK
FTM / EMIOS Counter Clock	SOSCDIV1_CLK SIRCDIV1_CLK FIRC_DIV1_CLK SPLLDIV1_CLK TCLKn (Pad) RTC_CLK SYS_CLK	CORE_CLK
ADC Conversion Clock	SOSCDIV2_CLK SIRCDIV2_CLK FIRCDIV2_CLK SPLLDIV2_CLK	CORE_CLK

Concluding this section, it is worth mentioning a couple of key general differences in the following table.

Table 9 S32K1 and S32K3 clocking features

Feature	S32K1	S32K3
System Clocking settings (multiplexers and dividers) are done by	SCG (System Clock Generator)	MC_CGM (Clock Generation Module)
Peripheral clock gating is performed by	PCC (Peripheral Clock Controller)	MC_ME (Mode Entry Module)
Clock Monitoring Units	S32K11x has 2 instances to monitor clocking operation in safety-relevant applications	Four new instances were introduced (6 in total), and two of them are frequency meters.

CLKOUT pins to view internal clocks are supported in both S32K systems.

5.2. Power management and operating modes

One of the most eye-catching differences in the transition from S32K1 to S32K3 is the number of supported power modes. The implemented power modes in both architectures and their relationship with Cortex M0+, Cortex M4 and Cortex M7 modes are depicted in the following figure.

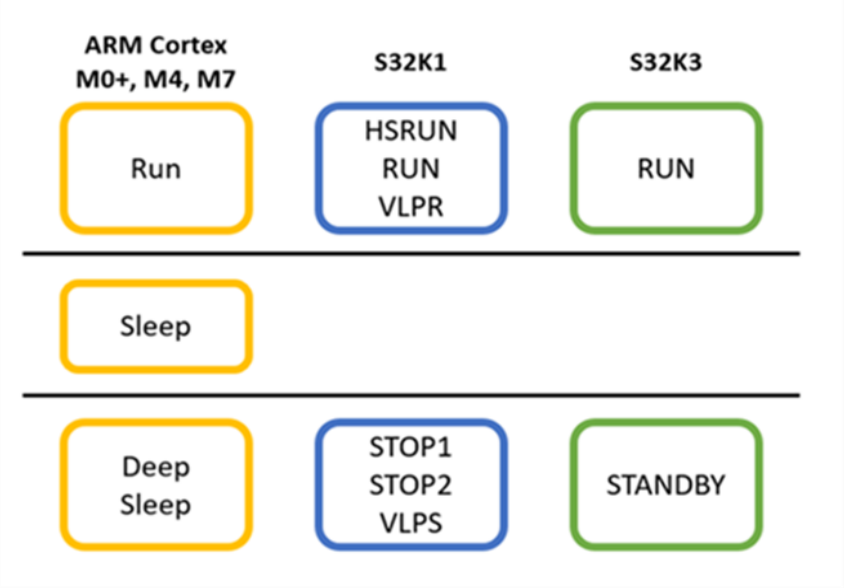


Figure 9. **S32K power modes**

5.2.1. Considerations for migrating to K3

A very important topic to keep in mind when developing low power applications on the S32K3 platform is the behavior of the chip when waking up.

The following figure shows that when S32K1 wakes up from a deep sleep, it enters to VLPR or even RUN mode (without going through a reset event).

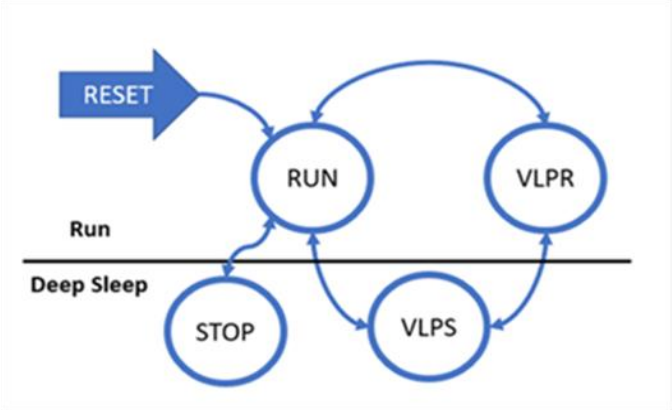


Figure 10. **S32K1 power mode state transition diagram (HSRUN not included)**

This process changes in S32K3 devices. Following diagram shows the high-level standby exit flow, during software development, the user must consider it when the device wakes up, the program will not continue immediately after the WFI instruction as used to be in S32K1.

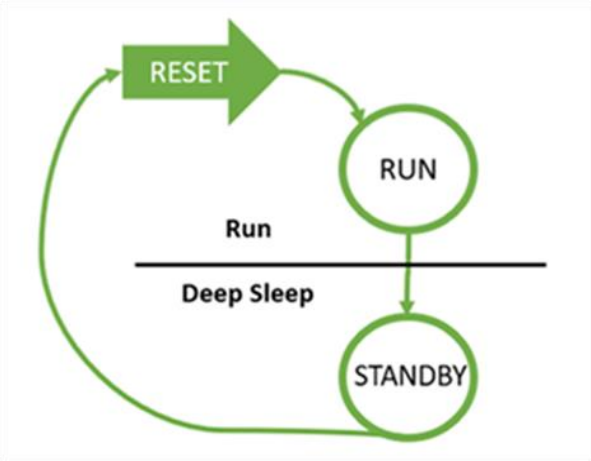


Figure 11. **S32K3 Power mode state transition diagram**

For more details on the reset generated after a wake up event, refer to the Reset and Boot section.

The Cortex M0+, Cortex M4 and Cortex M7 have the Asynchronous Wake-up Interrupt Controller (AWIC). The K3 incorporates the WKPU unit to configure wake-up events. The following shows a comparison of the available wake-up sources.

Table 10 S32K1 and S32K3 wake-up sources

S32K1 - Stop and VLPS	S32K3 - Standby
Available System Resets (RESET_b, POR, JTAG)	
Any enabled pin interrupt	60 GPIO pins
ADCx	Not available in Standby mode

CMP	Analog CMP (round-robin)
LPI2C0 **LPUART** **LPSPI** **LPTMR0**	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
RTC	RTC (API or timeout)
CAN0 (PNET)	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
Non-maskable interrupt (NMI)	Single NMI pin routed to all app cores.
WDOG	SWT0
FlexIO	Not available in Standby mode – Pin wakeup and then peripheral enablement is required
LPIT	RTI event
CRC **SGC**	Not available in Standby mode

NOTE

To compare the current consumption on each chip under a range of temperatures, refer to the S32K Datasheet.

It's time to analyze what modules are available during deep sleep, the below table lists them.

Table 11 S32K1 and S32K3 module operation in low power mode (deep sleep)

Modules	S32K1 STOP	S32K1 VLPS	S32K3 STANDBY
System			
Cores, NVIC	OFF	OFF	OFF
LVD / LVR	Both Active	LVR Active	LVR Active
DMA	Async operation	Async operation	OFF
Watchdog	Async op. (STOP1) FF (STOP2)	Async operation	FF

Modules	S32K1 STOP	S32K1 VLPS	S32K3 STANDBY
Clocks			
LPO / SXOSC	LPO FF	LPO FF	SXOSC FF
PLL	FF	OFF	OFF
SIRC	FF	FF	FF
FIRC	FF	OFF	FF
SOSC / FXOSC	FF	OFF	FF
Communication			
LPUART	Async op. (STOP1) FF (STOP2)	Async operation	OFF
LPSPI	Async op. (STOP1) FF (STOP2)	Async operation	OFF
LPI2C	Async op. (STOP1) FF (STOP2)	Async operation	OFF
FlexIO	Async op. (STOP1) FF (STOP2)	OFF	OFF
CAN	PNET (CAN0)	OFF	OFF
ENET / EMAC	Magic Packet Wakeup	OFF	OFF
QuadSPI	OFF (STOP1) FF (STOP2)	OFF	OFF
SAI	OFF (STOP1) FF (STOP2)	OFF	OFF
Timers			
LPIT / RTI0	Async op. (STOP1) FF (STOP2)	Async operation	FF
LPTMR	Async op. (STOP1) FF (STOP2)	Async operation	Not supported

Modules	S32K1 STOP	S32K1 VLPS	S32K3 STANDBY
RTC	Async op. (STOP1) FF (STOP2)	FF	FF
Safety			
CRC	Available in STOP2	OFF	OFF
Analog			
CMP	Low-speed and High-speed (STOP1) FF (STOP2)	Low-speed compare	FF
ADC	OFF (STOP1) FF (STOP2)	OFF	OFF
Human Machine Interface			
PORT / SIUL2	Async op. (STOP1) FF (STOP2)	OFF	OFF

*FF: Full functionality (SW configurable).

*Async operation: FF with alternate clock source.

5.3. Reset and Boot

In general, there are up to four different types of reset in the S32K family. The following table shows the reset sources. For more specific details, refer to the corresponding RM.

Table 12 S32K1 and S32K3 reset sources

Event Type	S32K1 reset sources	S32K3 reset sources
Power-on Reset (POR)	**Power supply is initially applied**	
	Supply voltage drops below VPOR	Brown-out in any power domain (V11, V25, VDD_HV_A/B) POR Watchdog time-out
System Reset	Asserting RESET_B pin	
	Supply voltage drops below VLVD	

Event Type	S32K1 reset sources	S32K3 reset sources
	WDOG / SWT reset request Software reset SOSC / FXOSC failure System PLL loss of lock	
		Clock Monitoring unit (CMU) detects a failure of: - CORE_CLK - AIPS_PLAT_CLK - HSE_CLK
		Clock generation Module (CGM) reports a System clock dividers alignment failure
	Core attempts to enter Stop mode, but not all modules acknowledge the request	STANDBY exit (Destructive)
	Core being locked (unrecoverable exception)	
		Self-Test Control Unit (STCU) - Self-test done - Unrecoverable fault
		Fault Collection & Control Unit (FCCU) - Failure to react. - Reset reaction
Debug Reset	MDM-AP (resets via JTAG/SWD) JTAG module	
HSE Reset		HSE SWT Timeout HSE boot reset Tamper Detect SNVS Tamper Detect

NOTE

Many reset functions for the chip as well as the reset sequence monitoring are managed by the Reset Control Module (RCM) in S32K1, and by the Reset Generation Module (MC_RGM) in the S32K3.

In terms of boot, the following table shows the general considerations for both S32K1 and S32K3.

Table 13 Boot considerations

Event Type	S32K1	S32K3
System RAM ECC initialization	Yes	Yes
Vector Table Offset Register (VTOR) initialization	Yes	Yes
Watchdogs	Disable watchdog (WDOG) if not required.	Enable corresponding watchdog (SWTx) if required by application.
Flash configuration	16 bytes of configuration data located at address 0x400: Contains boot options, Pflash/Dflash protection settings and flash security setting.	Device Configuration Format (DCF) records: A set of records stored in UTEST memory area to configure certain registers of the device during system boot.

Event Type	S32K1	S32K3
Memory/resources protection	NXP System MPU configuration	ARM Cores MPUs configuration. XRDC: Module to configure access policies of the bus masters to memory, peripherals, and pin resources. -> If HSE security usage enabled: Application needs to provide static XRDC configuration structure. The structure is read by SBAF boot firmware to configure XRDC accordingly. -> If HSE security usage disabled: Application to configure XRDC in runtime.
Other	NA	Boot header: A piece of data installed by the application, containing mainly the application cores to enable, boot address for each core, pointer to XRDC configuration (if HSE security usage enabled) and optional authentication tag.

6. Security

The S32K1 and S32K3 families both offer a security engine, for S32K1 it is called CSEc (Cryptographic Services Engine compact) and in S32K3 devices the module is called HSE (Hardware Security Engine). The following table provides a high-level comparison of the two security modules.

Table 14 Security differences

	S32K1	S32K3
Security System	CSEc	HSE-B
Location in SoC architecture	Embedded within Flash Controller	Independent Subsystem

		module.	
Firmware Upgradable		No	Yes
Security Ciphers	Symmetric	AES-128	AES-128 / 192 / 256 (50+ keys)
	Cipher modes	ECB, CBC	ECB. CBC, CMAC, GMAC, CTR, OFB, CCM, GCM
	Asymmetric	No	RSA (up to 4096 bytes) & ECC (up to 521 bytes)
	Hash	Miyaguchi-Preneel	Miyaguchi-Prenee, SHA-2/SHA-3 (up to 521 bytes)
Secure Boot		Secure boot as specified in SHE. Single memory area for verification using CMAC.	Up to 32 flexible memory regions to verify. Authentication tag can be CMAC, GMAC or RSA/ECC signature.
Random Number Generator		TRNG	TRNG & PRNG (AIS & NIST compliant)
Attack Resistance		No	Side Channel Resistance / Environment Monitoring
Code Flash		12 Kbytes (used) shared memory with EEPROM emulation	< 128 KB in Secured part of PFlash.
Data Flash		Depends number of keys, shared memory with EEPROM emulation	2 x 8 Kbytes (for Key Storage)
Requirement coverage		SHE+ Global-B CYS 2200	SHE+, Global-B, CYS 2200+, FCA Specification Customer Applications
Host interface		Commands and input/output data sent through the CSE_PRAM dedicated memory. Error flags sent back also through CSE_PRAM. Status read through flash controller registers.	Commands sent through the MU (Messaging Unit) registers. Input/output data shared through System RAM. Errors read from MU registers.

6.1. Considerations for migrating to K3

The following are the most important considerations when migrating between S32K1 and S32K3 device families in terms of security:

- Depending on S32K1 part number (CSEc enabled or not), CSEc is directly available in parts out of factory. For S32K3 parts, HSE firmware is delivered separately to be installed by customers following a chain of trust.
- For S32K3 multicore parts, the program must be designed so that both cores make an effective use of the HSE resources (MU channels), or prohibit access to either core, depending on the application needs. This can be done by leveraging XRDC, semaphores, or by software means. S32K1 devices are single core, no especial considerations to take in this regard.
- In S32K1 the Flash controller is not available for other flash commands (e.g. for program flash writes or EEPROM emulation writes) while a CSEc command is in progress. HSE module does not impose such restrictions of the flash controller.

7. Safety

S32K1 family covers ASIL B hardware requirements and S32K3 family covers both ASIL B and ASIL D requirements (depending on the family member). Alongside the microcontroller capabilities, a safety library is also provided and is already available for S32K3. The table below presents the major differences on safety topics.

Table 15 S32K1 and S32K3 safety related differences (related only for ASILB)

	S32K1	S32K3
Memory Protection Unit (MPU)	NXP proprietary	ARM MPU + XRDC
Error Injection Module (EIM) **Error Reporting Module (ERM)**	Both*	
Temperature sensor	YES (monitored via ADC)	
eDMA Controller	YES*	
Clock monitoring units	S32K11x (2) * S32K14x (0)	6 *
Interconnect bus	Crossbar switch (AXBS-Lite) + Peripheral Bridge (AIPS-Lite) *	
External Watchdog Monitor	YES (only on S32K14x family)	Yes, Resolved via FCCU
PMC (Power management control)	PMC with ASIL B	ASIL B: Implement ASIL B PMC with less Safety Measures

	S32K1	S32K3
		ASIL D: Covered

* Compatible configuration registers

The new Safety features on S32K3XX to arrange ASIL D:

- Lockstep mode.
- Built-In Self Test for Memory and Logical (MBIST/LBIST)
- Extended Resource Domain Controller (XRDC): memory and peripherals assigned for specific application cores.
- Fault Collection and Control Unit (FCCU). Key module to handle safety related events.
- Virtualization wrapper (VIRT_WRAPPER): IO signal assigned for specific cores
- Interrupt monitor (INTM)
- Crossbar Integrity Checker (XBIC)
- Self-test General-Purpose Registers (SELFTEST_GPR)
- Register Protection (REG_PROT)

7.1. Considerations for migrating to K3

If the application requires until ASIL B, it can be reused the S32K1 configuration and operation. If the application requires ASIL D, the new S32K3 safety modules listed above must be used. For S32K1xx, it is available a set of example codes for safety, including bare metal and SDK oriented code. For S32K3xx, it will be offered a Safety Software Framework.

8. Timing, Cross Triggering and ADC

This set of IP modules are commonly used, together, for many automotive use cases: ADC, BCTU, eMIOS, LCU and TRGMUX. The following tables shows the main differences between S32K1xx and S32K3.

Table 16 S32K1 and S32K3 Trigger Mux differences

TRGMUX	S32K1xx	S32K3
Internal and external routing options	Inputs: 77 Outputs: 58	Inputs: 128 Outputs: 112 Added eMIOS odis signals Added LPUART RX, TX, IDLE Added LCU1_LCU2 I/O support

TRGMUX	S32K1xx	S32K3
External pins I/O options	Inputs: 12 Outputs: 8	Inputs: 12 Outputs: 8

Table 17 S32K1 and S32K3 ADC differences

ADC	S32K1xx	S32K3
Instances / Channels	ADC_0: 32 external analog input channels ADC_1: 32 external analog input channels	ADC_0: 16 standard channels ADC_1: 16 standard channels ADC_2: 16 standard channels
Resolution	12-bit resolution	Up to 14-bit resolution
Self-Test	NO ADC Self-test	ADC Self-test

Table 18 S32K1 vs. S32K3 Timer Modules differences

Timer Modules	S32K1xx	S32K3
	FTM	**eMIOS**
Instances and Channels	Up to 4 FTM instances with 8 channels each.	up to 3 eMIOS instances eMIOS0: 24 channels (X/G/H/Y) eMIOS1: 24 channels (types: X/H/Y) eMIOS2: 24 channels (types: X/H/Y)
Prescaler and Counter Buses	Prescaler divide-by 1, 2, 4, 8, 16, 32, 64, or 128	Counter buses B, C, D, and E can be driven by Unified Channels 0,8,16, and 24, respectively. Counter bus A can be driven by Unified Channel 23. Counter bus F can be driven by a specified Unified Channel
Operation Modes	• Simple Input Capture, • Output compare, • Edge-Aligned PWM mode	• General-Purpose Input/Output (GPIO) • Single-Action Input Capture (SAIC) • Single-Action Output Compare (SAOC) • Input Pulse-Width Measurement (IPWM) • Input Period Measurement (IPM) • Double-Action Output Compare (DAOC) • Pulse/Edge Counting (PEC) • Modulus Counter (MC)

Timer Modules	S32K1xx	S32K3
		• Modulus Counter Buffered (MCB) • Output Pulse-Width and Frequency Modulation Buffered (OPWFMB) • Center Aligned Output Pulse Width Modulation with Dead Time Insertion Buffered (OPWMCB) • Output Pulse-Width Modulation Buffered (OPWMB) • Output Pulse-Width Modulation with Trigger (OPWMT)
Fault Control	Up to 4 fault inputs for global fault control	No fault inputs for global fault control

Table 19 S32K1 and S32K3 Logic Control Unit differences.

LCU	S32K1xx	S32K3
Instances	NONE	2 LCU instances, each with 3 logic cells with programmable logic function for generating output results LCU logic cells: 3 *Added 3 logic cell to allow 12 phase motor control applications (requires 24 PWM outputs)
I/O	NONE	12 inputs to logic cells and 12 outputs from logic cells LCU signal inputs: 12 LCU signal outputs: 12
Fault Control	NONE	Fault inputs for global Fault control

Table 20 S32K1 and S32K3 Programmable Delay Block and Body Cross Triggering Unit differences.

Programmable delay block	S32K1xx	S32K3
	PDB	**BCTU**
Trigger Inputs	2 Trigger input sources 1 Software trigger source	Number of channels:72 (69 eMIOS channels + 3 TRGMUX channels) 1 Software trigger source
ADC hardware trigger	8 Configurable PDB channels for	Up to 4 selection multiplexers to select one trigger at a time for each

Programmable delay block	S32K1xx	S32K3
	ADC hardware trigger	ADC
Complementary Logic	none	1 Priority selection logic per ADC
Memory Self Resources	none	1 List of ADC channels 2 FIFOs

8.1.1. Considerations to migrate from K1 to K3

The principal difference for Timing, Cross triggering and ADC among K1 and K3 is the change in FTM and PDB in K1 for the new eMIOS, LCU and BCTU modules in K3. In K1 the fault signals are managed by the FTM module, in contrast with K3 where the fault signal is managed by the LCU. Another important consideration for K3 is the ADC self-test function, not available in K1 and the inclusion in K3 for FIFO's in the new BCTU module, for ADC conversion sequences storage, contrasting the PDB module in K1 where no FIFOS are supported.

9. Communication modules

9.1. Ethernet MAC

The S32K3 family introduces a new Ethernet IP compared to the S32K1 family. The following table provides a high-level overview of differences between the two Ethernet IPs.

The information included in the table applies to all the S32K3 devices except for the S32K358 (8 MB variant). The S32K358 features an Ethernet Controller IP with similar architecture and functionality as the EMAC module, but with differences in terms of capabilities, being the major one that it has support for Gigabit Ethernet speed (1 Gbps), more detailed information is planned for the next revision.

Table 21 Ethernet IP differences

	S32K1	S32K3
Ethernet MAC controller	ENET	EMAC
Supported speeds	10/100 Mbps	10/100 Mbps 200 Mbps (MAC to MAC)
Tx Queues	1	2
Rx Queues	1	2
Tx FIFO size	2048 Bytes	8192 Bytes
Rx FIFO size	2048 Bytes	8192 Bytes

	S32K1	S32K3
Network acceleration features	Checksum generation and checking (IPv4, IPv6, TCP, UDP, ICMP)	Checksum generation and checking (IPv4, IPv6, TCP, UDP, ICMP)
Address filtering	MAC address Multicast and unicast based on 64-bit hash filter	MAC address Multicast and unicast based on 64-bit hash filter VLAN tag based Layer 3 and Layer 4 based
VLAN tags	Rx Frames: Detection	Tx Frames: Insertion, replacement and deletion. Rx Frames: Detection and deletion
Rx Frame parser	No	Yes
Time stamping (IEEE 1588)	Yes	Yes
Time Sensitive Networking (TSN) features	No	Time based scheduling (IEEE 802.1Qbv) Frame pre-emption (IEEE 802.1Qbu and IEEE 802.3br)
Traffic Shaping	SW	HW, with 2 transmission queues
Packet Sorting	SW	HW, with 2 reception queues
Programming model	Transfers handled using Buffer descriptors + Data Buffers	Transfers handled using Buffer descriptors + Data Buffers Context descriptors: Provide additional information (timestamp, vlan tags, etc).
Automotive Safety Features	No	ECC (Error Correction Code) protection for memories ECC error injection Parity and timeouts protection

9.1.1. Considerations for migrating to K3

The S32K3 Ethernet module has two Tx queues and two Rx queues. This advantage can be leveraged where possible for applications requiring two virtual communication channels over the same Ethernet bus.

The available interrupts are generated by different events or conditions in ENET module (S32K1) in comparison to the EMAC module (S32K3). It should be considered in the handling logic of the software driver or networking stack. The specifics are out of the scope of this guide, refer to the corresponding chapter in the device Reference Manual.

9.2. FlexCAN

The S32K3 incorporates an upgraded FlexCAN peripheral, with multiple new capabilities added for the reception of CAN-FD frames of up to 64-bytes payload length; such as reception in First-in-First-out order (RX FIFO) and DMA transfers, both handled entirely by hardware.

The following table summarizes the differences between FlexCAN in S32K1 and S32K3

Table 22 Changes of the FlexCAN peripheral between S32K1 and S32K3

Feature	S32K1	S32K3
CAN-FD	Only available in few instances	Available in all instances
Reception FIFO (RX FIFO)	For CAN 2.0B frames	For CAN classic and CAN-FD
Timestamping timer	16-bit wide	32-bit with added tick sources
DMA transfers	Only for CAN classical	Available for both CAN and CAN-FD
Message buffers	All instances have up to 32 message buffers (MB's)	Up to 96 Message buffers
Pretended Networking (PNET)	Available in FlexCAN0	Not supported
ECC memory	Not available	Each byte of FlexCAN memory is associated with 5 parity bits

9.2.1. Considerations for migrating to S32K3

The S32K3's FlexCAN module is 100% backwards compatible with the S32K1's one, except for the pretended networking (PNET) feature which is no longer available.

CAN-FD operation together with the new Enhanced RX-FIFO is now supported, allowing for an interrupt-less reception of up to 64-byte payload frames with a FIFO depth of 20 frames, and matching of up to 64 extended or 128 standard IDs is available, with three possible filtering schemes; mask and filter, a range between two IDs and two filters without mask.

9.3. FlexIO

The FlexIO module in S32K3 is bigger than S32K1 in the number of pins, timers and shifters also have new functionalities that are showing in the following tables

Table 23 FlexIO differences

	S32K1	S32K3
No. of pins	8	32
No. of timers	4	8
No. of shifter registers	4	8
No. of bits in counter	16	16
Interrupt request	✔	✔
DMA request	✔	✔
Adding Time stamp		✔
State machine		✔

Table 24 FlexIO Operation Data rate limitation

FlexIO Operation Data rate limitation	S32K1	S32K3
Master Tx	FlexIO_clk_Div_4	FlexIO_clk_Div_4
Slave Tx		FlexIO_clk_Div_10
Master Rx	FlexIO_clk_Div_6	FlexIO_clk_Div_8
Slave Rx	FlexIO_clk_Div_6	FlexIO_clk_Div_6

Table 25 FlexIO protocols support

	S32K1	S32K3
UART	✔	✔
I2C	✔	✔
SPI	✔	✔
PWM/Waveform generation	✔	✔
I2S	✔	✔
Display interface		✔ (Requires further validation at the complete application level)
Camera IF		✔
Motorola 64k/ Intel 8080		✔
SENT	✔ (through the usage of Flextimer module)	✔
Input capture		✔
Keypad Interface	✔	✔

9.3.1. Considerations for migrating to K3

To migrate from the S32K1 to S32k3 is important to verify the FlexIO operation Data rate limitation because of the differences in both families.

9.4. QuadSPI

Although QSPI (QuadSPI) is a communication protocol, its main intended use case is as a memory interface, giving greater possibilities to be able to store and execute code from an external memory connected. The table below indicates main differences.

Table 26 S32K1 and S32K3 QSPI differences

Feature	S32K1	S32K3
QSPI max communication clock (4MB version)	Side A: up to 80MHz Side B: up to 20MHz (when Core is at full speed)	K358: up to 125MHz K344: up to 120MHz K342: up to 80MHz (when Core is at full speed)

Number of data lines	4 for SDR and 8 for HyperRAM	K358: 8 for SDR K34x: 4 for SDR
SDR support	YES	
DDR support	YES: Only side B	Only on K358
Execution in Place (*run code from ext. Flash*)	YES	
Max communication speed	Up to 320Mbps	K358: Up to 2Gbps K344: Up to 480Mbps
Max data rate when core is at full speed	Up to 320Mbps	K358: Up to 2Gbps K344: Up to 480Mbps
QSPI & ENET simultaneously	NO	YES (at 120MHz ~ 480Mbps)
AHB access for reading	YES	YES
Direct memory mapping of external flash.	YES	YES
AIPS access read/write	YES/YES	YES/YES
AHB Buffer	1kB	256B
RXFIFO	128B	128B
LUT SIZE	16	4
QSPI A port	YES	YES
QSPI B port	YES	NO
HyperRAM, HyperFLASH	YES	Only on K358

9.4.1. Considerations for migrating to K3

On the S32K1 family, only S32K148 includes the QuadSPI interface, while on the S32K3 family, S32K3x4 and S32K3x2 devices have this interface. S32K3x1 does not include QSPI interface.

One important difference between S32K1 and S32K3 about the QSPI module is the number of ports. S32K3 includes only port A, while in S32K1, we can find Port A and Port B. Considering this, S32K3 does not support HyperRAM, HyperFlash and DDR. On the other hand, S32K3 QSPI gives the advantage of supporting QSPI and EMAC simultaneously and higher speed.

9.5. UART/LIN

The LPUART includes registers to control baud rate, select options, report status, and store transmit/receive data. Access to an address outside the valid memory map generates a bus error. The LPUART supports full-duplex, asynchronous, NRZ serial communication and comprises a baud rate generator, transmitter, and receiver block. The transmitter and receiver operate independently, although they use the same baud rate generator. The following describes each of the blocks of the LPUART.

Table 27 LPUART functional blocks

Feature	S32K1	S32K3
LIN support	YES	YES
LIN Master	YES	YES
LIN Slave	YES	YES
Auto-synchronization	YES	YES
RXFIFO	4 word	4 word
TXFIFO	4 word	4 word
Parity	Even, odd, 1, 0	Even, odd, 1, 0
DMA support	YES	YES
Number of instances	up to 24	up to 16

9.5.1. Considerations for migrating to K3

For considerations to migrate from the K1 to K3 on LPUART, everything is pretty the same just the number of instances on the K3. For more information about instances for each device please consult the last version of the Reference Manual.

9.6. SPI

The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus, either as a master and/or as a slave.

Table 28 SPI features

Feature	S32K1	S32K3
Word size	32 bits	32 bits
Slave operation	Yes	Yes
Master operation	Up to 4 peripheral chip selects	Yes
DMA	Yes	Yes
Command/transmit	4 words	4 words
Receive FIFO	4 words	4 words

9.6.1. Considerations for migrating to K3

In K1 the number of interfaces was limited to three LPSPI modules on the S32K148. In the K3 the number of instances increases to four on the S32K311, S32K312, S32K322, and S32K342 and to six on the S32K314, S32K324, S32K344 and S32K358.

9.7. I2C

The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or as a slave.

- The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation.
- The LPI2C is designed to use little CPU overhead, with DMA offloading of FIFO register accesses.

The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 3. The SMBus is a single ended simple two-wire bus, which is typically used for low bandwidth communications.

Table 29 I2C features

Feature	S32K1	S32K3
I2C max communication speed (Slave mode)	up to 400Khz	up to 3.4 MHz
I2C max communication speed (master mode)	up to 400kHz	up to 400kHz
SMBus support	YES	YES
RXFIFO	4 word	4 word
TXFIFO	4 word	4 word
DMA support	YES	YES
# of instantiation	1	2

9.7.1. Considerations to migrating to K3

As is shown in the above table, is important to consider that the communication speed on slave mode increases up to 3.4Mhz. Besides that, the number of interfaces also increases up to two on the S32K311, S32K312, S32K322, S32K342, S32K314, S32K324, S32K344 and S32K358. It is important to mention that on the K3 a new derivative was added: I3C.

NOTE

I3C is not available on the S32K3x4 family members.

9.8. SAI

The SAI (Synchronous audio interface) module provides an interface that supports full-duplex serial interfaces with frame synchronization, different protocol supported, such as I2S, AC97, TDM, and codec/DSP interfaces. These peripheral remains very similar between K1 and K3 family, below table shows the functionalities.

Table 30 S32K1 and S32K3 SAI differences

Feature	S32K1xx	S32K3xx
Word size	32 bits	32 bits
Maximum Data Rate on communication channel	12.288 Mbps (Master Clock = 24.576 MHz)	12.288 Mbps (Master Clock = 24.576 MHz)
Number of communications channels	4 of SAI0 + 1 of SAI1	4 of SAI0 + 1 of SAI1
Frame Synchronization	I2S / AC97 / Codec-IF / DSP-IF /TDM	I2S / AC97 / Codec-IF / DSP-IF /TDM
DMA	Yes	Yes
TX FIFO size	8-32 bits	8-32 bits
Maximum frame size per data line	16 words	16 words
Working in low power mode	OFF in STOP1 and VLPS, FF in STOP2, VLPR and HSRUN	OFF

9.8.1. Considerations for migrating to K3

As mentioned before, there are not major changes in SAI module between K1 and K3. S32K3 add some bitfields that allow some features, like BCS which allow bit clock swap in async mode, or like BYP which allow bypass the bit clock signal. Something important to consider is that SAI module in S32K1 is only available in S32K148, while in S32K3 family, it is included in the S32K314, S32K32x and S32K34x variants. S32K311 and S32K312 does not include SAI module.

10. Pin management and characteristics

The pin configuration between S32K1xx and S32K3xx is completely different.

The S32K1xx has two modules for the pin configuration PORT and GPIO. The S32K3xx has one module to handle the pin configuration called Signal Integration Unit Lite (SIUL2).

10.1. Port and pin assignment

Table 31 Difference between S32K3xx and S32K1xx port and pin assignment

S32K1xx (PORT register)	S32K3xx (SIUL2_MSCR register)
PORTA[0-31]	MSCR0 - MSCR31
PORTB[0-31]	MSCR32 - MSCR63
PORTC[0-31]	MSCR64 - MSCR95
PORTD[0-31]	MSCR96 - MSCR127
PORTE[0-31]	MSCR128 - MSCR159
	MSCR160 - MSCR191
	MSCR192 - MSCR219

10.2. K1 and K3 pin features

PORTn_PCR is the register that contains the specific pad settings (pull up, interrupt status flag, pin mux control, etc.).

SIUL2_MSCR is the register that contains the description of control signals (pull up, output enable, input enable, etc.).

Table 32 Differences between S32K3xx and S32K1xx pin features

	S32K1xx	S32K3xx
Pull Up / Pull Down	Yes	
Pad keeping	All I/O retain their state in low power modes.	Yes (configurable)
Slew rate control	No	Yes
Drive strength	Yes	
Input filter	Yes	Supported for RESET pad only (PTA5)
Pin mux control	Yes (PCR_MUX)	Yes (MSCR_SSS)
GPIO	Yes Alternative 1	Yes Alternative 0
GPIO input	Yes	Yes

	S32K1xx	S32K3xx
	(PTx_PDIR)	(GPDIx_PDI)
GPIO output	Yes (PTx_PDOR)	Yes (GPDOx_PDO)

10.3. External Interrupts

The S32K1xx configure the external interrupts by port. It means that any pin can be used as an external interrupt. To configure an external interrupt in S32K1xx the PORTx_PCRn[IRQC] register is used.

To configure in S32K3xx external interrupt by a specific pin. To know which pin can be used as an external interrupt see attached “S32K3xxIO_Signal_Multiplexing” in the Reference Manual. To configure an external interrupt the S32K3xx has the following registers.

- DIRER
- DIRSR
- IREEER / IFEER
- DISR

11. Hardware and pinout

The difference between the S32K1 MCUs and the S32K3 MCUs family is considerable. The MCU packages are different and the customer would need to perform a more detailed analysis to understand the extent of the redesign that needs to be considered. The table below summarizes all MCU packages per family.

Table 33 S32K3 and S32K1 MCU family package options

S32K3xx Family		S32K1xx Family	
Part	**MCU Package Type**	**Part**	**MCU Package Type**
- S32K344 - S32K324 - S32K314	257MBGA	- S32K148	176LQFP
- S32K312 - S32K344 - S32K342 - S32K324 - S32K322 - S32K314	172MaxQFP	- S32K148 - S32K146	144LQFP

S32K3xx Family		S32K1xx Family	
- S32K312 - S32K311 - S32K342 - S32K322	100MaxQFP	- S32K148 - S32K146 - S32K144 - S32K142	100LQFP
- S32K311	48LQFP	- S32K148 - S32K146 - S32K144	100BGA
		- S32K144 - S32K146 - S32K142 - S32K118	64LQFP
		- S32K144 - S32K142 - S32K118 - S32K116	48 LQFP
		- S32K116	32 QFN

Table 34 S32K3XX power supply pins

			Power supply pins and domains										
			VDD [1]	VDDA	VDD_HV_A [1] [2]	VREFH	VDD_HV_B [2]	V15	V25 [4]	V11 [4]	XTAL/EXTAL	VSS/VREFL	GPIOs
S32K3 MCU Family	S32K344 /24 /14	257 MBGA	-	-	5	1	3	4	1	4	2	19	218
	S32K344 /42 /24 /22 /14	172 MaxQFP	-	-	5	1	3	4	1	4	2	10	142
	S32K342 /22	100 MaxQFP	-		3	1	2	2	1	2	2	7	80
	S32K312	172 MaxQFP	-	-	8	1	-	-	1	4	2	11	145
	S32K312 /11	100 MaxQFP	-	-	4	1	-	-	1	2	2	7	83

			Power supply pins and domains										
			VDD [1]	VDDA	VDD_HV_A [1] [2]	VREFH	VDD_HV_B [2]	V15	V25 [4]	V11 [4]	XTAL/EXTAL	VSS/VREFL	GPIOs
	S32K311	48 LQFP	-	-	TBD	TBD	-	-	TBD	TBD	TBD	TBD	TBD
S32K1 MCU Family	- S32K148	176 LQFP	8	1	-	1	-	-	-	-	2[5]	10	157
	- S32K148 - S32K146	144 LQFP	6	1	-	1	-	-	-	-	2[5]	8	126
	- S32K148 - S32K146 - S32K144 - S32K142	100 LQFP	4	4	-	1	-	-	-	-	2[5]	5	84
	- S32K148 - S32K146 - S32K144	100 BGA	4	4	-	1	-	-	-	-	2[5]	5	84
	- S32K144 - S32K146 - S32K142 - S32K118	64 LQFP	2	1	-	1	-	-	-	-	2[5]	2	56
	- S32K144 - S32K142 - S32K118 - S32K116	48 LQFP	2	1	-	-	-	-	-	-	2[5]	2	41
	- S32K116	32 QFN	2	-	-	-	-	-	-	-	2[5]	2	26

[1] Normal Operation Voltage +3.3V or +5.0V
[2] Domain voltage for I/O pins
[3] VREFH ≤ VDD_HV_A for S32K3xx and VREFH ≤ VDD for S32K3xx
[4] Internal MCU reference
[5] XTAL and EXTAL pins can be configured as GPIO if external oscillator is not connected for S32K1 only

Table 35 S32K3 and S32K1 summary of HW IP differences per package variant

MCU Pin Name	S32K3								S32K1						
	MCU Package								MCU Package						
	S32K311 48LQFP	S32K342 /22 100MQFP	S32K312 /11 100MQFP	S32K344 /42 /24 /22 /14 172MQFP	S32K312 172MQFP	S32K344 /24 /14 257MBGA	176 LQFP	144 LQFP	100 BGA	100BGA	64 LQFP	48 LQFP	32QFN
	Power Domain								Power Domain						
	A	A	B	A	A	B	A	A	B	VDD/VDDA					
GPIOs		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
ADCx		■		■	■		■	■		■	■	■	■	■	■	▪
TSPC		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
JTAG		■		■	■		■	■		■	■	■	■	■	■	▪
TRACE		■		■	■			■		■	■					
SWD		■		■	■		■	■		■	■	■	■	■	■	▪
ADCx		■		■	■		■	■		■	■	■	■	■	■	▪
CMPx		■		■	■		■	■		■	■	■	■	■	■	▪
FXIO		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
EMIOSx		■	■	■	■	■	■	■	■							
WKPU		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
ENET			■			■			■	■	■					
QuadSPI			■			■			■	■	■					
LPSPIx		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
SAIx			■			■			■	■	■					
FCCU		■	■	■	■	■	■	■	■							
I2C		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
WKPU		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
EIRQ		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
CAN		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
LPUART		■	■	■	■	■	■	■	■	■	■	■	■	■	■	▪
I3C					■	■	■	■	■							
TRGMUX		■		■	■	■	■	■	■	■	■	■	■	■	■	▪

12. Software and tools

Software and tools become a major enablement for both S32K families. Key elements to highlight is that as much compatibility as possible is planned to be maintained to ease SW reuse from the customer, however, there are a few significant differences which need to be considered and will be highlighted in the following tables.

IDE/compilers (IAR, Greenhills, etc) are either already supporting or are planning on supporting both families.

12.1. Software products available or planned from NXP

Table 36 Software products available for the devices

	S32K1	S32K3
Autosar supported version	Autosar 4.0 / 4.2 / 4.3	Autosar 4.4
Non-Autosar SW development kit	SDK & Real Time Drivers (Planned in 2021)	Real Time Drivers
Math and motor control library	Yes	Yes
Security	MCAL Crypto driver	HSE FW and MCAL Crypto driver
Safety	S32K1 safety cookbook implementation example code	Safety Framework
Operating system	FreeRTOS	FreeRTOS
Bootloader	BootLoader	To be confirmed
LIN stack	Yes	Yes
TCP/IP stack	Yes	Yes
FreeMaster	Yes	Yes
Iseled	Yes	To be confirmed
Model based design toolbox	Yes	Yes

12.2. Debugging capabilities

In terms of partner debugger/IDE/compiler tools, all of the known partners for debuggers (Lauterbach, IAR, Greenhills, P&E Micro, Segger, etc) The K1 and K3 devices have implemented the ARM Core sight debug IP, however K3 has enhanced debug capabilities.

Table 36 K3 Enhanced Debug Capabilities

S32K1	S32K3
MTB - Micro Trace Buffer	ETM - Embeded Trace Macrocell
MTB_DWT – Data Watchpoint and Trace	DWT - Debug Watchpoint and Trace.
N.A.	SWO - Serial Wire output
N.A.	ITM - Instrumentation Trace Macrocell
N.A.	FPB - Flash patch and breakpoints

N.A.	TPIU - Trace Port interface Unit
N.A.	ETF - Embedded Trace FIFO
N.A.	SWV - Serial Wire Viewer

In general, the debugging system for the K1 is less powerful than K3, however still capable of handling the typical requirements of the applications.

13. References

For more details, please refer to the corresponding detailed technical documents. Particularly for S32K1 all information is stored in nxp.com/s32k1, but for S32K3 information is still shared either through the corresponding customer FAE or via docstore.

- S32K1xx and S32K3xx reference manuals.
- S32K3 Product brief
- S32K1 and S32K3 safety manuals
- S32K1 Application notes
- HSE related information:
  - HSE Firmware Reference Manual
  - HSE_Service_Reference Manual
- S32K1 software (i.e. SDK, MCAL, cookbook)
- S32K3 software (i.e. Real Time Drivers, platform integration examples, BareMetal drivers)

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: AN13414
Rev. 0
10/2021