AN13304

Boot from QSPI Flash on MIMXRT595-EVK

Rev. 0 — 08 July 2021 Application Note

Contents

1 Introduction

The i.MX RT series support design flexibility through multiple external memory interface options, including NAND, eMMC, QuadSPI NOR flash, and parallel NOR flash. The software used in this document is based on the i.MX RT500 SDK 2.9.0. The development environment is MCUXpresso IDE v11.3.0 and IAR EWARM 8.50.6. The hardware development environment is MIMXRT595-EVK board.

The MIMXRT595-EVK board supports two different external flashes, Octal (default) and QSPI. The SDK provides out-of-the-box support for the octal flash, but if the user wants to switch to the QSPI flash memory, there are a few modifications required in hardware and software. For details, see Figure 1.

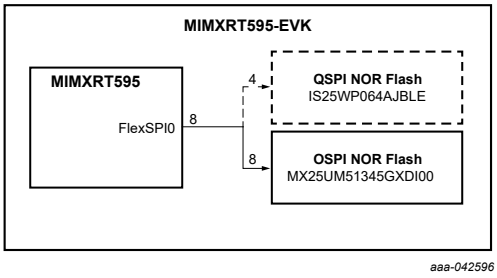

Figure 1. NOR flash memories available in MIMXRT595-EVK

2 MIMXRT595-EVK modifications for QSPI flash

2.1 MIMXRT595-EVK hardware modification

The MIMXRT595-EVK configures the hardware connections to use Octal flash (MX25UM51345GXDI00) by default. To switch to QSPI flash (IS25WP064AJBLE), the user requires to modify the hardware connections, see Figure 2.

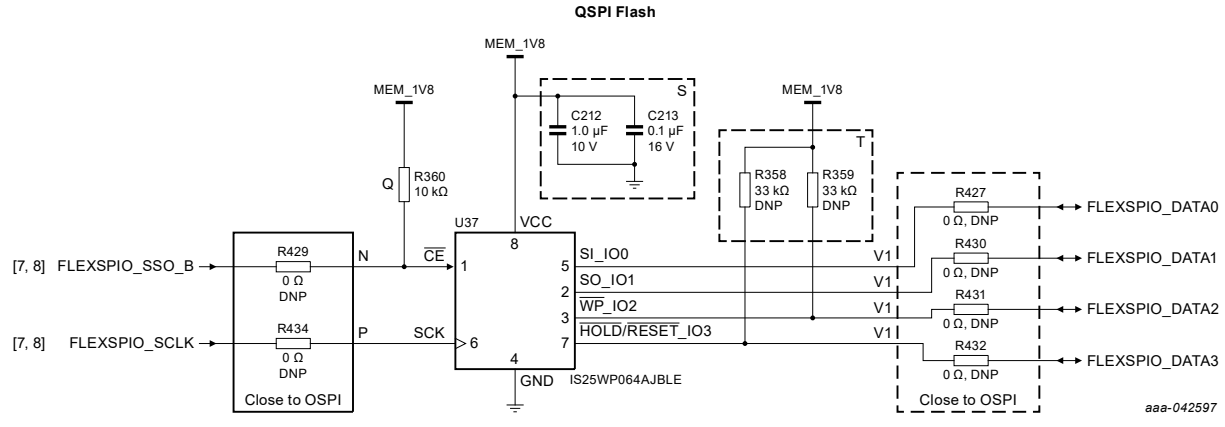

Figure 2. QSPI flash connections

Table 1 summarizes the hardware configurations required by the flash memories available in the evaluation board.

Table 1. MIMXRT595-EVK memory configurations

Type	Populated	DNP
QSPI (IS25WP064AJBLE)	N, P, Q, S, V1	A, B, C, D, E1, E2, F, L, T
OSPI (MX25UM51345GXDI00)	A, B, C, D, E1, E2, F, G, H, M, Q, S	J, K, L, N, P, T, V1

2.2 MIMXRT595-EVK software modification

The MIMXRT595-EVK SDK configures the project settings and software to use Octal flash by default. To switch to QSPI flash, the user requires to adapt the following items:

- Flash Configuration Block
- FlexSPI0 clock frequency
- Flash driver configuration

2.2.1 Flash Configuration Block

The Flash Configuration Block (FCB) is a 512 byte block of memory that stores the flash settings for the boot ROM to configure the FlexSPI controller.

The FCB is located at offset 0x400 on the flash device. If the `FLEXSPI_FLASH_AUTO_PROBE_EN` OTP fuse is not blown, the boot ROM looks at offset 0x400 on the flash device, if data at offset 0x400 equal to 0x42464346, the boot ROM reads the FCB into on-chip SRAM and configure the FLEXSPI controller using this FCB accordingly. See "Table 76. Flash Config Table" in *i.MX RT500 Low-Power Crossover Processor Reference Manual with Addendum* (document IMXRT500RM) for the details about fields within the FCB.

The SDK examples use the `/flash_config/flash_config.c` file to configure the FCB; the user can select not to include the FCB on the project by disabling `BOOT_HEADER_ENABLE` preprocessor macro in project properties, see Figure 3.

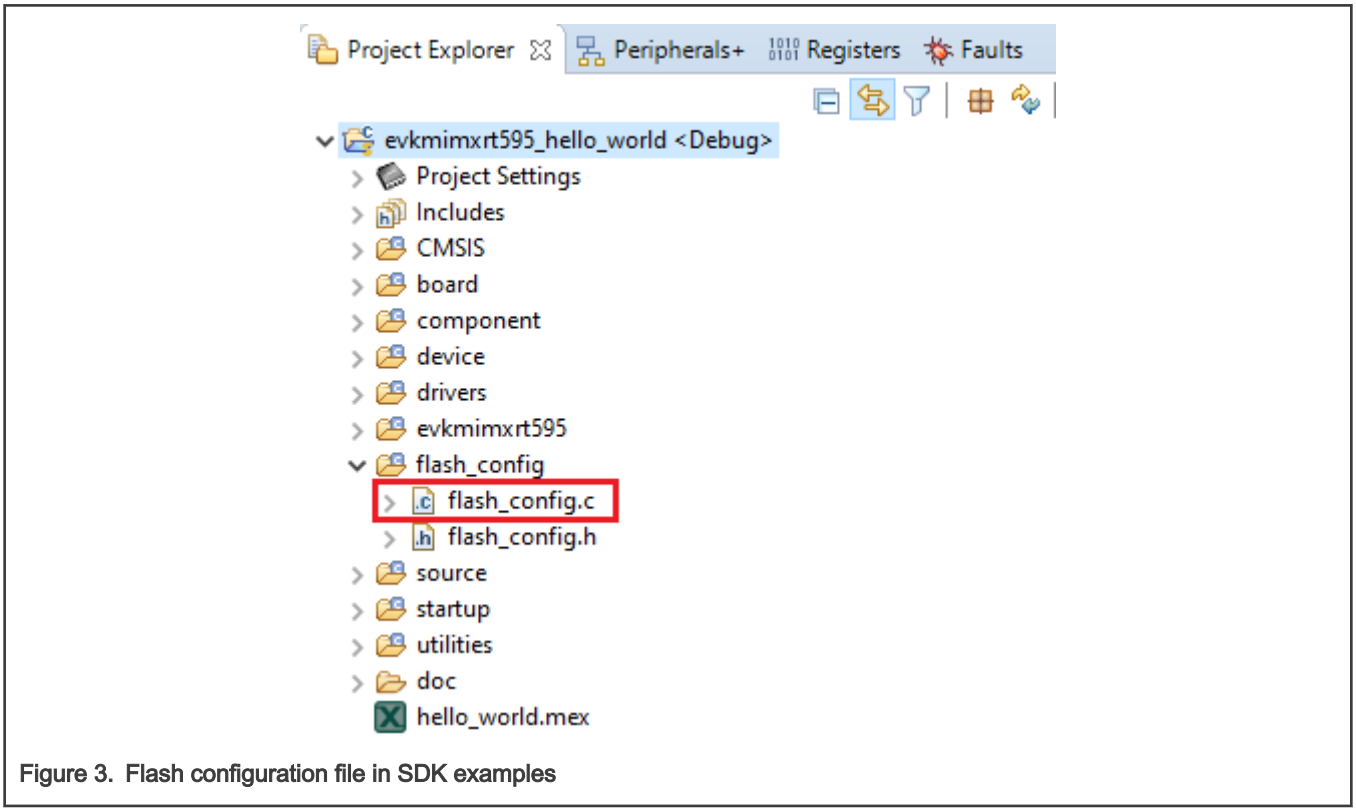

Figure 3. Flash configuration file in SDK examples

The following `flash_config` structure can be used for the QSPI flash (IS25WP064AJBLE) available on the MIMXRT595-EVK. Replace the `flash_config` configuration from the project to enable QSPI flash at `/flash_config/flash_config.c`

```
const flexspi_nor_config_t flash_config = {
    .memConfig =
        {
            .tag                = FLEXSPI_CFG_BLK_TAG,
            .version            = FLEXSPI_CFG_BLK_VERSION,
            .readSampleClkSrc   = kFlexSPIReadSampleClk_LoopbackFromDqsPad,
            .csHoldTime         = 3,
            .csSetupTime        = 3,
            .deviceModeCfgEnable = 0,
            .deviceModeType     = kDeviceConfigCmdType_Generic,
            .waitTimeCfgCommands = 0,
            .controllerMiscOption = (1u << kFlexSpiMiscOffset_SafeConfigFreqEnable),
            .deviceType    = kFlexSpiDeviceType_SerialNOR,
            .sflashPadType = kSerialFlash_4Pads,
            .serialClkFreq = kFlexSpiSerialClk_80MHz,
            .sflashA1Size  = 8ul * 1024u * 1024u,
            .lookupTable =
                {
                    /* Read */
                    [0] = FLEXSPI_LUT_SEQ(CMD_SDR, FLEXSPI_1PAD, 0xEB, RADDR_SDR, FLEXSPI_4PAD, 0x18),
                    [1] = FLEXSPI_LUT_SEQ(MODE8_SDR, FLEXSPI_4PAD, 0x00, DUMMY_SDR,
FLEXSPI_4PAD, 0x04),
                    [2] = FLEXSPI_LUT_SEQ(READ_SDR, FLEXSPI_4PAD, 0x04, STOP_EXE, FLEXSPI_1PAD, 0x0),

                    /* Read Status */
                    [4 * 1 + 0] = FLEXSPI_LUT_SEQ(CMD_SDR, FLEXSPI_1PAD, 0x05, READ_SDR,
FLEXSPI_1PAD, 0x24),

                    /* Write Enable */
                    [4 * 3 + 0] = FLEXSPI_LUT_SEQ(CMD_SDR, FLEXSPI_1PAD, 0x06, STOP_EXE,
FLEXSPI_1PAD, 0x00),
                },
        },
    .pageSize      = 256u,
    .sectorSize    = 4u * 1024u,
    .blockSize     = 64u * 1024u,
    .flashStateCtx = 0,
};
```

2.2.2 FlexSPI0 clock frequency

The SDK examples configure the FlexSPI0 interface frequency to `Main_Clk/2` (396 MHz/2 = 198 MHz).

NOTE

The max clock frequency supported by the Octal flash is 200 MHz.

When the QSPI is configured, the FlexSPI0 interface must be adjusted to meet max flash requirements, therefore user must configure divider `Main_Clk/3` (396MHz/3 = 132 MHz); the max clock frequency supported by the QSPI flash is 133 MHz.

This configuration is implemented in `BOARD_BootClockRUN()` function from `clock_config.c`.

```
BOARD_SetFlexspiClock(FLEXSPI0, 0U, 3); /* from BOARD_BootClockRUN() */
```

2.2.3 Flash driver

A flash driver contains the knowledge required to program the flash on a given MCU. This knowledge may be either hardwired into the driver, or some of it may be determined by the driver as it starts up (typically known as a *generic* flash driver).

Flash devices typically contain a data block describing their properties such as device size, low-level structure, and programming details. These data blocks and their use are collectively known as Serial Flash Discovery Protocol (SFDP). The standard for these blocks is described by JEDEC JESD216 standards.

Flash drivers cannot detect the type of flash (QSPI or Hyperflash) fitted on a board, it is responsibility of the user to ensure that the correct driver is used.

2.2.3.1 MCUXpresso flash driver

The LinkServer (CMSIS-DAP) Flash drivers are used by LinkServer debug connections. By default, the LPC-Link2 debug probe on the MIMXRT595-EVK is configured with CMSIS-DAP firmware to program and debug applications to the evaluation board.

In MCUXpresso, the flash driver is configured in Project Properties >> C/C++ Build >> MCU settings, see Figure 4.

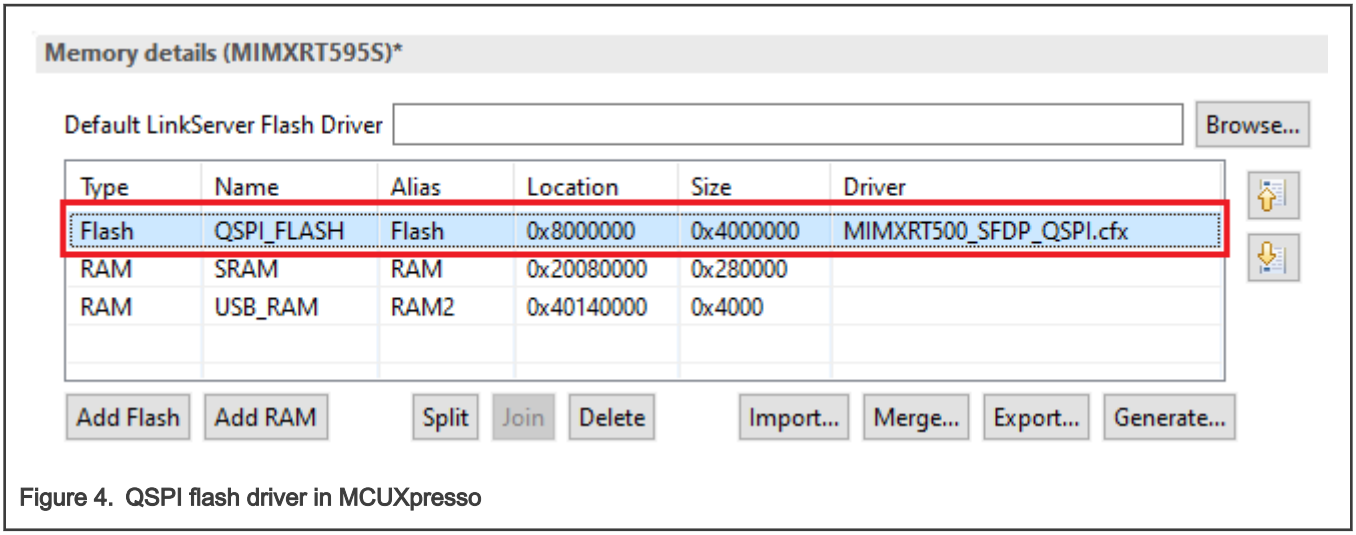

Figure 4. QSPI flash driver in MCUXpresso

See "Section 15.2.3 i.MX RT QSPI and Hyper Flash Drivers" in *MCUXpresso IDE User Guide* available on www.nxp.com for more details about the QSPI and Hyper Flash drivers in MCUXpresso.

2.2.3.2 IAR EWARM flash loader

IAR Embedded Workbench provides flash loaders for various microcontrollers. The flash loader for the MIMXRT500 supports OSPI and QSPI flashes from the MIMXRT595-EVK, user just must adjust a parameter in flash loader configuration to select between the two options.

The flash loader is configured on Project Options >> Debugger >> Download >> Edit, see Figure 5.

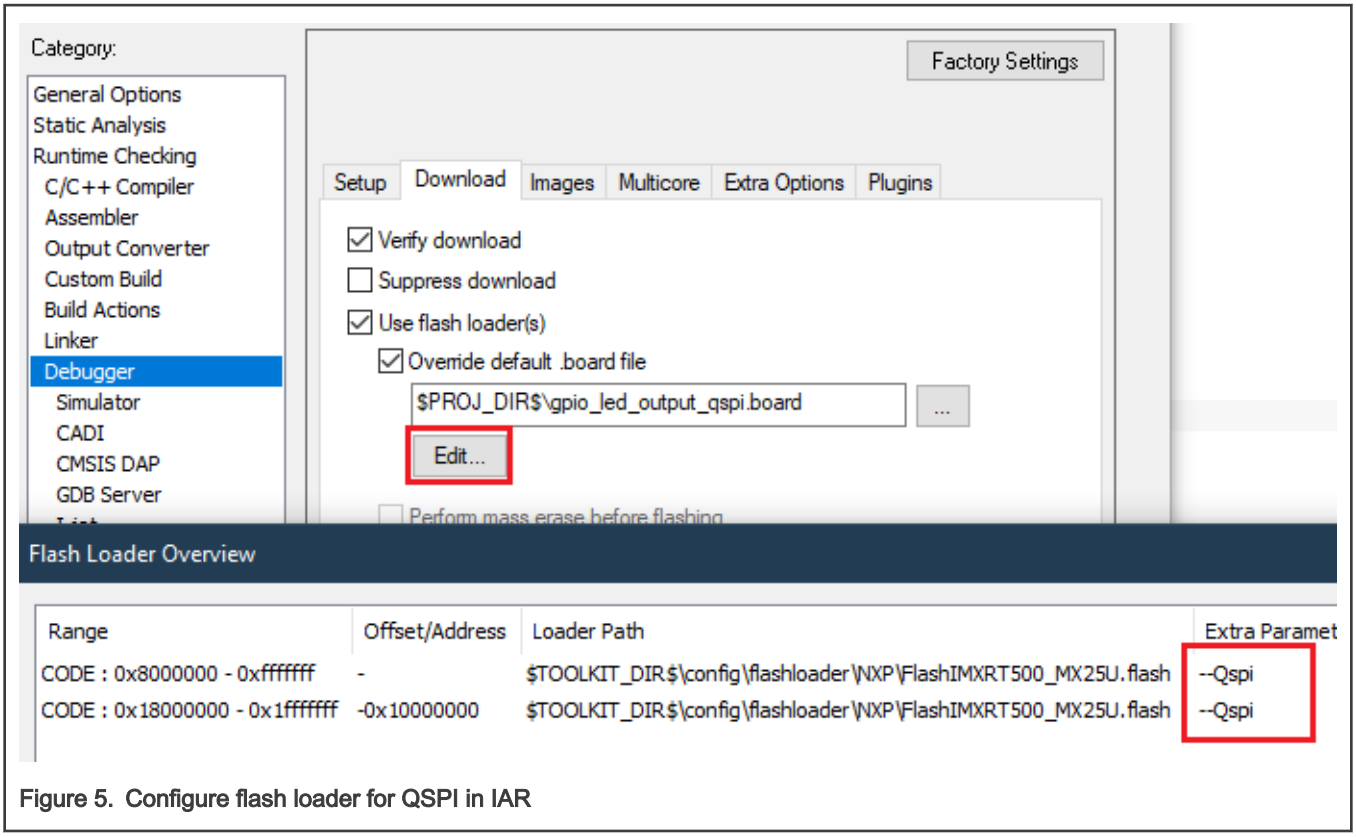

Figure 5. Configure flash loader for QSPI in IAR

Set `--Qspi` extra parameter for QSPI flash loader configuration and `--MxicOct` extra parameter for Octal flash loader configuration.

2.3 Obtain FCB using Boot ROM and blhost

The boot ROM supports read, write, and erase external Serial NOR Flash devices via the FlexSPI Module. The Boot ROM can generate the FlexSPI NOR Configuration Block based on the simplified Flash Configuration Option Block for several Serial NOR Flash devices in the market.

1. Configure board to boot from serial ISP (for UART, place SW7 to 100).
2. Connect board through port J40.
3. Download and extract blhost application from MCUBOOT: MCU Bootloader for NXP Microcontrollers.
4. Open a command line in Windows or terminal in Linux.
5. Navigate to `<blhost_path>\bin` location.
6. Steps in blhost to obtain FCB
    a. Verify communication between ROM and blhost:

```
blhost -p COMx get-property 1
```

    b. Store memory config parameter in RAM:

```
blhost -p COMx fill-memory 0x1c000 4 0xc0000002
```

    c. Apply config parameter stored in RAM to FlexSPI interface (0x9):

```
blhost -p COMx configure-memory 0x9 0x1c000
```

d. Verify, you can now communicate with the flash. Read the FCB region at 0x400 offset:

```
blhost -p COMx read-memory 0x8000400 0x200
```

e. Erase external flash starting from address 0x08000000, size 0x10000:

```
blhost -p COMx flash-erase-region 0x08000000 0x10000
```

f. Generate and program FlexSPI Nor FCB into flash for FlexSPI boot. The FCB was obtained by previous FlexSPI Config Parameter (0xc0000002 in this case). Store the FCB generating and program parameter into RAM:

```
blhost -p COMx fill-memory 0x1d000 4 0xf000000f
```

g. Generate FCB and program it to flash at offset 0x400 (0x8000400):

```
blhost -p COMx configure-memory 0x9 0x1d000
```

h. Verify that FCB is generated and stored at 0x8000400:

```
blhost -p COMx read-memory 0x8000400 0x200
```

After the configuration is obtained, return the ISP mode to boot from FlexSPI: Place SW7 to 001.

The FCB should be configured by now; You can copy the recently obtained configuration to the const `flexspi_nor_config_t flash_config` structure in `/flash_config/flash_config.c`, to include FCB as part of application binary. A simple way to do this is by running the flash_iap demo from RAM and store the contents from `0x8000400` to a flexspi_nor_config_t structure.

See "Section 18.6.1 Serial NOR Flash through FlexSPI" in *i.MX RT500 Low-Power Crossover Processor Reference Manual with Addendum* (document IMXRT500RM).

3 Revision history

Table 2 summarizes the changes done to this document since the initial release.

Table 2. Revision history

Revision number	Date	Substantive changes
0	08 July 2021	Initial release

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Limited warranty and liability — Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX,EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org. M, M Mobileye and other Mobileye trademarks or logos appearing herein are trademarks of Mobileye Vision Technologies Ltd. in the United States, the EU and/or other jurisdictions.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 08 July 2021
Document identifier: AN13304

arm