AN13218

PN7160 RF settings guide

Rev. 1.4 — 31 July 2024 Application note

Document information

Information	Content
Keywords	NFC, PN7160, NCI, RF settings
Abstract	This document provides further information about the PN7160 RF settings and offers guidelines to tune them to optimize RF performances according to the PN7160 integration.

1 Introduction

PN7160 offers a lot of physical registers to allow the Device Host (DH) to configure PN7160 in its system environment. From a system point of view, these registers are viewed as parameters with a dedicated address and programmable value, which, when opened to the user, can be addressed through NCI protocol (see [1]) via the physical connection.

The purpose of this document is to provide more information on the use of the different parameters, especially the ones related to the Contactless Interface (CLIF) corresponding to the RF configuration.

2 NCI command structure

2.1 Register setting command

The NCI command syntax is based on the TLV (Tag, Length, Value) mechanism as described in the PN7160 User manual [2].

According to the NCI 2.0 specification [1], the parameter space related to proprietary command use starts from the NXP proprietary extension Tag 0xA0. For PN7160 needs, the tag space has been extended and coded on 16 bits, starting from 0xA0 and followed by a second byte, which means 0xA0 XX.

An important example concerning the clock selection and configuration is given as below:

Name of the parameter: CLOCK_SEL_CFG

Tag Address: 0xA0 03

Length: 1

Value (default=crystal): 0x08

The corresponding NCI command setting parameter is then: **A0 03 01 08**

2.2 RF_TRANSITION_CFG parameter structure

The RF_TRANSITION_CFG parameter, which allows configuring the CLIF registers is different from the above structure since there must be transitions to take into account, as soon as a parameter is valid for different modes (for example, reader and card) while its value can be different.

The extension of the TLV structure is given as below:

- The Tag Address is usually 0xA0 0D
- The Length can be L=3, 4 or 6
- The Value is actually a secondary data area with a transition ID, the CLIF register offset (equivalent to an address), and the actual value.

Table 1. RF_TRANSITION_CFG parameter structure

Tag (2 Bytes)	Length (1 Byte)	Value (3, 4 or 6 Bytes, depending on the transition ID/CLIF register offset)		
0xA0 0D	0x03	Transition ID (1 Byte)	CLIF register offset (1 Byte)	1-Byte reg. value
	0x04			2-Byte reg. value
	0x06			4-Byte reg. value

Basically, depending on the polling loop events, the transition ID corresponds to a set of transitions applied in the registers.

The transition ID depends on:

- IN vs. OUT
  - In each IN transition a set of CLIF registers is loaded out of the EEPROM
  - In each OUT transition the settings are reverted
- Initiator vs. Target
- TX vs. RX
- Technology (A, B, F, etc.)
- Baud rate (106 kB/s etc.)

2.3 RF transitions

A simplified view of the different transition IDs is depicted in Figure 1 below. It does not include asymmetric data rates for instance.

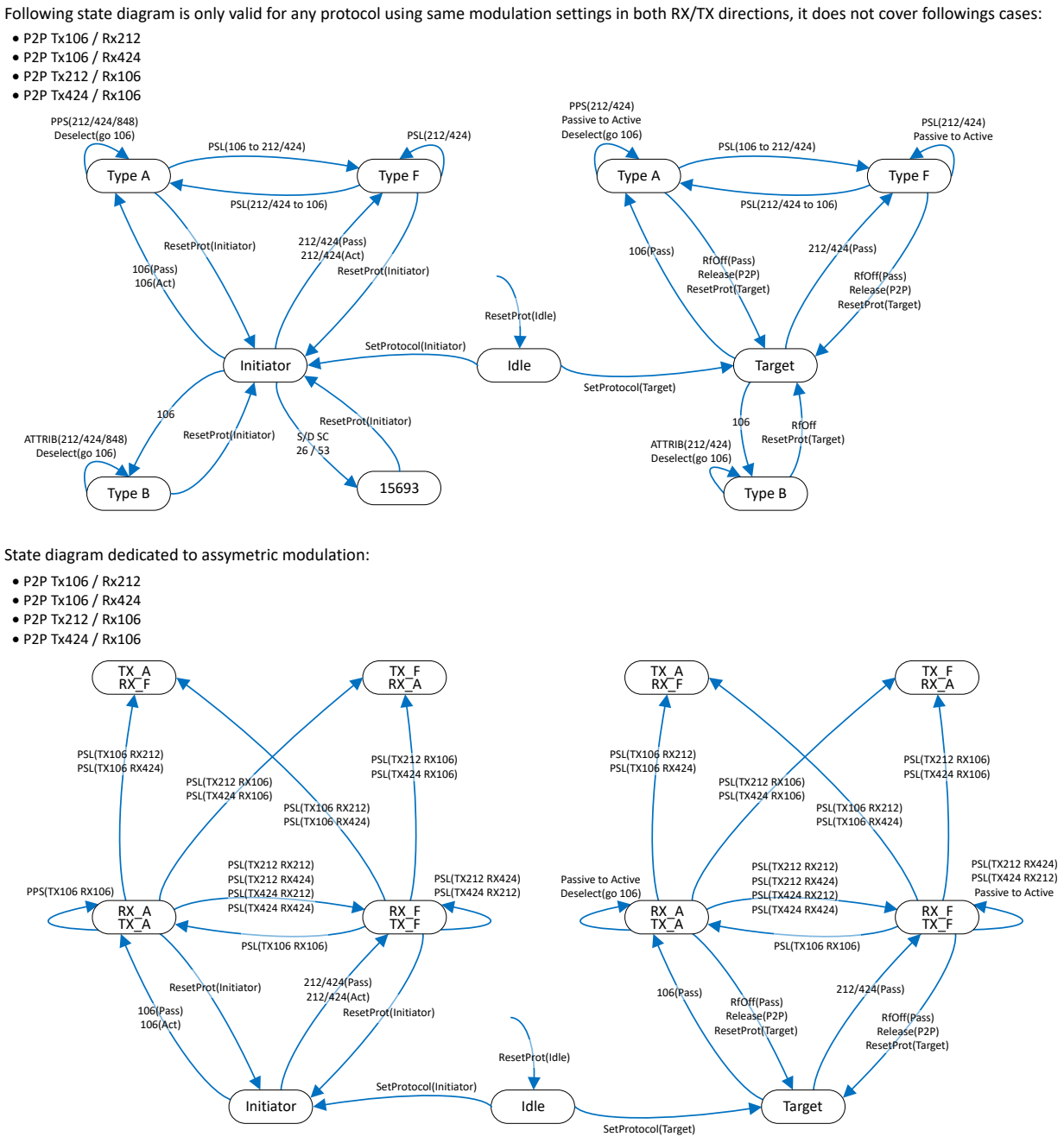

Figure 1. RF transitions diagram

PN7160 can go to different states, but cannot jump to a state to which no link is defined, which makes the solution more robust. The transitions are defined as below:

- BOOT
  - Called at boot time
  - Basic initialization of CLIF (for example, SMU_ANA_TX_STANDBY_REG)
- INITIATOR
  - Called at the beginning of the reader phase
  - Initialization common Reader/Initiator mode settings
- TARGET
  - Called when external field is detected and the CE/P2P Target is active
  - Initialization of common CE/Target mode settings
- TECHNO_I_RX_X, TECHNO_I_TX_X, TECHNO_T_RX_X, TECHNO_T_TX_
  - Initialization of common technology-dependent settings for transmitter and receiver
- BR_XXX
  - Initialization of bit rate-specific settings for transmitter and receiver for all different technologies / modes

The list of transition IDs is shown in Table 2 below:

Table 2. Transition ID values

Name	ID
RF_CLIF_CFG_BOOT	**00**
RF_CLIF_CFG_INITIATOR	**06**
RF_CLIF_CFG_TARGET	**08**
RF_CLIF_CFG_I_PASSIVE	**0C**
RF_CLIF_CFG_I_ACTIVE	**10**
RF_CLIF_CFG_T_ACTIVE	**12**
RF_CLIF_CFG_TECHNO_T_RXF	**1C**
RF_CLIF_CFG_TECHNO_I_RXF_A	**22**
RF_CLIF_CFG_TECHNO_T_RXA_P	**24**
RF_CLIF_CFG_TECHNO_T_TXB	**28**
RF_CLIF_CFG_TECHNO_T_TXF_P	**2C**
RF_CLIF_CFG_BR_106_T_RXA	**34**
RF_CLIF_CFG_BR_212_T_RXA	**36**
RF_CLIF_CFG_BR_424_T_RXA	**38**
RF_CLIF_CFG_BR_848_T_RXA	**3A**
RF_CLIF_CFG_BR_106_I_RXA_P	**3C**
RF_CLIF_CFG_BR_212_I_RXA	**3E**
RF_CLIF_CFG_BR_424_I_RXA	**40**
RF_CLIF_CFG_BR_106_T_RXB	**44**
RF_CLIF_CFG_BR_212_T_RXB	**46**
RF_CLIF_CFG_BR_424_T_RXB	**48**
RF_CLIF_CFG_BR_848_T_RXB	**4A**
RF_CLIF_CFG_BR_106_I_RXB	**4C**
RF_CLIF_CFG_BR_212_I_RXB	**4E**

Table 2. Transition ID values...*continued*

Name	ID
RF_CLIF_CFG_BR_424_I_RXB	**50**
RF_CLIF_CFG_BR_212_T_RXF	**56**
RF_CLIF_CFG_BR_212_I_RXF_P	**5E**
RF_CLIF_CFG_BR_424_I_RXF_P	**60**
RF_CLIF_CFG_BR_106_I_RXA_A	**62**
RF_CLIF_CFG_BR_848_T_TXA	**70**
RF_CLIF_CFG_BR_106_I_TXA	**72**
RF_CLIF_CFG_BR_212_I_TXA	**74**
RF_CLIF_CFG_BR_424_I_TXA	**76**
RF_CLIF_CFG_BR_848_I_TXA	**78**
RF_CLIF_CFG_BR_106_I_TXB	**82**
RF_CLIF_CFG_BR_212_I_TXB	**84**
RF_CLIF_CFG_BR_424_I_TXB	**86**
RF_CLIF_CFG_BR_212_I_TXF	**94**
RF_CLIF_CFG_BR_424_I_TXF	**96**
RF_CLIF_CFG_BR_106_T_TXA_A	**98**
RF_CLIF_CFG_BR_212_T_TXF_A	**9A**
RF_CLIF_CFG_BR_424_T_TXF_A	**9C**

The registers can be one to four bytes long. As an example, Figure 2 below shows the register *CLIF_ANA_TX_AMPLITUDE_REG* in transition *RF_CLIF_CFG_TARGET* to 0xF3F30000.

Note: *The byte order for the register value is defined as Little Endian, meaning the LSByte is written first (LSB to MSB).*

The order of the different bytes is as follows (32 bits):

[7:4] [3:0] [15:12] [11:8] [23:20] [19:16] [31:28] [27:24]

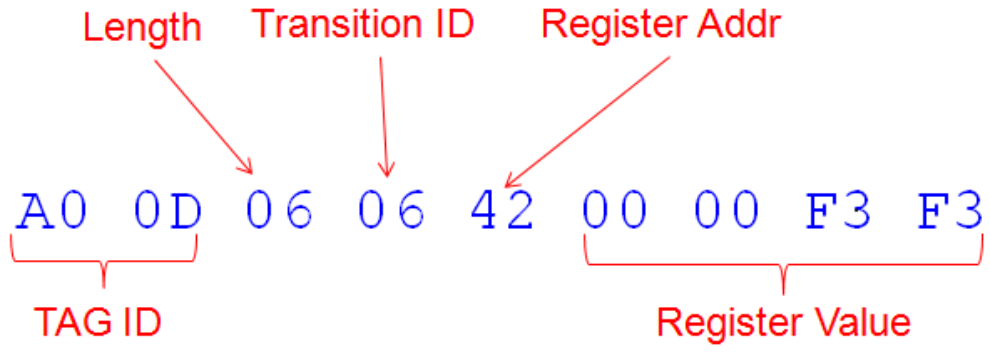

Figure 2. Example of transition ID

3 PN7160 RF Settings Command Builder

NXP offers a tool, which may help to create a dedicated NCI command. The tool is available under [3].

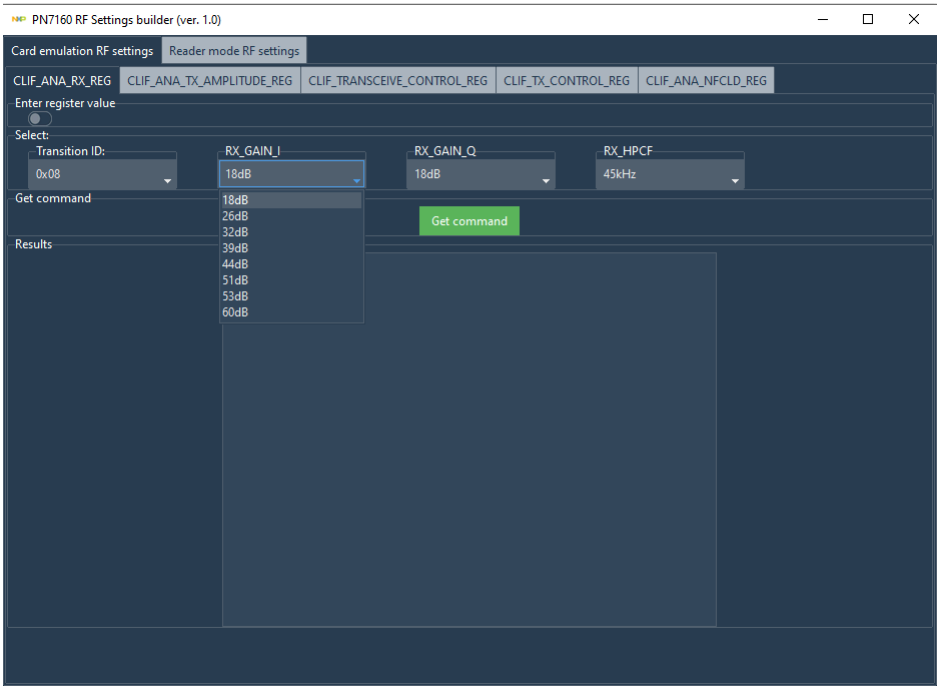

Figure 3. PN7160 RF Settings Command Builder

The tool contains most of the relevant RF registers and its output is in "MCUXpresso" or "Android" NCI format.

A dedicated NCI command is directly generated based on the registers default values described in Section 4.1. See an example in Figure 4

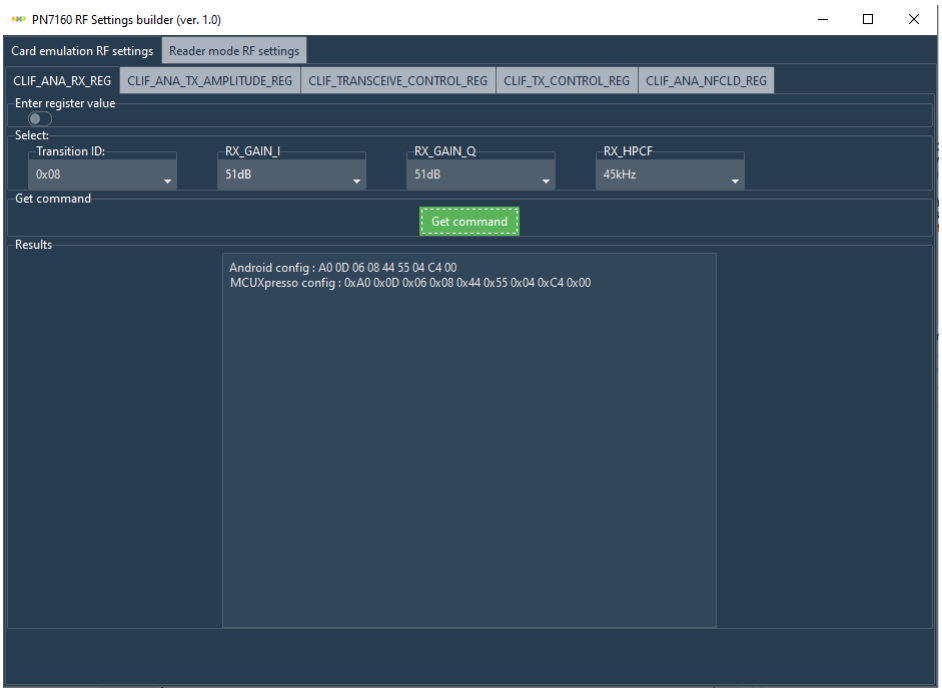

Figure 4. NCI command based on the default value

The tool also offers putting a custom register value as shown below. Then, the NCI command is generated based on the "custom" entered register value. See an example in Figure 5. Keep in mind that some register values must not be changed. If possible, it is recommended to generate the NCI command based on the default value.

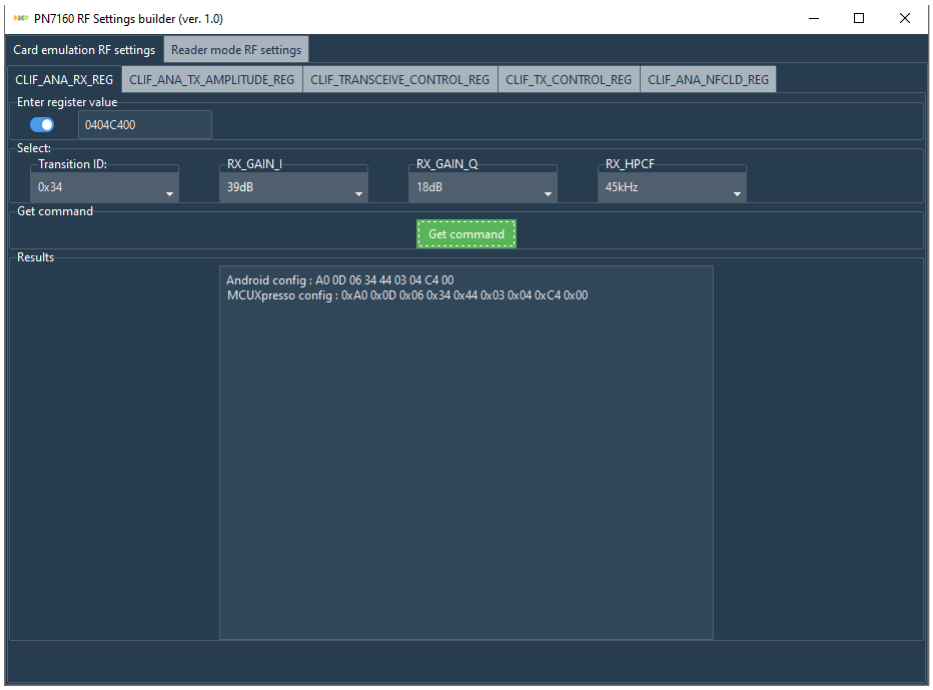

Figure 5. NCI command based on the custom value

4 Register settings configuration

4.1 Registers default values

RF settings influence the performance of the system in reader or card emulation mode by changing the phase, amplitude, and shaping of the TX and RX path signal. Their default value and the way to optimize them are strongly dependent on the type of antenna used (size, topology, characteristics) and the design of the matching/tuning network.

Most of the registers values must not be changed, once they were already programmed by NXP. The registers that may be customized are explained in the subsequent chapters.

The NCI command to be used for updating those registers values is the CORE_SET_CONFIG_CMD (see [1]) which is:

→ 20 02 [length] [number of parameters] [bytes of parameter n°1] [bytes of parameter n°2]… [bytes of parameter n°N]

Example: [20 02 0A 01 A0 0D 06 08 42 00 00 FF FF]

- Length = 10 (0x0A)
- Number of parameters = 1 (0x01)
- Parameter TX_Amplitude on RF_CLIF_CFG_TARGET transition = A0 0D 06 08 42 00 00 FF FF

The complete list of the RF registers and their default values can be found in Annex 3.

4.2 How to optimize register settings

This chapter explains the procedure to optimize the registers in all configurations (card, reader modes). The procedure shall be, as much as possible, independent of the antenna characteristics.

The procedure is generally based on the EMVCo test bench methodology. Refer to Book D for EMV Contactless Communication Protocol Specification [5] chapter 3.4 and 4, to get more insight on Load Modulation definition, mechanisms, and timing constraints.

For more clarity, each register setting procedure follows the below plan:

- Modified parameter (which register bits and their meaning)
- Measurement method
- Target (or acceptance criteria)

Before starting the fine-tuning of this register, we suggest disabling the dynamic LMA (DLMA) feature (by default DLMA is enabled).

To disable DLMA, use the following NCI command: [20, 02, 10, 01, A0, AF, 0C, 03, C0, 80, A0, 00, 03, C0, 80, A0, 00, 00, 08]

5 Configuring registers in card mode

The following registers with different transitions ID, improve the card emulation mode performance in type A, B, and F, by influencing the load modulation amplitude (LMA) and the sidebands levels on the TX signal path.

This tuning must ensure a correct operation and interoperability between PCD and PICC products. Performance for high distance communication (Low field strength) must be checked against readers like Pegoda and payment readers.

In addition to the readers, the following test benches shall be used to get the best performance:

1. EMVCo test bench to define minimum functionality for PICC and PCD usage vs. RF powering, frames, timings, Type A, Type B commands.
2. ISO test bench to verify the operation of a PICC vs. ISO/IEC 14443-2, and ensures independency vs. coupling effect.

5.1 CLIF_TX_CONTROL_REG

Firstly, the load modulation mode (for card mode) has to be selected via the following register:

Table 3. Load modulation modes register for card mode

Register name	Transition ID	Register Address
CLIF_TX_CONTROL_REG	0x08	0x37

Register example: A0 0D 06 08 37 **XX** 76 00 00

The corresponding value for **XX** are the following:

Table 4. Load Modulation generation modes register values

Mode	Register Value
Mode 1	0x28
Mode 2	0x08
Mode 3	0x48

5.2 Card mode ALM phase

5.2.1 Register definition

The card mode ALM phase is the first parameter to configure in order to adjust the DLL clock phase offset between the RX and TX paths.

Based on the clock offset, the signal emitted at the second half of the antenna is in phase with the emitted field from the reader. Therefore, its impact on the amplitude of the reader field is different, and can drastically impact the corresponding load modulation.

The tag ID of this register is 0xA0 3A and it allows configuring default phase settings for Field-On/TypeA/TypeB/TypeF (2 bytes each) in 5 degrees steps:

→ A0 3A 08 Field-ON TypeA TypeB TypeF

To set the phase value, take a value in HEX and convert to DEC, this is the value of the phase in degrees (for example: 0x002D = 45 degrees, 0x0163 = 355 degrees).

Inverting the bytes for the NCI command:

→ 45° = A0 3A 08 2D 00 2D 00 2D 00 2D 00

→ 355° = A0 3A 08 63 01 63 01 63 01 63 01

It is recommended to set all types including field-on with the same value.

Default value: A0 3A 08 A5 00 A5 00 A5 00 A5 00

5.2.2 Register setting procedure

Parameter: CLOCK_CONFIG_DLL_ALM

Value range: 00h to 163h (NCI 00 00 to 63 01)

Measurement process:

1. Set the 0xA0 3A register to the desired clock phase value
2. Run EMVCo *CA131* (or NFC Forum *9.1.3.1 Load Modulation amplitude for NFC-A* poller 0) test @ 2 cm
3. Get LMA values
4. Get and check the waveform screenshot
5. If the LMA is not the maximum amplitude, change the clock phase value

Target:

1. Select the clock phase value for which the waveform is the best sine wave
2. Confirm the optimal setting by using a Pegoda (or payment) reader and getting the best distance

5.2.3 Measurement example

The graphs below show a selection of measurements done on a reference design. The best sine wave allows selecting the right clock phase.

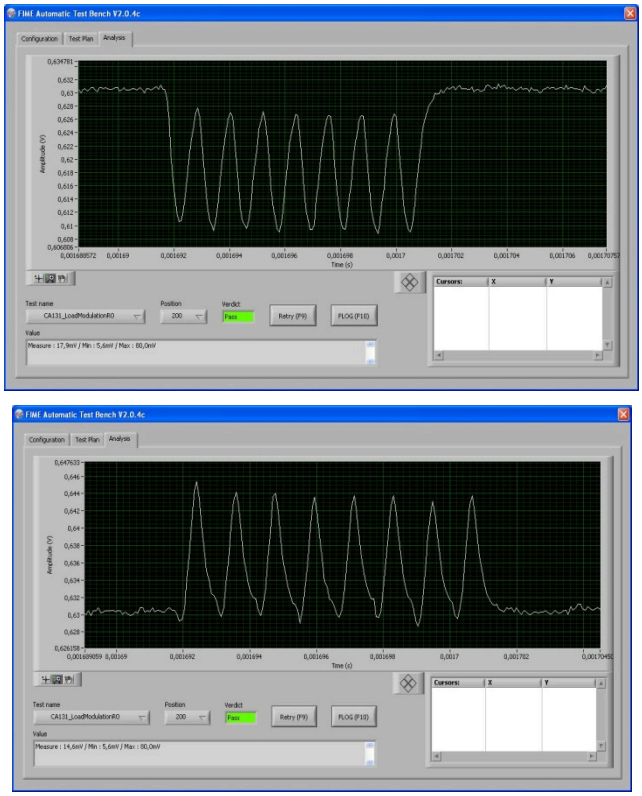

Figure 6. Example of correct EMVCo waveforms

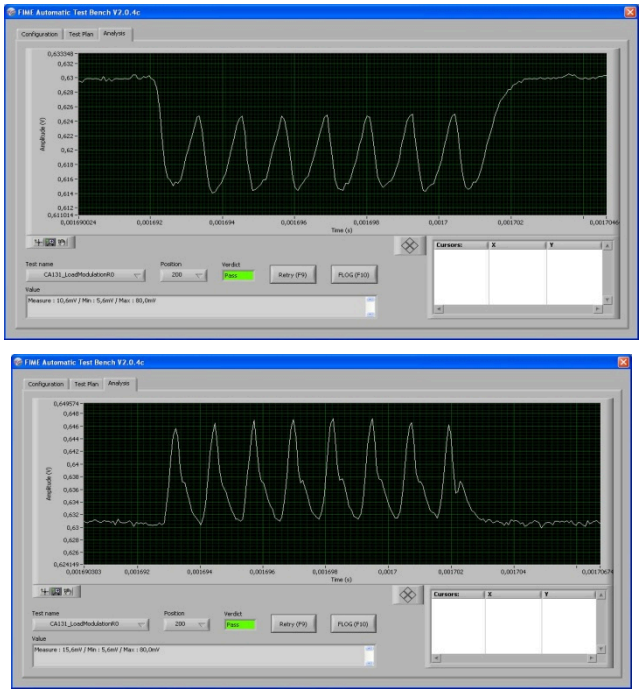

Figure 7. Example of bad EMVCo waveforms

5.3 CLIF_ANA_TX_AMPLITUDE_REG

5.3.1 Register definition

CLIF_ANA_TX_AMPLITUDE_REG is the second register to configure.

[27:24] and [19:16] adjust the N-MOS transistor conductance value applied during nonmodulated phases (CW - Continuous Wave) and modulated phase (MOD - Modulation phase) respectively. 0001b means minimum conductance (maximum impedance), and vice versa (*note that value 0000b shall not be used*.).

[9:8] adjust the load modulation amplitude by choosing the amplitude of the output signal generated at PN7160 TX pin (*it is recommended to use the maximum value 00b*).

Based on these adjustments, the load modulation shape can be improved to comply with the targeted standards, including interoperability.

Table 5. CLIF_ANA_TX_AMPLITUDE_REG register setting for card mode

Bit	Symbol	Description
[31:28]	Internal use	Must not be modified
[27:24]	**TX_GSN_CW_CM**	**gsn setting @ continuous wave in card mode**
[23:20]	Internal use	Must not be modified
[19:16]	**TX_GSN_MOD_CM**	**gsn setting @ modulation in card mode**
[15:10]	Internal use	Must not be modified
[9:8]	**TX_CW_AMPLITUDE_ALM_CM**	**Set amplitude of unmodulated carrier @ card mode [00] => Amplitude is TVDD – 150 mV [01] => Amplitude is TVDD – 250 mV [10] => Amplitude is TVDD – 500 mV [11] => Amplitude is TVDD – 1000 mV**
[7:3]	TX_RESIDUAL_CARRIER	set Load Modulation amplitude (0=100%, 1F = 0%)
[2 :0]	Internal use	Must not be modified

TX amplitude register has different transitions available. To assure a good performance, it is important to keep the same value for all transitions ID. So, if you modify the TX amplitude for one transition ID this value must be updated for other transitions IDs.

Table 6. Fine-tuning register TX amplitude for card mode

Register name	Transition ID	Register Address
CLIF_ANA_TX_AMPLITUDE_REG	0x08	0x42

5.3.2 Register setting procedure

- **Adjusting CW GSN to get optimal field strength (best RX sensitivity)**

Parameter: TX_GSN_CW_CM

Value range: 1h to Fh

Measurement process:

1. Run EMVCo *CA121* (or NFC Forum 9.1.2.1 Modulation Polling Device to Listening Device at Limit Condition - NFC-A poller 0) test @ 4 cm (or 5 cm if no proven results)
2. Read distance on Pegoda.

Target:

1. Select the range of CW for which *CA121* passes (OK).
2. Get the best CW value, which provides the highest distance.

- **Adjusting MOD GSN to get optimal reader distance (optimal LMA on TX)**

Keep the best value found in the previous test for CW GSN.

Parameter: TX_GSN_MOD_CM

Value range: 1h, 3h, 9h, or Fh

Measurement process:

1. Read distance on reader
2. Perform EMVCo test *CA131* (or NFC Forum 9.1.3.1 Load Modulation amplitude for NFC-A poller 0) test @ 2 (LMA) and get value.

Target:

1. Get MOD for highest distance, and confirm
2. Confirm LMA passes for the selected MOD value and with 3 cm and 4 cm.

5.3.3 Measurement examples

The graphs below show a selection of measurements regarding distance, MinPowerLevel, and LMA. The best [CW, MOD] can be selected accordingly:

[CW, MOD] = (1,6), but a range within (1,6)(1,6) can be considered in case of interoperability issues.

"MOD"= 0x3:

"CW"	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
LMA [mVpp]	9	7	6.5	6.5	6	6	6	5.5	5.5	5.5	5.5	5	5
CA121	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	KO	KO

"MOD"= 0x6

"CW"	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
LMA [mVpp]	6.5	6.5	6	6.5	6.5	5.5	5.5	5.5	5	5	5	5	4.5
CA121	OK	OK	OK	OK	OK	OK	OK	OK	KO	KO	KO	KO	KO

"MOD"= 0x9

"CW"	0x3	0x4	0x5	0x6	0x7	0x8	0x9	0xA	0xB	0xC	0xD	0xE	0xF
LMA[mVpp]	7	6.5	6	6	5.5	5.5	5.5	5	5	5	5	4.5	4.5
CA121	OK	OK	OK	OK	OK	OK	KO	KO	KO	KO	KO	KO	KO

Figure 8. Example of MinPowerLevel results

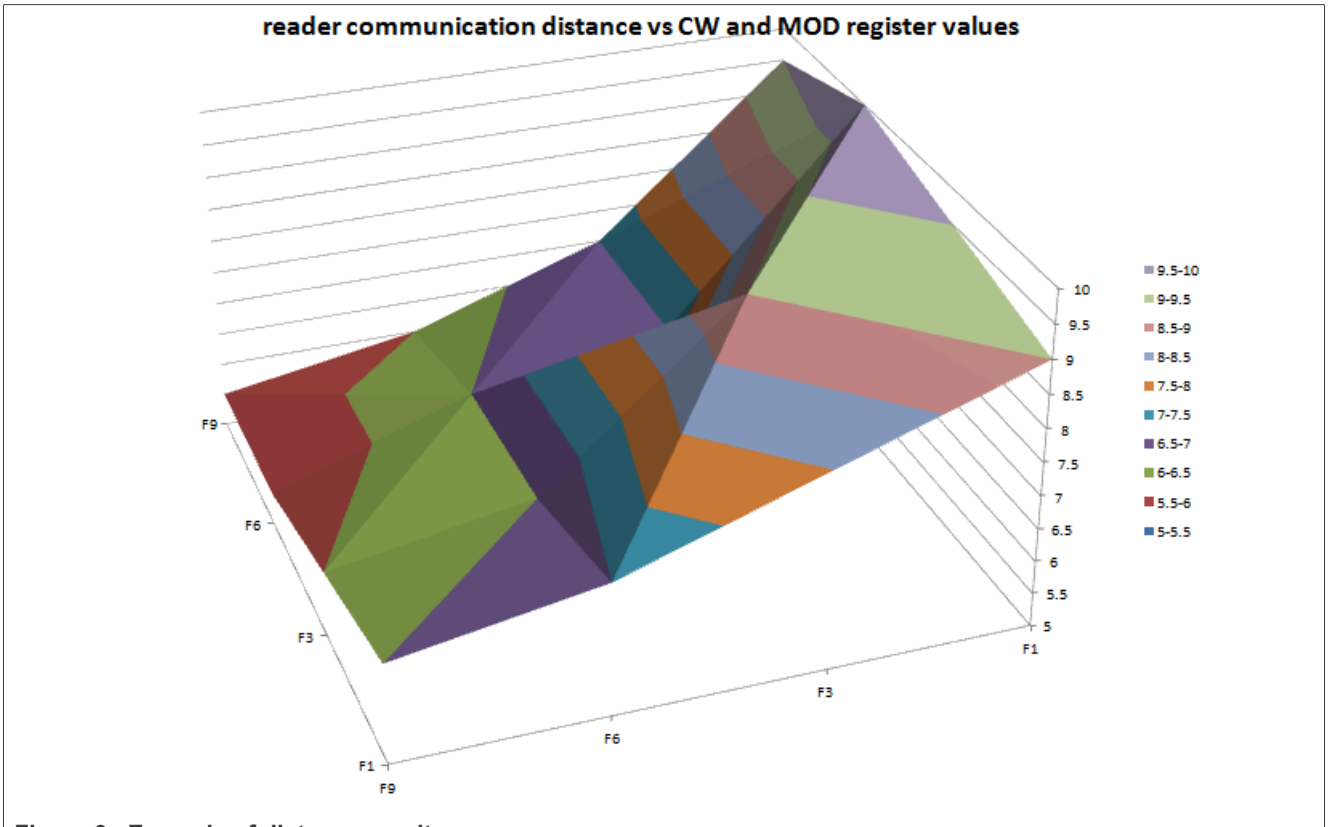

Figure 9. Example of distance results

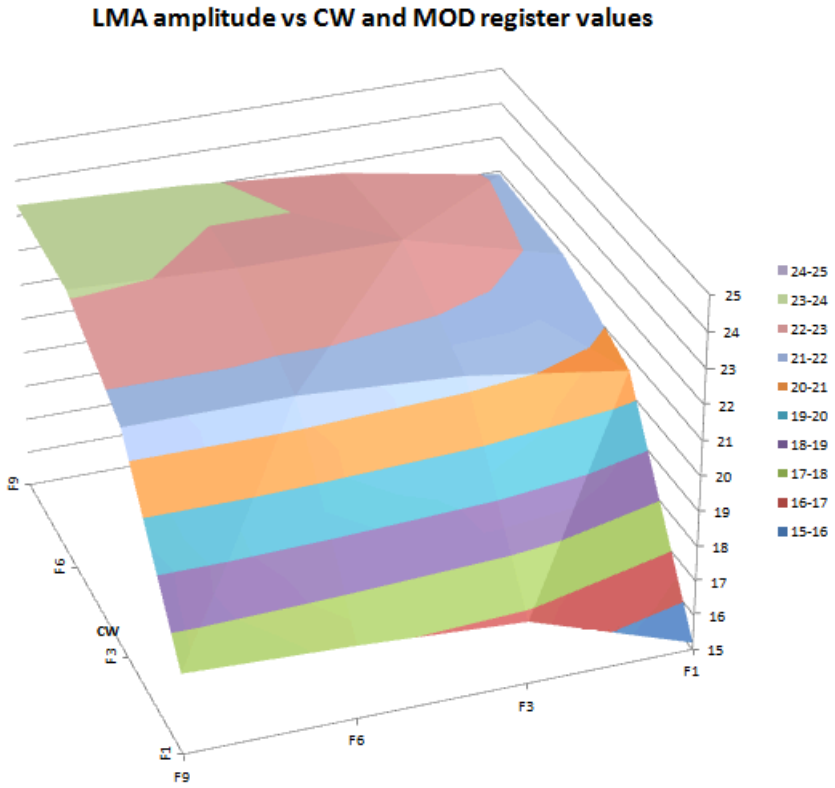

Figure 10. Example of LMA results

5.3.4 Schematics providing principle

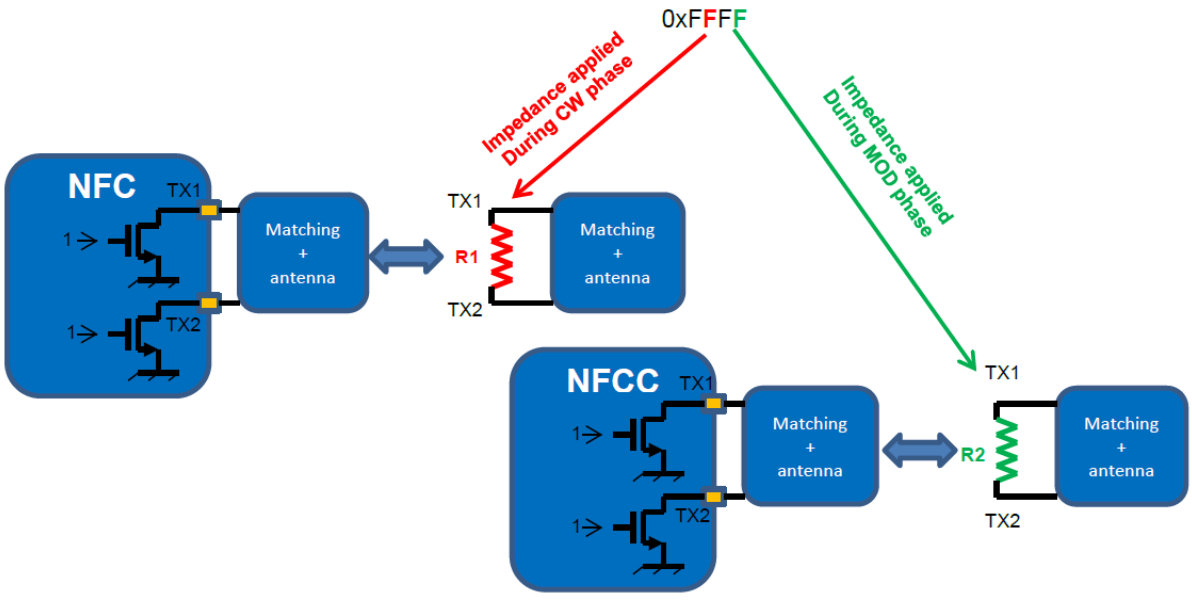

Figure 11. TX_GSN_CW_CM / TX_GSN_MOD_CM principle

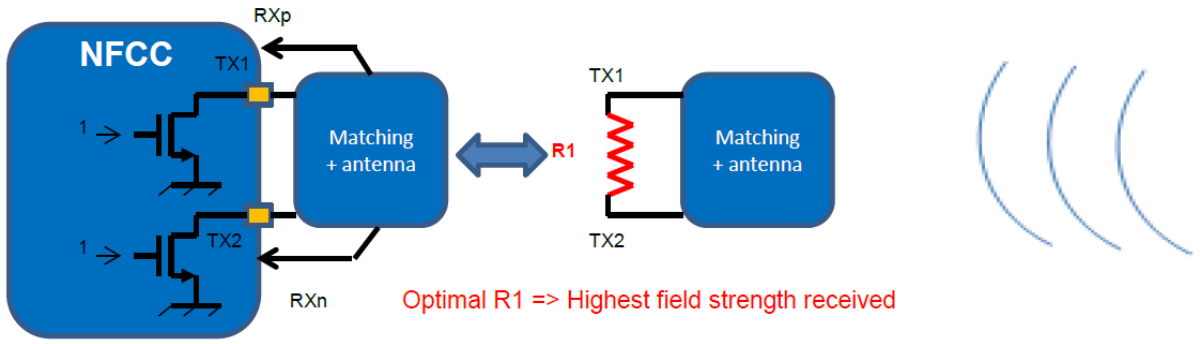

Figure 12. Settings principle optimal R1

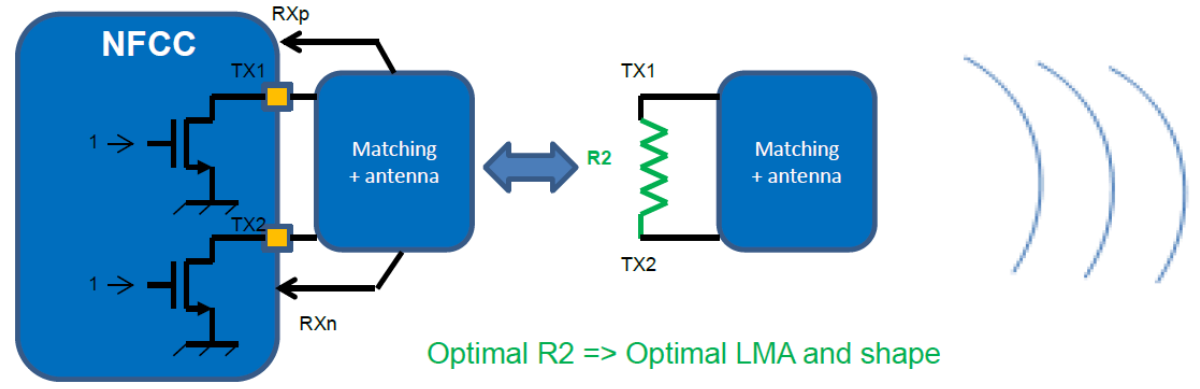

Figure 13. Settings principle optimal R2

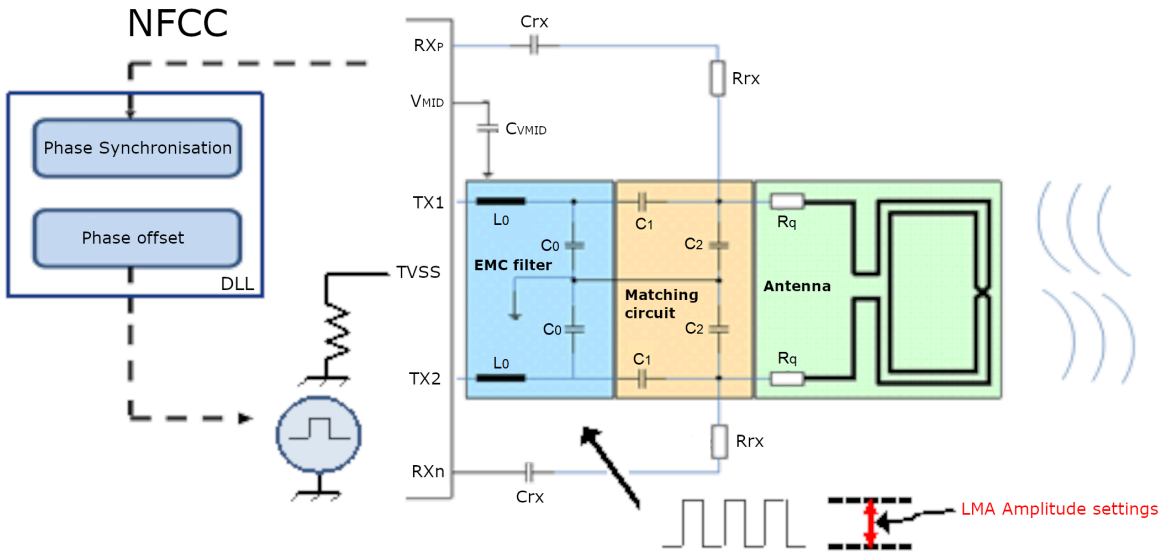

Figure 14. TX_CW_AMPLITUDE_ALM_CM principle

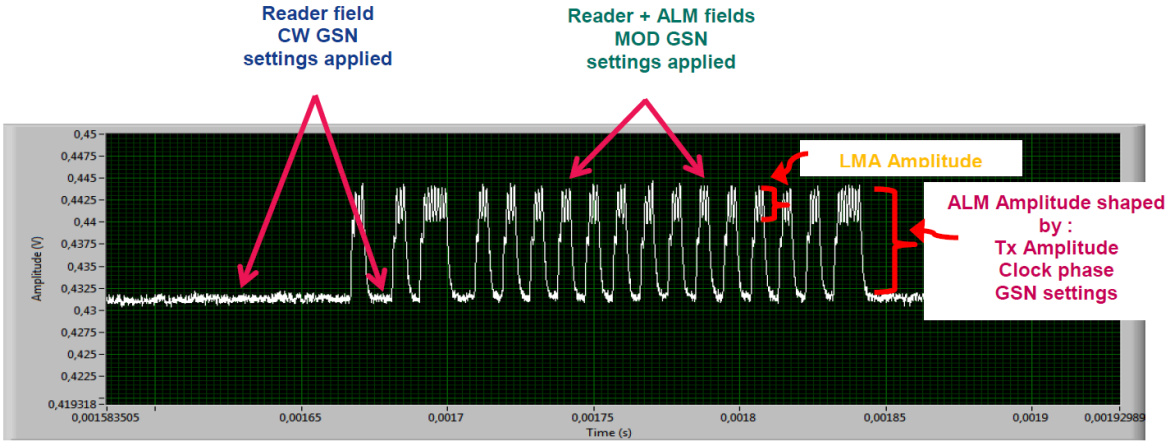

Figure 15. Settings applied during the CW and MOD phases

5.4 CLIF_TRANSCEIVE_CONTROL_REG

5.4.1 Register definition

CLIF_TRANSCEIVE_CONTROL_REG can be adjusted to meet FDT requirement.

Table 7. CLIF_TRANSCEIVE_CONTROL_REG register for card mode

Register name	Transition ID	Register Address
CLIF_TRANSCEIVE_CONTROL_REG	0x24	0x03

Table 8. CLIF_TRANSCEIVE_CONTROL_REG register setting for card mode

Bit	Symbol	Description
[7:0]	**TX_BITPHASE**	**Defines the number of 13.56 MHz cycles used for adjustment of tx_wait to meet the FDT.**

5.4.2 Register setting procedure

Parameter: TX_BITPHASE

Value range: 0h to FFh. A variation of +1 in the register means a shift of +1/13.56Mhz s on the FDT time.

Measurement process:

1. Run EMVCo *CA144.200* (No analogy with NFC Forum test) FDT value.

Target:

1. The result of the $FDT_{A,PICC,ANTICOLLISION}$ must be between 9 etu + 84/Fc + 150 ns and 9 etu + 84/Fc + 200 ns to achieve the best performances in combination tests.

5.5 CLIF_ANA_NFCLD_REG

5.5.1 Register definition

CLIF_ANA_NFCLD_REG can be adjusted to define the RF level detector level, i.e. the level of the external RF field seen by PN7160. Indeed, in some cases, the external RF field might not be fully turned OFF, and still detected to be present.

Table 9. Other fine-tuning register for card mode

Register name	Tag ID
CLIF_ANA_NFCLD_REG	0xA0 38

TagID A038: Sets the NFCLD for RF_ON, RF_OFF, P2P, RSSI_METHOD:

→ **Default value:** A0 38 04 14 0B 0B 00 (RSSI_METHOD must be set to 00)

1. Start with the value RF_OFF: 1h.
2. Run EMVCo *CA112.200* (or/and NFC Forum 9.1.1.12 Power On) and *CA113.200* (or NFC Forum 9.1.1.12 Power OFF) tests.
3. If the test is FAIL, increase the RF_OFF +1 until PASS the test.
4. Set P2P value as the same as RF_OFF value

5.5.2 Register setting procedure

Parameter: RF_ON

Value range: 0h to 3Fh

Default value: 14h

Measurement process:

1. Starting with a default value of 14h
2. Using an ISO Test bench start from 0 A/m to generate a very small field strength. Increase the field strength of the ISO PCD until the device gives a field ON notification (NCI event "61070101" RF_FIELD_INFO_NTF[field On]).
3. The first field ON notification must happen when the field strength of the ISO test bench is 300-350 mA/m(rms).
4. If field ON notification is received before 300 mA/m (rms), RF ON must be increased. field ON notification is received after 350 mA/m (rms) RF ON must be decreased.

Parameter: RF_OFF and P2P (both have the same value)

Value range: 0h to 3Fh

Default value: 0Bh

5.6 AGC_INPUT_REG

When a signal is present at the RX level, the AGC regulates the signal at a certain level Vref. To improve the convergence of the AGC, a starting point can be defined on the AGC_INPUT_REG.

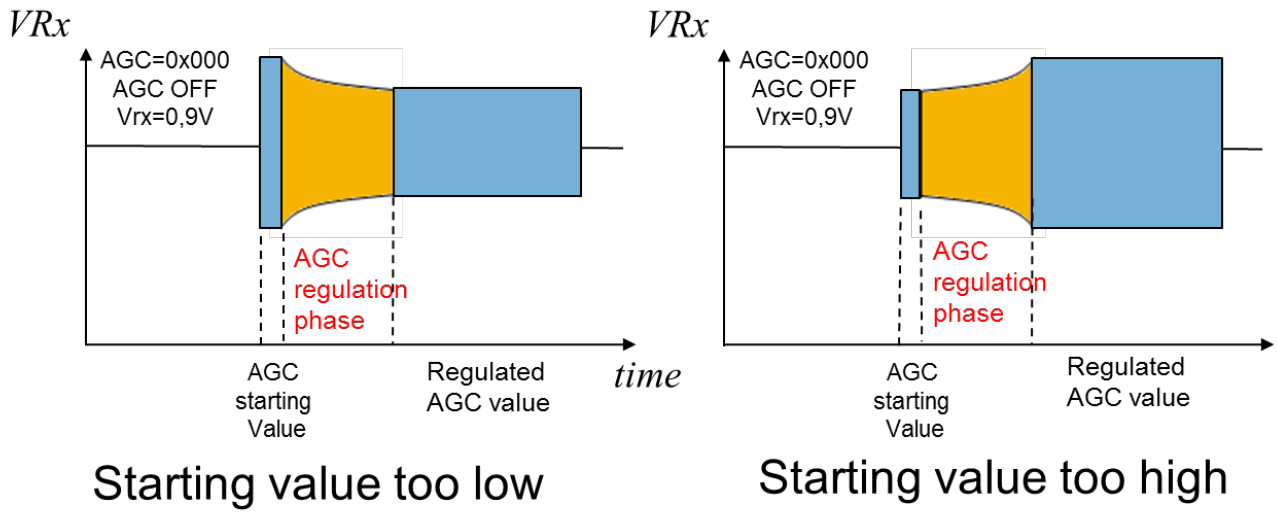

Figure 16. AGC_INPUT_REG

In case of issue during an IOT test, example transaction takes 1 or 2 s to be completed, reducing the AGC starting value can improve the reception of the NFCC.

Table 10. CLIF_AGC_INPUT_REG register for card mode

Register name	Transition ID	Register Address
CLIF_AGC_INPUT_REG	0xC2	0x35

Table 11. CLIF_AGC_INPUT_REG register setting for card mode

Bit	Name	Description
[9:0]	AGC_CM_VALUE	Static AGC value used for card mode. From 0 (less attenuation) to 0x380 (higher attenuation)

Recommendation is to try the following values A0, 0D, 06, C2, 35 + 4 bytes value:

- 00 3D 00 03 (AGC input CM set to 256 dec)
- 80 3C 00 03 (AGC input CM set to 128 dec)
- 40 3C 00 03 (AGC input CM set to 64 dec)

5.7 Card Mode settings in DEVICE OFF

For devices using an Xtal to provide the clock for the NFC chip, the card mode settings are the same for DEVICE ON and DEVICE OFF operation.

For devices using an external clock and which cannot provide a clock during DEVICE OFF, the procedure to tune the card mode settings are explained here.

Using the following register (0xA0 29), we can set the following parameters specific for DEVICE OFF (default value: A0 29 17 1A 07 00 1D 00 02 00 1D 00 02 00 40 F3 F3 00 43 F3 F3 38 70 00 00 00)

→ A0 29 17 YY 07 AA AA AA AA BF BF BF BF TA TA TA TA TB TB TB TB ZZ 70 00 00 XX

- The TxLDO value XX
- The card mode ALM phase YY
- TX driver used to send the response ZZ
- The TX Amplitude register on TA TA TA TA TB TB TB TB
- The AGC input register AA AA AA AA BF BF BF BF

The first parameter to configure is the TxLDO value:

Table 12. TxLDO voltage select

XX Value	TxLDO
0	3 V
1	3.3 V
2	3.6 V
3	4.5 V
4	4.75 V
5 or 6 or 7	5.25 V
8	2.7 V
9	3.9 V
10	4.2 V
11	4.7 V
12 or 13 or 14 or 15	5 V

The TxLDO value must be set per the maximum value provided on pin VUP-150mV.

Ex1: The device has no DC-DC, and VBAT (3.85 V) is connected to VUP. In this case, TxLDO can be 3.6 V or less.

Ex2: The device has a DC-DC (Vout=5.4 V) connected to VUP, in this case TxLDO can be 5.25 V or less.

The second parameter is the card mode ALM clock phase offset between the RX and TX paths must be set for DEVICE OFF. Like the process described in Section 5.2, the best phase for card mode in DEVICE OFF operation must be found.

Table 13. CLK_MAN value

YY Value	TxLDO
18h	0°
19h	45°
1Ah	90°
1Bh	135°
1Ch	180°
1Dh	225°
1Eh	270°
1Fh	315°

The third parameter that can impact the performance in card mode is the TX driver used to transmit the response during device off operation.

In DEVICE OFF operation, the device must recover the clock from the RF field of the reader and send the responses using one of the TX drivers. Depending on the connections, the clock recovery can be optimized if the TX1 or TX2 is used.

- ZZ = 28: TX1 driver to transmit the responses
- ZZ = 38: TX2 driver to transmit the responses

To decide which value must be used, it is recommended to test both values 38h and 28h, in front of a commercial reader (or EMVCo test bench). Keep the value, which provided bigger communication distance.

The TX amplitude values can be chosen for type A ("TA TA TA TA") and type B/F ("TB TB TB TB").

The procedure to choose the TX amplitude value is the same as the DEVICE ON procedure in Section 5.3

Similar as the use of AGC_INPUT in DEVICE ON: In case of slow response times, the AGC_INPUT values can be chosen for some RX optimization in type A ("AA AA AA AA") and type B/F ("BF BF BF BF").

The AGC input value in card mode is defined on bits [0:9].

The recommendation is to try the following NCI formatted values for both types:

- 00 1D 00 02: [0:9] = 100h → AGC input CM set to 256
- 80 1C 00 02: [0:9] = 80h → AGC input CM set to 128
- 40 1C 00 02: [0:9] = 40h → AGC input CM set to 64

5.8 CLIF_ANA_RX_REG

5.8.1 Register definition

CLIF_ANA_RX_REG can be fine-tuned to improve the analog down-sampling and baseband amplification of the card response before it is processed by the digital block.

Table 14. CLIF_ANA_RX_REG address

Register name	Register Address
CLIF_ANA_RX_REG	0x44

[9:8]: Set the lower corner frequency of the BBA internal band-pass filter to reduce analog demodulation interferences.

Care:

- If the corner frequency is set too close or above the actual baseband signal frequency, the signal strength of the « useful » signal is dampened, leading to a loss of reading range. But at the same time it can also stabilize the reader performance → Tradeoff might be necessary.
- Furthermore, the RX_HPCF parameter influences the BBA amplification level (gain) → Higher HPCF gives lower gain (1-2 dB / per setting).
- For a reliable setting of the HPCF, the observation of the frequency spectrum of the BBA input should be available for the given design → Since not available, each setting must be evaluated by functional testing

[2:0] and [6:4]: Set the amplification level of the **B**ase **B**and **A**mplifier.

Care:

- The gain must be set in combination with the HPCF parameter for the optimization of the disturbances in the down-mixed RX signal.

Value range:

- High performance and sensitivity for max. reading range: 10b … 11b
  - Strongly depends on the SNR in the system
- Typical: 01b … 10b
- High robustness and stability but low reading range: 00b

Table 15. CLIF_ANA_RX_ REG register

Bit	Symbol	Description
[31:10]	Internal use	Must not be modified
[9:8]	**RX_HPCF**	**Lower Corner Frequency:** **00->45kHz,** **01->85kHz,** **10->150kHz,** **11->250kHz**
[6:4]	**RX_GAIN_Q**	**Gain Adjustment BBA:** **00->18 dB,** **01->26 dB,** **10->32 dB,** **11->39 dB** **100->44 dB** **101->51 dB** **110->53 dB** **111->60 dB**
[3]		**RFU**
[2:0]	**RX_GAIN_I**	**Gain Adjustment BBA:** **00->18 dB,** **01->26 dB,** **10->32 dB,** **11->39 dB** **100->44 dB** **101->51 dB** **110->53 dB** **111->60 dB**

Table 16. CLIF_ANA_RX_ REG transitions for card mode

Technology	Baud rate	Transition ID
Global	-	0x08
type A	106	0x34
	212	-
	424	0x38
	848	0x3A
type B	106	0x44
	-	-
type F	-	0x1C

Remark: For each communication type and baud rate, you must choose the right transition. In the table below, you find the transition, which corresponds to each tag type.

6 Configuring registers in reader mode

6.1 Pulse shape definitions

6.1.1 Type A

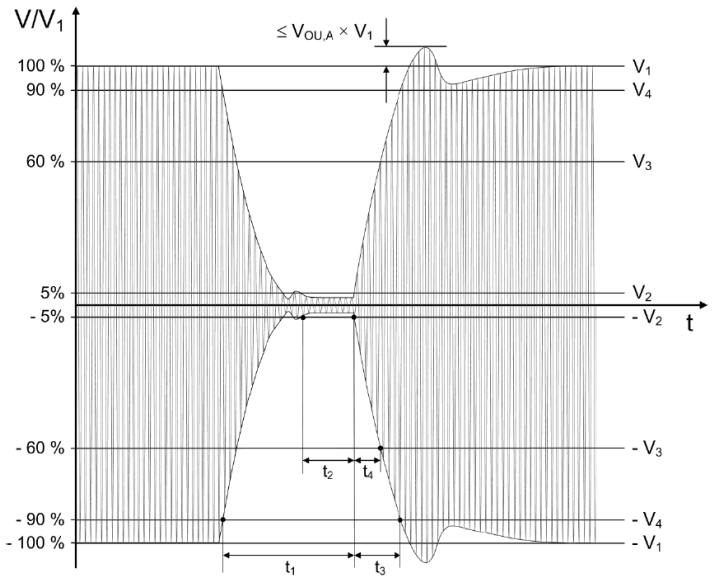

Figure 17. Pulse shape Type A in EMVCo

The time t1-t2 describes the time span in which the signal falls from 90% down below 5% of the signal amplitude.

The most critical time for rising carrier envelope is t4. It must be checked that the carrier envelope at the end of the pause reaches 60% of the continuous wave amplitude within 0.4 µs.

Ringing following the falling edge shall remain below Vou,A*V1.

Overshoots immediately following the rising edge shall remain within (1+/- Vou,A)*V1.

Refer to [5] to get t1, t2, t3, t4, and Vou,A values.

The following register can be fine-tuned to improve the shaping of the pulse in Type A and Modulation index in Type B.

6.1.2 Type B

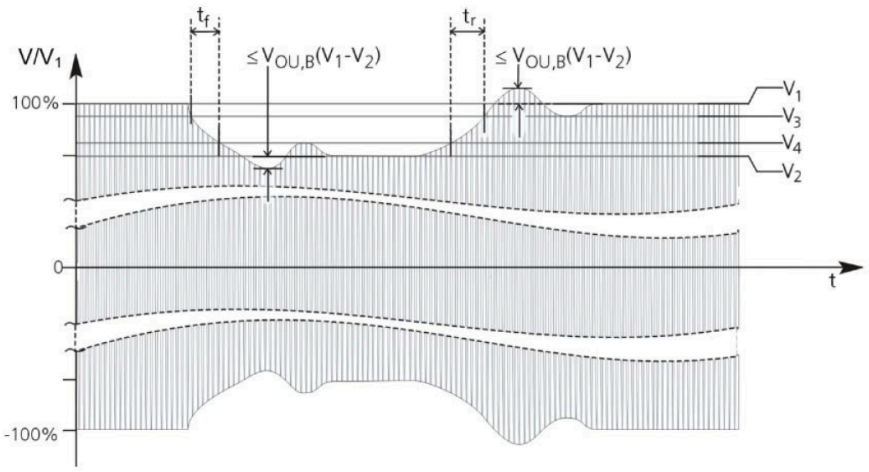

Figure 18. Pulse shape Type B in EMVCo

V1 is the initial value measured immediately before any modulation is applied by the reader while V2 is the lower value.

The modulation index (mi), V3 and V4 are defined as follows:

- mi = (V1-V2)/(V1+V2)
- V3 = V1 – 0.1*(V1-V2)
- V4 = V2 + 0.1*(V1-V2)

Refer to [5] to get the values of modi, tf, tr, and Vou,B.

6.2 CLIF_ANA_TX_AMPLITUDE_REG

6.2.1 Register definition

CLIF_ANA_TX_AMPLITUDE_REG is the register to configure several parameters of the transmission in reader mode.

Table 17. CLIF_ANA_TX_AMPLITUDE_REG address

Register name	Register Address
CLIF_ANA_TX_AMPLITUDE_REG	0x42

Table 18. CLIF_ANA_TX_AMPLITUDE_REG register for reader mode

Bit	Symbol	Description
[31:28]	**TX_GSN_CW_RM**	**gsn setting @ continuous wave in reader mode**
[27:24]	Internal use	Must not be modified
[23:20]	**TX_GSN_MOD_RM**	**gsn setting @ modulation in reader mode**
[19:14]	Internal use	Must not be modified
[13:12]	**TX_CW_AMPLITUDE_RM**	**Set amplitude of unmodulated carrier @ reader mode [00] => Amplitude is TVDD – 150 mV [01] => Amplitude is TVDD – 250 mV [10] => Amplitude is TVDD – 500 mV [11] => Amplitude is TVDD – 1000 mV**
[11:8]	Internal use	Must not be modified
[7:3]	**TX_RESIDUAL_CARRIER**	**Set amplitude of unmodulated carrier**
[2:0]	Internal use	Must not be modified

This register has different lengths depending on the transition ID used. The description of the register is the same, however for initiator the description go until bit 31, and for Type A,B, F212 and F424 the description go until bit 15.

Table 19. CLIF_ANA_TX_AMPLITUDE_REG transitions for reader mode

Technology	Baud rate	Transition ID
Initiator	All	0x06
type A	106	0x72
type B	106	0x82
type F	212	0x94
	424	0x96

The initiator transition defines some common parameters for all types A, B, F212 and F424.

For initiator transition the only parameter to be changed is TX_CW_AMPLITUDE_ALM_CM, this defines the amplitude of unmodulated carrier for all type A,B, F.

Table 20. CLIF_ANA_TX_AMPLITUDE_REG register TX_CW_AMPLITUDE_ALM_CM field

Bit	Symbol	Description
[13:12]	TX_CW_AMPLITUDE_ALM_CM	Set amplitude of unmodulated carrier @ reader mode [00] => Amplitude is TVDD – 150 mV [01] => Amplitude is TVDD – 250 mV [10] => Amplitude is TVDD – 500 mV [11] => Amplitude is TVDD – 1000 mV

For Type A, B, F212 and F424 transition the only parameter to be changed is TX_RESIDUAL_CARRIER.

Table 21. CLIF_ANA_TX_AMPLITUDE_REG register TX_RESIDUAL_CARRIER field

Bit	Symbol	Description
[7:3]	TX_RESIDUAL_CARRIER	It plays on the modulation index Type B. The higher the value, the higher the modulation index

This will defines the modulation index for type B, F212, F424 (the type A parameter does not need to be changed).

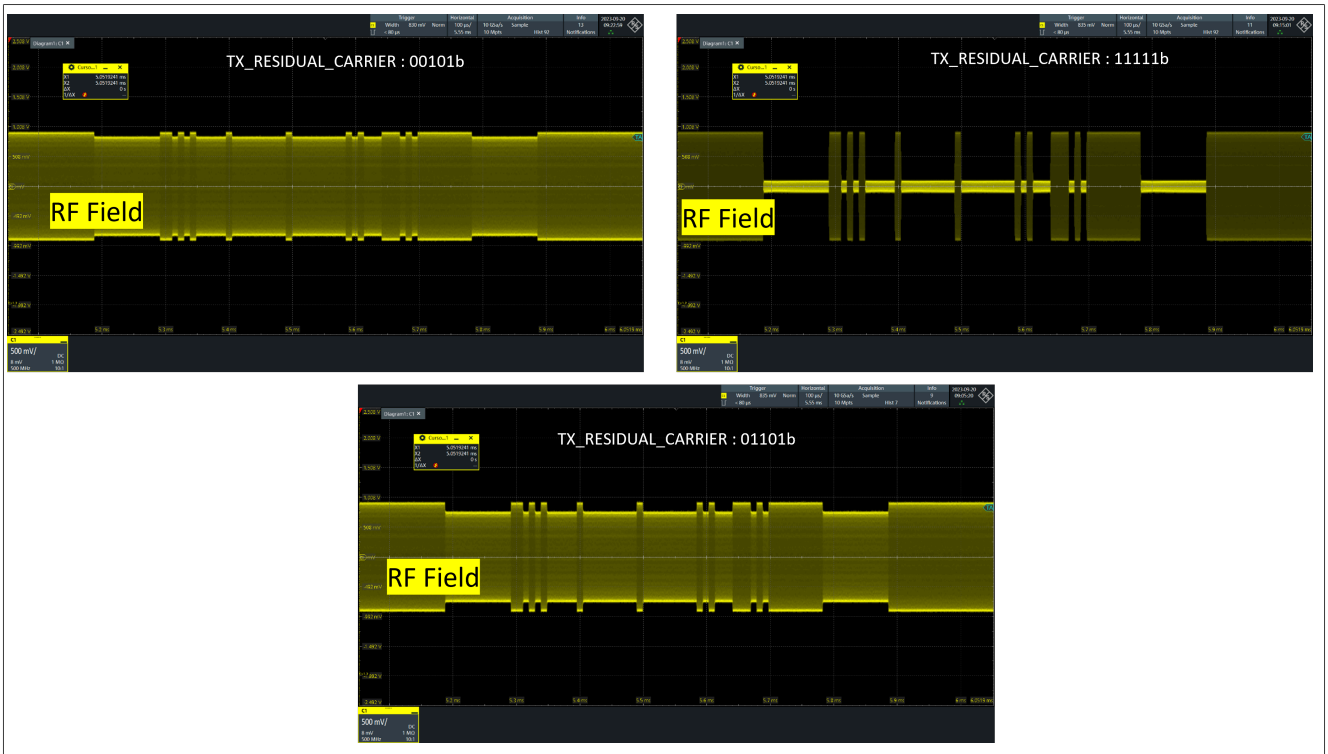

Figure 19. Modulation index adjustment

6.2.2 Register setting procedure

- **Adjusting TX_RESIDUAL_CARRIER**

Parameter: TX_RESIDUAL_CARRIER.

Values: 60h, 70h, 80h, **90h**, A0, B0, C0, C8.

Measurement process:

1. Use a PICC card and an oscilloscope to observe the modulation index Type B @ 0 cm, then 1 cm. Both must meet the standard.
2. Start with the default value (**90h**).
3. Increase the index with the value A0h, B0h, C0h and C8h.
4. Decrease the index with value 80h, 70h and 60h.

Target:

1. Select the value for which the modulation index is correct.

6.3 CLIF_ANA_TX_SHAPE_CONTROL_REG

6.3.1 Register definition

CLIF_ANA_TX_SHAPE_CONTROL_REG can be used to shape the TX transmission signal, by adjusting its rising/falling edge.

Table 22. CLIF_ANA_TX_SHAPE_CONTROL_REG address

Register name	Register Address
CLIF_ANA_TX_SHAPE_CONTROL_REG	0x4A

Table 23. CLIF_ANA_TX_SHAPE_CONTROL_REG register

Bit	Symbol	Description
[31:29]	Internal use	Must not be modified
[28 :24]	**TX_RESIDUAL_CARRIER_OV_PREV**	**Defines the value for the residual carrier for the period the overshoot prevention pattern is active.**
[23:18]	Internal use	Must not be modified
[17]	**TX_SET_BYPASS_SC_SHAPING**	**Bypasses switched capacitor shaping of the transmitter signal.**
[16:8]	Internal use	Must not be modified
[7:4]	**TX_SET_TAU_MOD_FALLING**	**Transmitter TAU setting for falling edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope.**
[3:0]	**TX_SET_TAU_MOD_RISING**	**Transmitter TAU setting for rising edge of modulation shape. In AnalogControl module the output signal is switched with the tx_envelope.**

Table 24. CLIF_ANA_TX_SHAPE_CONTROL_REG transitions

Technology	Baud rate	Transition ID
type A	106	0x72
type B	106	0x82
type F	212	0x94
	424	0x96

6.3.2 Register setting procedure

- **Adjusting TX_SET_TAU_MOD_RISING**

Parameter: TX_SET_TAU_MOD_RISING.

Values: 0h to Fh

Measurement process:

1. Use oscilloscope and zoom as depicted in the picture below.

Target:

1. Select settings for which the timing meets the specification.
2. 0 value means faster rising edges (potential overshoot, undershoot issue).
3. F value means smoother rising edges.

- **Adjusting TX_SET_TAU_MOD_RISING**

Parameter: TX_SET_TAU_MOD_ FALLING.

Values: 0h to Fh

Measurement process:

1. Use oscilloscope and zoom as depicted in the picture below.

Target:

1. Select settings for which the timing meets the specification.
2. 0h value means faster falling edges (potential overshoot, undershoot issue).
3. Fh value means smoother falling edges.

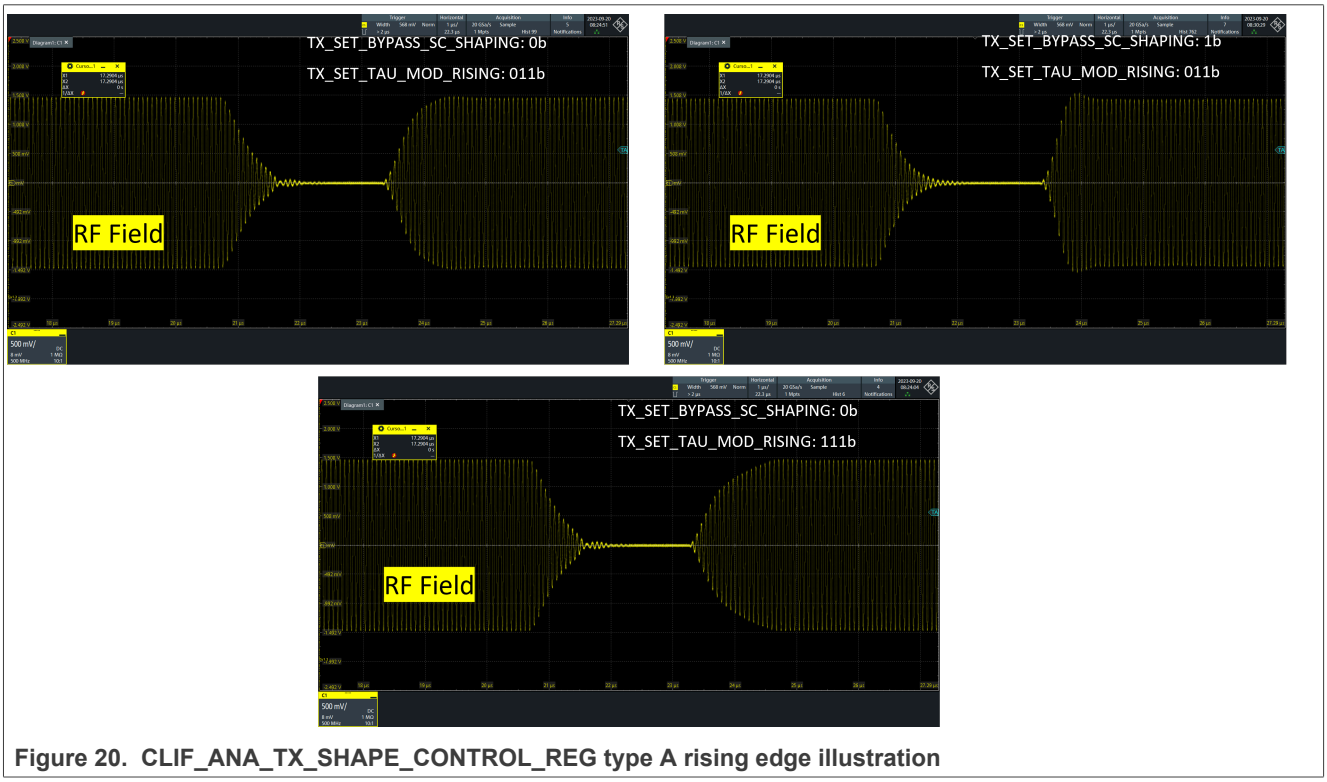

Figure 20. CLIF_ANA_TX_SHAPE_CONTROL_REG type A rising edge illustration

- **Adjusting Residual Carrier**

With the TX shaping, the overshoot at the end of the pulse can be reduced. The TX SC shaping can be enabled with the bit TX_BYPASS_SC_SHAPING, which must be set to 0h (= disable the bypass).

The TX_RESIDUAL_CARRIER defines the carrier level at the end of the pulse, when the risetime of the pulse starts.

Parameter: **TX_RESIDUAL_CARRIER_OV_PREV**

Values: 0h to 1Fh

Measurement process:

1. Use a reference PICC to observe the overshoots.

Target:

1. Increase or decrease the value to meet the standard.

6.4 CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG

6.4.1 Register definition

CLIF_TX_UNDERSHOOT_CONFIG_REG can be used to shape the TX transmission signal, by adjusting the undershoot pattern.

Table 25. CLIF_TX_UNDERSHOOT_CONFIG_REG address

Register name	Register Address
CLIF_TX_UNDERSHOOT_CONFIG_REG	0x16

Table 26. CLIF_TX_UNDERSHOOT_CONFIG_REG register

Bit	Symbol	Description
[4:1]	TX_UNDERSHOOT_PATTERN_LEN	Defines length of the undershoot prevention pattern (value +1). The pattern is applied starting from the MSB of the defined pattern, all other bits are ignored.
[0]	**TX_UNDERSHOOT_PROT_ENABLE**	If set to 1, the undershoot protection is enabled

Table 27. CLIF_TX_UNDERSHOOT_CONFIG_REG transitions

Technology	Baud rate	Transition ID
type A	106	0x72
type B	106	0x82
type F	212	0x94
	424	0x96

6.4.2 Register setting procedure

- **Adjusting TX_UNDERSHOOT_CONFIG_REG**

The undershoot protection must be enabled with TX_UNDERSHOOT_PROT_ENABLE (bit 0) in the TX_UNDERSHOOT_CONFIG register.

Parameter: TX_UNDERSHOOT_PATTERN.

Values: 0h to Fh

Measurement process:

1. Use oscilloscope and zoom as depicted in the picture below.

Target:

1. Select settings for which the timing meets the specification.
2. 0h value means small pattern length (potential overshoot, undershoot issue).
3. Fh value means maximum pattern length.
4. Typically a pattern length around 3 to 5 turned out to be useful

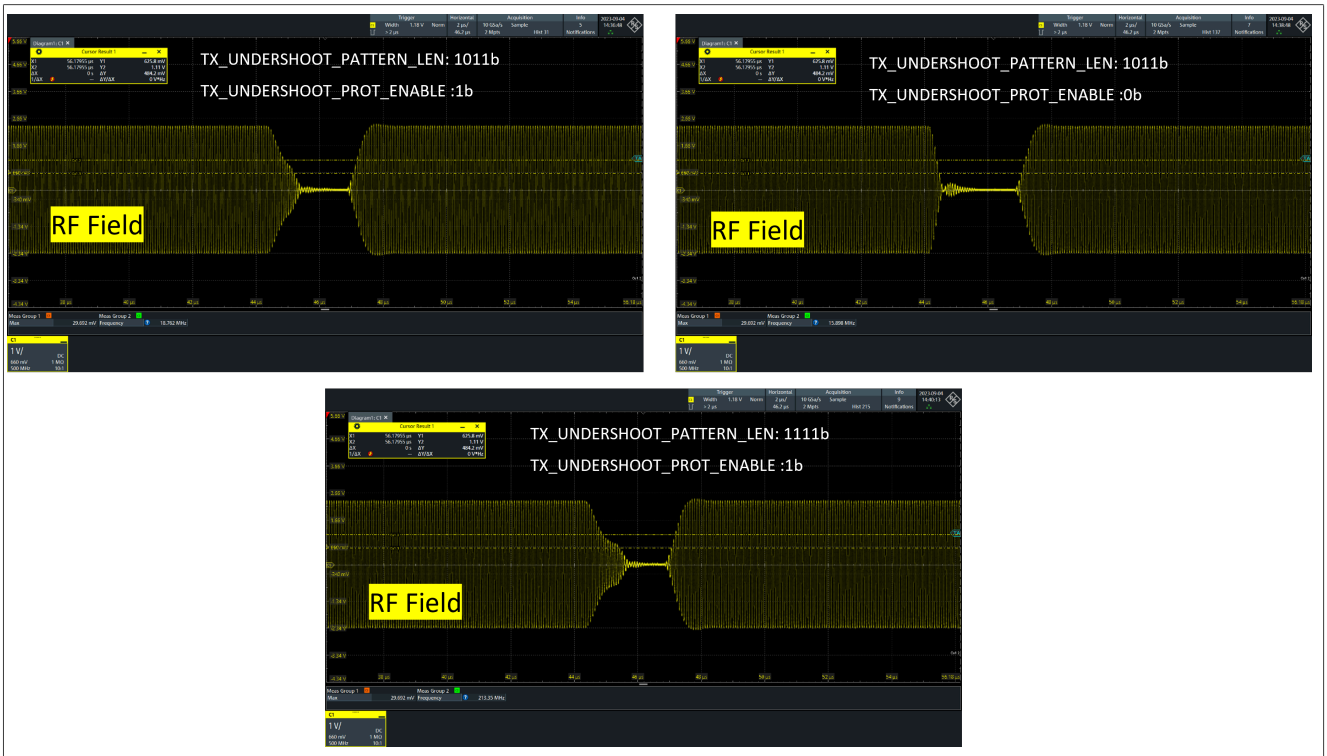

Figure 21. TX_UNDERSHOOT_CONFIG_REG

6.5 CLIF_ANA_RX_REG

6.5.1 Register definition

Refer to Section 5.8.1 for CLIF_ANA_RX_REG register definition.

Table 28. CLIF_ANA_RX_ REG transitions for reader mode

Technology	Baud rate	Transition ID
15693	-	0x20
type A	106	0x3C
	212	0x3E
	424	0x40
	848	0x42
type B	106	0x4C
	212	0x4E
	424	0x50
	848	0x52
type F	212	0x5E
	424	0x60

Remark: For each communication type and baud rate, you must choose the right transition. In the table below, you find the transition, which corresponds to each tag type.

6.5.2 Register setting procedure

Parameter: RX_HPCF

Values: 0h to 3h

Measurement process:

1. Use MIFARE DESFire EV1, MIFARE Ultralight UL, TOPAZ, and measure distance (see Section 8).

Target:

1. Select settings for which distance is improved.

Parameter: RX_GAIN_I and RX_GAIN_Q

Values: 0h to 7h

Measurement process:

1. Use MIFARE DESFire EV1, MIFARE Ultralight UL, TOPAZ, and measure distance (see Section 8).

Target:

1. Select settings for which distance is improved. Check if the logs are OK (The **CORE_GENERIC_ERROR_NTF (60 07 01 a1)** should not be observed).
2. It is strongly recommended to check the performance for different ambient temperatures

When the best parameter of CLIF_ANA_RX_REG is found, the configuration of CLIF_SIGPRO_RM_CONFIG1_REG can start.

⚠ If the RX Gain is set too high, you might get the CORE_GENERIC_ERROR_NTF (60 07 01 a1). For more details, see the AN13892.

6.6 CLIF_SIGPRO_RM_CONFIG1_REG

6.6.1 Register definition

CLIF_SIGPRO_RM_CONFIG1_REG can be used to tune the digital signal processing regarding the bit and subcarrier detection for the down-sampled and amplified card mode response. The configuration of this register must be done when the best configuration of CLIF_ANA_RX_REG has been found.

Table 29. CLIF_SIGPRO_RM_CONFIG1_REG address

Register name	Register Address
CLIF_SIGPRO_RM_CONFIG1_REG	0x2D

[15:12]: Defines the threshold for the bit and subcarrier detection based on the amplitude of the correlated I and Q channel signal. It is used for all card mode response types.

[11:8]: Defines the threshold for the phase shift detection based on the amplitude of the correlated I and Q channel. It is used for Type B (all baud rates) and Type A higher baud rates in addition to the Min_Level.

For Min_Level and Min_Level_P:

- High value: The receiver is less sensitive but more robust against noise
- Low value: The receiver becomes sensitive to small card response but also to noise in the system
- Strong dependency on ANA_RX_REG

Care:

- The direct result of a register change is visible after a functional with target activated
- Since the amplitude of the correlated I&Q channels is evaluated, the whole receiver path configuration has a major impact on the final register value (from the RXN/ RXP-pins to the BBA output)

Value range:

- High performance and sensitivity for max. reading range: 2h … 5h
- Typical: 5h … 9h
- High robustness and stability but low reading range: 9h … Fh

Table 30. CLIF_SIGPRO_RM_CONFIG1_REG register

Bit	Symbol	Description
[31:16]	Internal use	Must not be modified
[15:12]	**MIN_LEVEL**	**Define the min level of the reception**
[11:8]	**MIN_LEVEL_P**	**Define the min level for the phase shift detector unit**
[7:0]	Internal use	Must not be modified

⚠ If the CLIF_SIGPRO_RM_CONFIG1_REG is set too low, you might get the CORE_GENERIC_ERROR_NTF (60 07 01 a1). Especially, bits [15:12] → Define the min level of the reception

Table 31. CLIF_SIGPRO_RM_CONFIG1_ REG transitions

Technology	Baud rate	Transition ID
type A	106	0x3C
type B	106	0x4C
type F	212	0x5E
	424	0x60

6.6.2 Register setting procedure

Parameter: MIN_LEVEL.

Values: 0h to Fh

Measurement process:

1. Use MIFARE DESFire EV1, MIFARE Ultralight, TOPAZ, and measure distance (see annex 1).

Target:

1. Select settings for which distance is improved. Check if the logs are OK (The **CORE_GENERIC_ERROR_NTF (60 07 01 a1)** should not be observed).
2. It is strongly recommended to check the performance for different ambient temperatures

Parameter: MIN_LEVEL_P.

Values: 0h to Fh

Measurement process:

1. Use type B and F cards and measure distance (see annex 1).

Target:

1. Select settings for which distance is improved.

6.7 AGC_INPUT_REG

When a signal is present at the RX level, the AGC regulates the signal at a certain level “Vref”. To improve the convergence of the AGC, a starting point can be defined on the AGC_INPUT_REG.

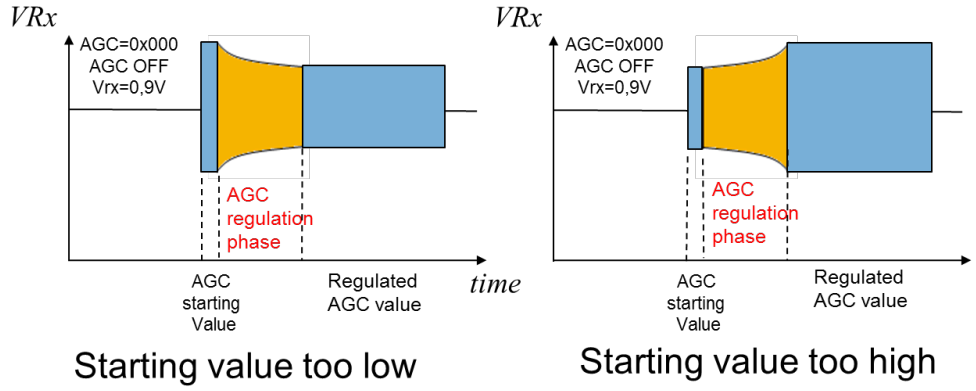

Figure 22. AGC_INPUT_REG

To improve RX on reader mode, the recommendation is to set the AGC value with the same value as the AGC when using LPCD with trace mode enable (set register 0xA0 40 to 0x81, see PN7160 User Manual [2]), without any card on the field.

Example trace: "6F13040080**EE02**"

In this case AGC is **0x2EE**, so use this value as AGC_INPUT_REG for the AGC_RM_VALUE.

Table 32. Fine-tuning of AGC_INPUT register

Register name	Transition ID	Register Address
CLIF_AGC_INPUT_REG	0x06	0x35

Table 33. CLIF_AGC_INPUT_REG register setting

Bit	Symbol	Description
[25 :16]	AGC_RM_VALUE	Static AGC value used for reader mode From 0 (less attenuation) to 0x380 (higher attenuation)

7 Abbreviations

Table 34.

Abbr.	Meaning
AN	Application Note
ALM	Active Load Modulation
CLIF	ContactLess InterfFace
DH	Device Host
FW	Firmware
HW	Hardware
I²C	Inter-Integrated Circuit (serial data bus)
IC	Integrated Circuit
NCI	NFC Controller Interface (NFC Forum Specification)
NFC	Near Field Communication
PCB	Printed Circuit Board
RF	Radio Frequency
RFU	Reserved for Future Use
SLALM	Single Loop ALM
SW	Software

8 Annex 1: Communication distance evaluation and fine-tuning

8.1 Introduction

When the device is in reader mode, the communication with a tag is split in 2 parts:

- Request from reader to tag
- Answer from tag to the reader

When the communication distance is not good enough, the goal is to identify where is the limitation.

- **Phase 1: From reader to tag**

Reason: RF field not sufficient to power up the tag

Symptom: No card answer present

How to solve: Increase the field by adjusting the tuning with lower impedance.

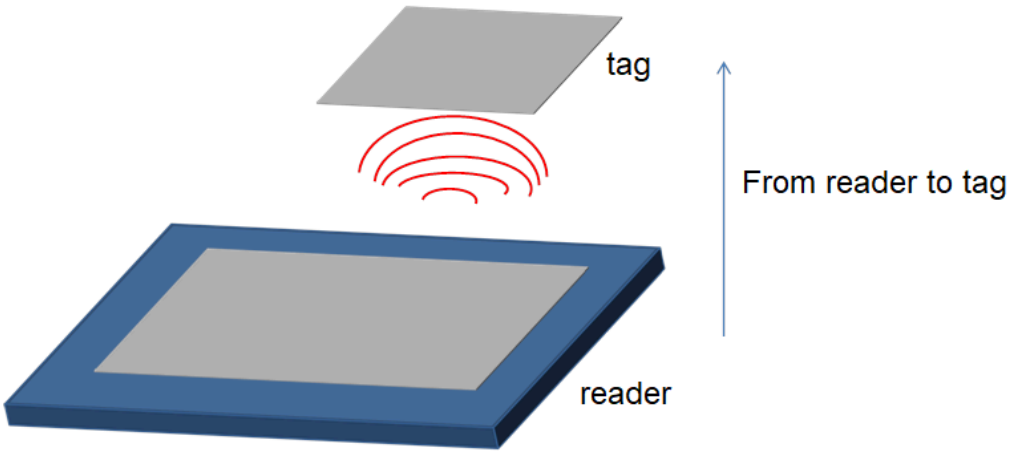

Figure 23. Reader to tag

- **Phase 2: from tag to reader**

Reason: The reader cannot understand the answer from the tag.

Symptom: The card answer is present but not detected by the reader.

How to solve: Adjust the CLIF_ANA_RX_REG and the CLIF_SIGPRO_RM_CONFIG1_REG.

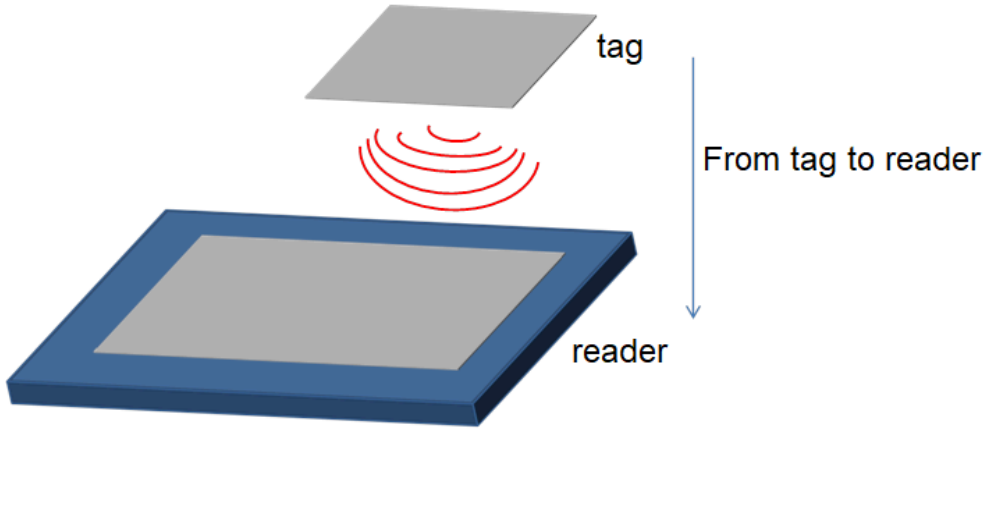

Figure 24. Tag to reader

8.2 Way of working

8.2.1 Step 1

To verify if the tag reacts to the reader, and the answer is received by the device, a spying coil can be put on the tag and connected to an oscilloscope.

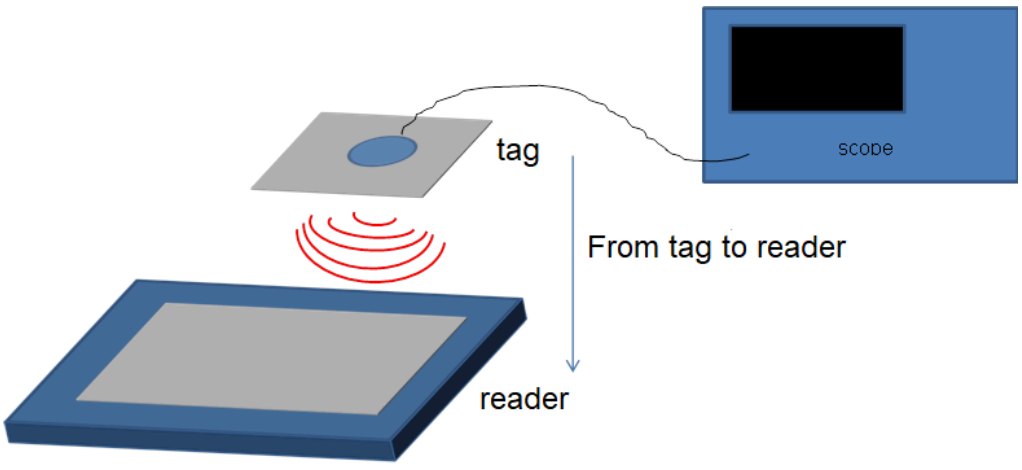

Figure 25. Coil connection

8.2.2 Step 2

Put the tag + spying coil close to the device to set the trigger of the scope (see figure below) to capture the card answer. The tag must be read.

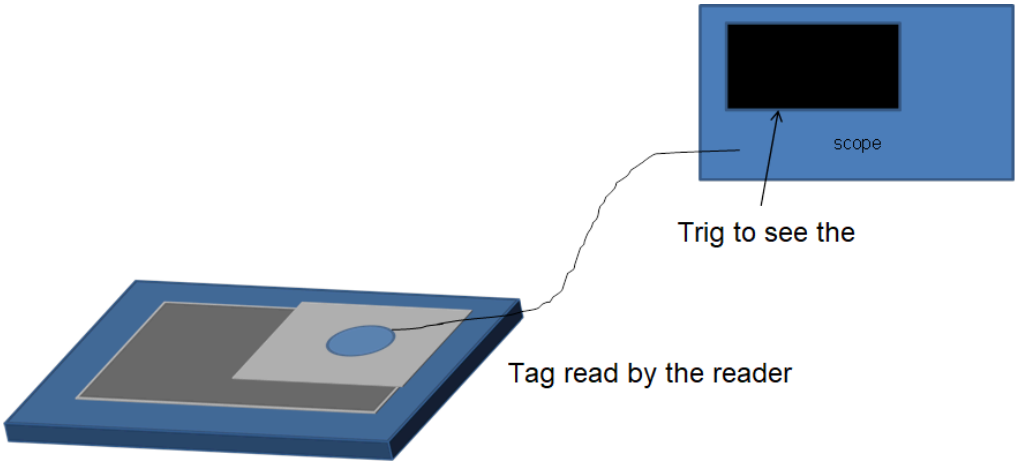

Figure 26. Tag read distance

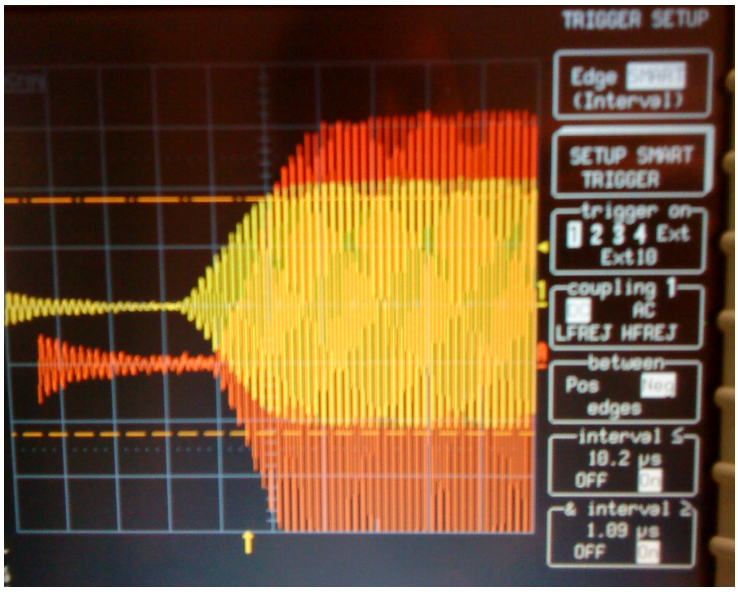

Figure 27. Oscilloscope trigger setup example

8.2.3 Step 3

Put the tag + spying coil far from the device then decrease the distance between the tag and the reader.

When you see the answer from the tag on the scope, you find **the tag answer distance**.

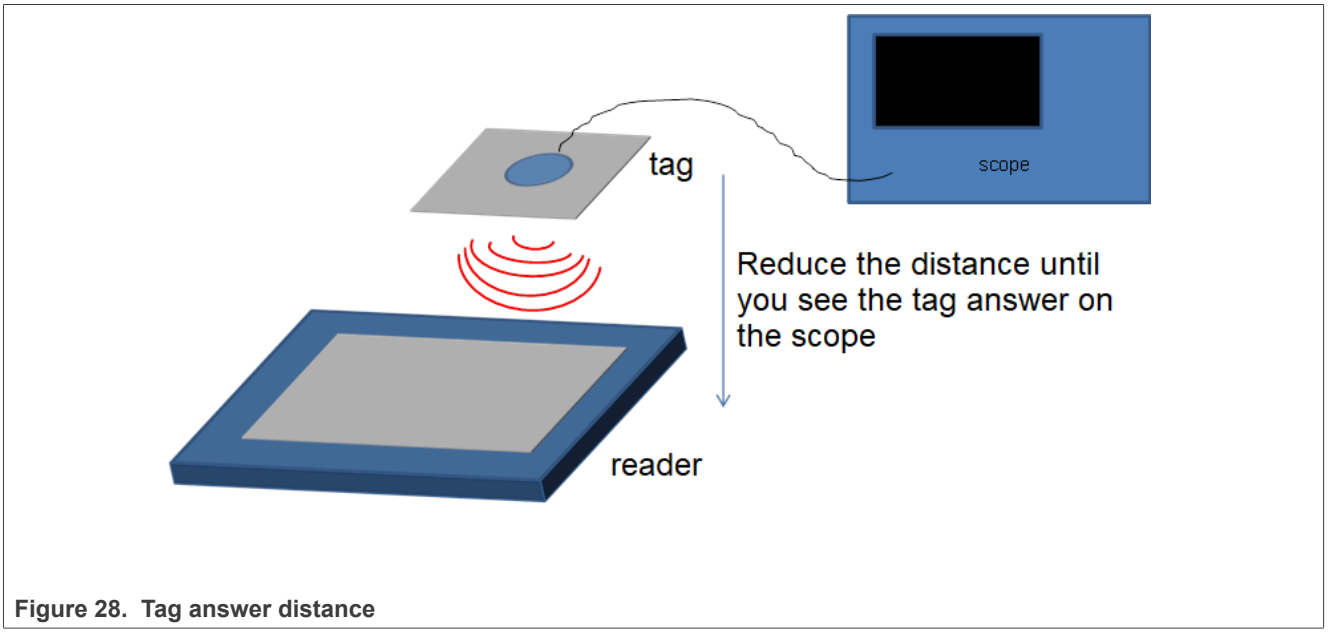

Figure 28. Tag answer distance

8.2.4 Step 4

Continue to decrease the distance between the device and the tag. When the device detects the tag, **the communication distance** has been found.

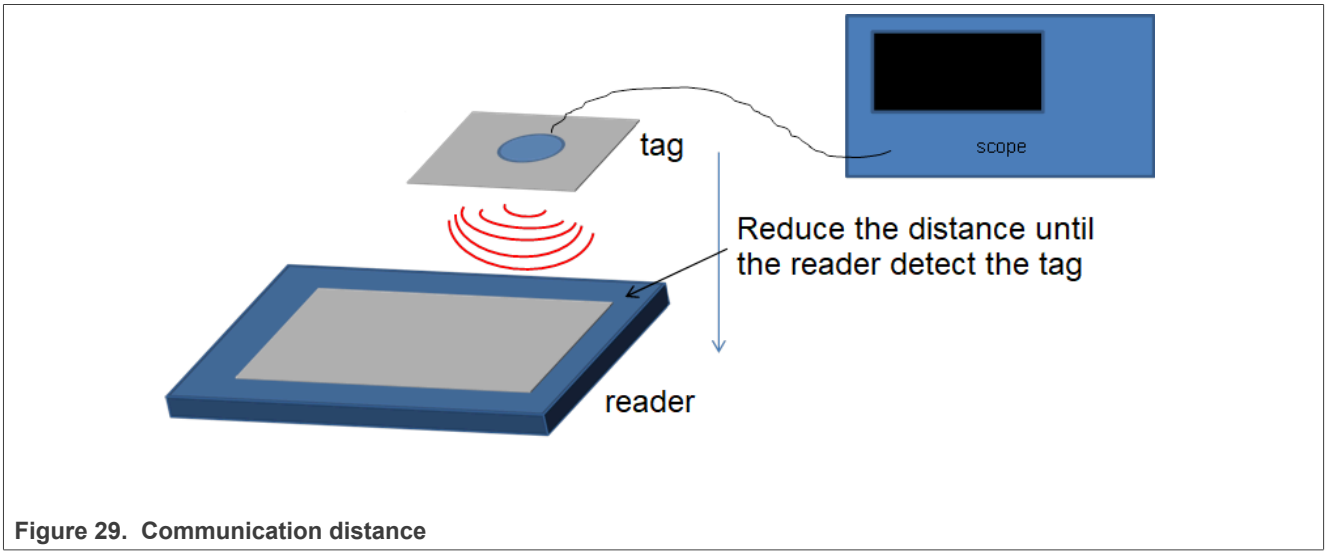

Figure 29. Communication distance

8.2.5 Step 5

Analyze the results:

If **tag answer distance = communication distance**, the performance is limited by the TX part:

To increase the communication distance:

- Increase the RF field power by decreasing the tuning impedance
- Adjust the TX shape to fulfill the communication type specification (ISO14443 for example)

If **tag answer distance > communication distance** the performance is limited by the RX part.

To increase the communication distance:

- Adjust the CLIF_ANA_RX_REG and CLIF_SIGPRO_RM_CONFIG1_REG to improve the communication distance

Remark: The communication distance will generally be lower than the tag answer distance due to the TX performances of the PN7160.

In the table below you find a communication distance example in a device environment with a 40 mm * 25 mm 4 turns antenna.

Table 35. Communication distance examples

Cards	Full Power
ISO15693	62 mm
Topaz	43 mm
FeliCa	35mm
MIFARE Classic 1K	45 mm
MIFARE Classic 4K	32 mm
MIFARE Plus X	26 mm
NTAG 203	42 mm
NTAG 210	58 mm
MIFARE Ultralight	45 mm
MIFARE Ultralight C	25 mm
MIFARE DESFire	23 mm

9 Annex 2: ALM Amplitude and TX shaping evaluation using a standard Scope

In case the EMVCo, ISO, or NFC Forum test setup is not available. A basic measurement using a standard scope can be done. See a few examples below.

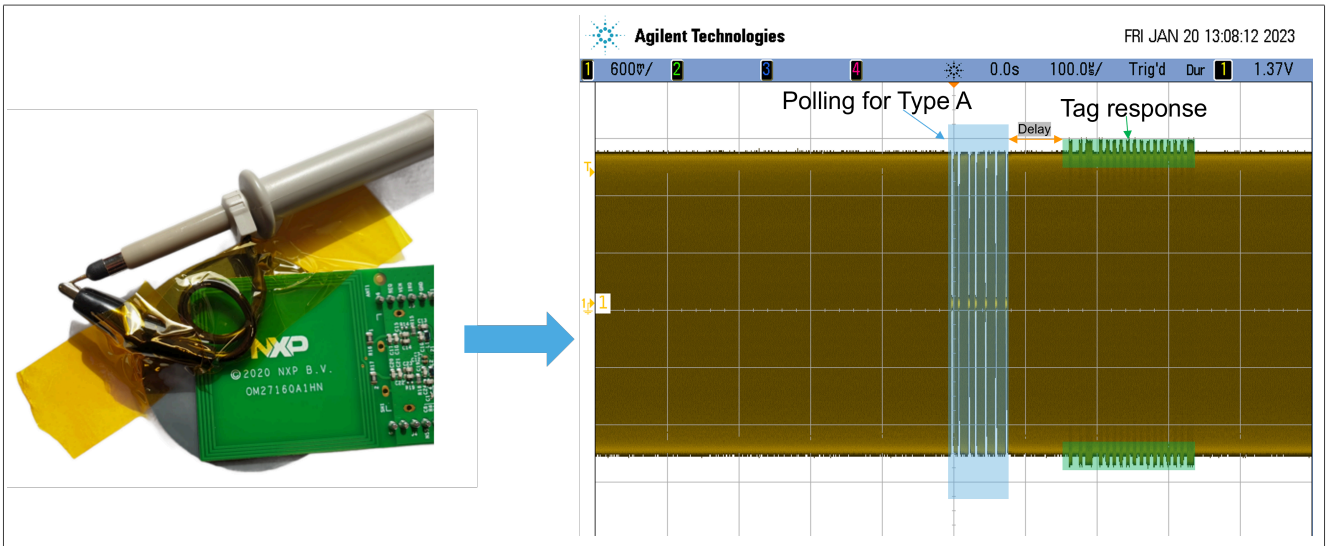

Figure 30. NFC communication captures by the scope

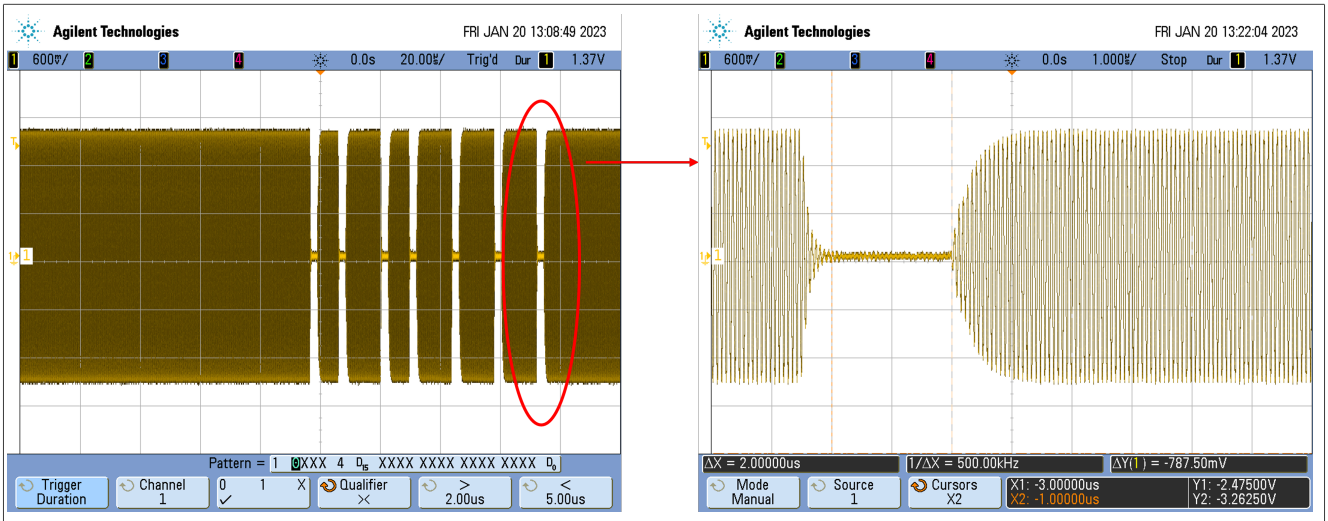

Figure 31. TX Shaping using the scope

To capture the Type A, the following trigger setup (**) can be used:

- Single event
  - Polarity – negative
  - Width
    - Width 2us
    - +- delta 999.9ns

(**) It may be different for different scope types.

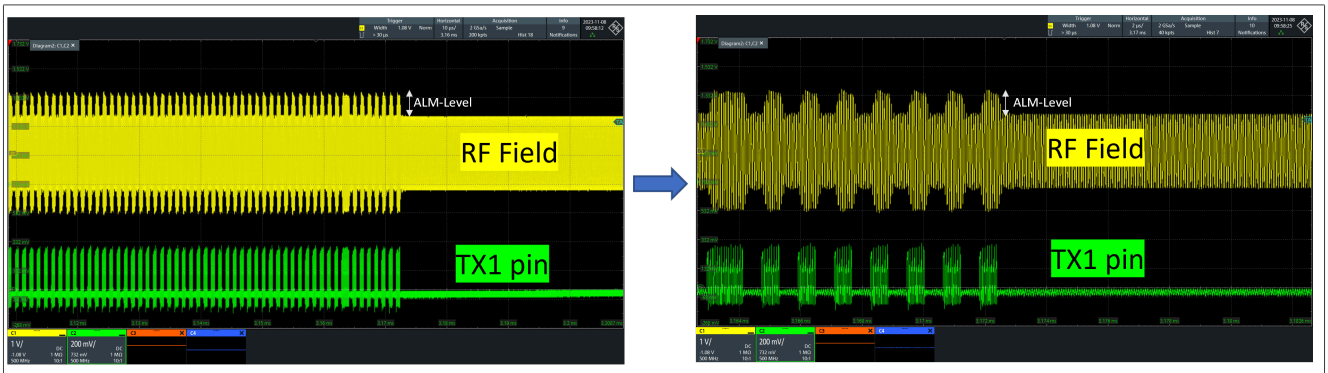

Figure 32. Active Load Modulation Amplitude (Card mode) captured by the scope

10 Annex 3: Default PN7160 RF settings

Table 36 lists the Card/Listener mode registers that can be adjusted.

Table 36. Default PN7160 RF settings: Adjustable Card/Listener mode registers

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name	Description	Comment
0x08	0x44	04 04 04 C4 00	RF_CLIF_CFG_TARGET	(CM) CLIF_ANA_RX_ REG - Global	Receiver settings (RX Gain, HPCF)
0x34	0x44	04 04 04 C4 00	RF_CLIF_CFG_BR_106_ T_RXA	(CM) CLIF_ANA_RX_ REG - Type A/106	Receiver settings (RX Gain, HPCF)
0x38	0x44	04 02 04 C4 00	RF_CLIF_CFG_BR_424_ T_RXA	(CM) CLIF_ANA_RX_ REG - Type A/424	Receiver settings (RX Gain, HPCF)
0x3A	0x44	04 11 00 C4 00	RF_CLIF_CFG_BR_848_ T_RXA	(CM) CLIF_ANA_RX_ REG - Type A/848	Receiver settings (RX Gain, HPCF)
0x44	0x44	04 04 04 C4 00	RF_CLIF_CFG_BR_106_ T_RXB	(CM) CLIF_ANA_RX_ REG - Type B/106	Receiver settings (RX Gain, HPCF)
0x1C	0x44	04 05 04 C4 00	RF_CLIF_CFG_ TECHNO_T_RXF	(CM) CLIF_ANA_RX_ REG - Type F	Receiver settings (RX Gain, HPCF)
0x08	0x42	04 00 02 FF FF	RF_CLIF_CFG_TARGET	(CM) CLIF_ANA_TX_ AMPLITUDE_REG	Transmitter settings (TVDD, GSN, Residual carrier)
0x24	0x03	01 7F	RF_CLIF_CFG_ TECHNO_T_TXA_P	(CM) CLIF_ TRANSCEIVE_ CONTROL_REG	Frame Delay Time (FDT) adjustment
0x08	0x37	04 08 76 00 00	RF_CLIF_CFG_TARGET	(CM) CLIF_TX_ CONTROL_REG	Load Modulation generation modes
0xC2	0x35	04 00 3E 00 03	RF_CLIF_EXT_FIELD_ ON	(CM) CLIF_AGC_INPUT_ REG	Starting AGC point settings

Table 37 lists the Reader/Poller mode registers that can be adjusted.

Table 37. Default PN7160 RF settings: Adjustable Reader/Poller mode registers

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name	Description	Comment
0x06	0x35	04 F4 05 70 02	RF_CLIF_CFG_ INITIATOR	(RM) CLIF_AGC_INPUT_ REG	Starting AGC point settings
0x20	0x44	04 55 0A 00 00	RF_CLIF_CFG_ TECHNO_I_RX15693	(RM) CLIF_ANA_RX_ REG - 15693	Receiver settings (RX Gain, HPCF)
0x3C	0x44	04 66 0A 00 00	RF_CLIF_CFG_BR_106_ I_RXA_P	(RM) CLIF_ANA_RX_ REG - Type A/106	Receiver settings (RX Gain, HPCF)
0x3E	0x44	04 65 09 00 00	RF_CLIF_CFG_BR_212_ I_RXA	(RM) CLIF_ANA_RX_ REG - Type A/212	Receiver settings (RX Gain, HPCF)
0x40	0x44	04 65 09 00 00	RF_CLIF_CFG_BR_424_ I_RXA	(RM) CLIF_ANA_RX_ REG - Type A/424	Receiver settings (RX Gain, HPCF)
0x42	0x44	04 55 0A 00 00	RF_CLIF_CFG_BR_848_ I_RXA	(RM) CLIF_ANA_RX_ REG - Type A/848	Receiver settings (RX Gain, HPCF)
0x4C	0x44	04 65 0A 00 00	RF_CLIF_CFG_BR_106_ I_RXB	(RM) CLIF_ANA_RX_ REG - Type B/106	Receiver settings (RX Gain, HPCF)
0x4E	0x44	04 65 09 00 00	RF_CLIF_CFG_BR_212_ I_RXB	(RM) CLIF_ANA_RX_ REG - Type B/212	Receiver settings (RX Gain, HPCF)
0x50	0x44	04 65 09 00 00	RF_CLIF_CFG_BR_424_ I_RXB	(RM) CLIF_ANA_RX_ REG - Type B/424	Receiver settings (RX Gain, HPCF)

Table 37. Default PN7160 RF settings: Adjustable Reader/Poller mode registers*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name	Description	Comment
0x52	0x44	04 65 0A 00 00	RF_CLIF_CFG_BR_848_I_RXB	(RM) CLIF_ANA_RX_REG - Type B/848	Receiver settings (RX Gain, HPCF)
0x5E	0x44	04 55 08 00 00	RF_CLIF_CFG_BR_212_I_RXF_P	(RM) CLIF_ANA_RX_REG - Type F/212	Receiver settings (RX Gain, HPCF)
0x60	0x44	04 55 08 00 00	RF_CLIF_CFG_BR_424_I_RXF_P	(RM) CLIF_ANA_RX_REG - Type F/424	Receiver settings (RX Gain, HPCF)
0x06	0x42	04 F8 40 FF FF	RF_CLIF_CFG_INITIATOR	(RM) CLIF_ANA_TX_AMPLITUDE_REG - Initiator	Transmitter settings (TVDD, GSN, Residual carrier)
0x72	0x42	02 F8 40	RF_CLIF_CFG_BR_106_I_TXA	(RM) CLIF_ANA_TX_AMPLITUDE_REG - Type A/106	Transmitter settings (TVDD, GSN, Residual carrier)
0x82	0x42	02 68 40	RF_CLIF_CFG_BR_106_I_TXB	(RM) CLIF_ANA_TX_AMPLITUDE_REG - Type B/106	Transmitter settings (TVDD, GSN, Residual carrier)
0x94	0x42	02 78 40	RF_CLIF_CFG_BR_212_I_TXF	(RM) CLIF_ANA_TX_AMPLITUDE_REG - Type F/212	Transmitter settings (TVDD, GSN, Residual carrier)
0x96	0x42	02 80 40	RF_CLIF_CFG_BR_424_I_TXF	(RM) CLIF_ANA_TX_AMPLITUDE_REG - Type F/424	Transmitter settings (TVDD, GSN, Residual carrier)
0x72	0x4A	04 53 07 00 1B	RF_CLIF_CFG_BR_106_I_TXA	(RM) CLIF_ANA_TX_SHAPE_CONTROL_REG - Type A/106	Shaping of the TX transmission signal - rising/falling edge
0x82	0x4A	04 33 07 00 07	RF_CLIF_CFG_BR_106_I_TXB	(RM) CLIF_ANA_TX_SHAPE_CONTROL_REG - Type B/106	Shaping of the TX transmission signal - rising/falling edge
0x94	0x4A	04 43 07 00 07	RF_CLIF_CFG_BR_212_I_TXF	(RM) CLIF_ANA_TX_SHAPE_CONTROL_REG - Type F/212	Shaping of the TX transmission signal - rising/falling edge
0x96	0x4A	04 11 07 01 07	RF_CLIF_CFG_BR_424_I_TXF	(RM) CLIF_ANA_TX_SHAPE_CONTROL_REG - Type F/424	Shaping of the TX transmission signal - rising/falling edge
0x72	0x16	01 01	RF_CLIF_CFG_BR_106_I_TXA	(RM) CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG - Type A/106	Shaping of the TX transmission signal - prevent undershoots
0x82	0x16	01 00	RF_CLIF_CFG_BR_106_I_TXB	(RM) CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG - Type B/106	Shaping of the TX transmission signal - prevent undershoots
0x94	0x16	01 00	RF_CLIF_CFG_BR_212_I_TXF	(RM) CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG - Type F/212	Shaping of the TX transmission signal - prevent undershoots
0x96	0x16	01 00	RF_CLIF_CFG_BR_424_I_TXF	(RM) CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG - Type F/424	Shaping of the TX transmission signal - prevent undershoots
0x3C	0x2D	04 DC 40 04 00	RF_CLIF_CFG_BR_106_I_RXA_P	(RM) CLIF_SIGPRO_RM_CONFIG1_REG - Type A/106	Receiver digital signal processing adjustment
0x4C	0x2D	04 15 34 1F 01	RF_CLIF_CFG_BR_106_I_RXB	(RM) CLIF_SIGPRO_RM_CONFIG1_REG - Type B/106	Receiver digital signal processing adjustment

Table 37. Default PN7160 RF settings: Adjustable Reader/Poller mode registers*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name	Description	Comment
0x5E	0x2D	04 0D 48 0C 01	RF_CLIF_CFG_BR_212_I_RXF_P	(RM) CLIF_SIGPRO_RM_CONFIG1_REG - Type F/212	Receiver digital signal processing adjustment
0x60	0x2D	04 0D 5A 0C 01	RF_CLIF_CFG_BR_424_I_RXF_P	(RM) CLIF_SIGPRO_RM_CONFIG1_REG - Type F/424	Receiver digital signal processing adjustment

Table 38 lists the Card/Listener and Reader/Poller mode registers set by NXP, which must not be changed from the default value to ensure proper functionality.

Table 38. Default PN7160 RF settings: Card/Listener and Reader/Poller mode registers set by NXP

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name
0x00	0x42	02 FF FF	RF_CLIF_CFG_BOOT
0x00	0x43	01 A0	RF_CLIF_CFG_BOOT
0x00	0x7F	04 4B 00 50 09	RF_CLIF_CFG_BOOT
0x02	0x33	04 0F 81 01 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x34	04 07 20 00 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x35	04 F4 01 F4 01	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x41	01 82	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x42	04 00 00 FF FF	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x44	04 00 00 D4 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x45	04 40 80 00 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x47	01 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0x48	01 00	RF_CLIF_CFG_ANTENNA_TEST
0x02	0xFE	04 1F 00 00 00	RF_CLIF_CFG_ANTENNA_TEST
0x04	0x33	04 0F 40 04 00	RF_CLIF_CFG_IDLE
0x04	0x35	04 00 3E 00 00	RF_CLIF_CFG_IDLE
0x04	0x40	01 00	RF_CLIF_CFG_IDLE
0x04	0x44	04 00 08 F6 00	RF_CLIF_CFG_IDLE
0x04	0x45	04 80 40 00 00	RF_CLIF_CFG_IDLE
0x04	0x47	01 00	RF_CLIF_CFG_IDLE
0x04	0x4A	04 00 00 00 00	RF_CLIF_CFG_IDLE
0x08	0x15	01 00	RF_CLIF_CFG_TARGET
0x08	0x16	04 AE 00 1F 00	RF_CLIF_CFG_TARGET
0x08	0x2B	02 88 09	RF_CLIF_CFG_TARGET
0x08	0x2C	04 14 F0 4D B2	RF_CLIF_CFG_TARGET
0x08	0x2D	04 0D 25 2C 01	RF_CLIF_CFG_TARGET
0x08	0x2E	04 20 0F 00 00	RF_CLIF_CFG_TARGET
0x08	0x2F	04 EF AD 80 01	RF_CLIF_CFG_TARGET
0x08	0x30	04 70 00 18 00	RF_CLIF_CFG_TARGET
0x08	0x3F	04 00 00 00 00	RF_CLIF_CFG_TARGET
0x08	0x41	01 40	RF_CLIF_CFG_TARGET
0x08	0x45	04 83 60 40 05	RF_CLIF_CFG_TARGET
0x08	0x85	04 25 13 00 00	RF_CLIF_CFG_TARGET

Table 38. Default PN7160 RF settings: Card/Listener and Reader/Poller mode registers set by NXP*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name
0x09	0x2F	04 00 00 00 01	Internal use
0x09	0x30	04 00 00 00 00	Internal use
0x09	0x37	04 00 00 00 00	Internal use
0x09	0x3F	01 08	Internal use
0x09	0x41	01 03	Internal use
0x09	0x42	04 01 10 FF FF	Internal use
0x09	0x85	04 00 00 00 00	Internal use
0x0C	0x40	01 01	RF_CLIF_CFG_I_PASSIVE
0x0C	0x45	04 C3 82 71 05	RF_CLIF_CFG_I_PASSIVE
0x0C	0x47	01 02	RF_CLIF_CFG_I_PASSIVE
0x10	0x2D	04 0D 25 2C 01	RF_CLIF_CFG_I_ACTIVE
0x10	0x2E	01 60	RF_CLIF_CFG_I_ACTIVE
0x10	0x2F	04 EF AD 80 01	RF_CLIF_CFG_I_ACTIVE
0x10	0x30	04 70 00 18 00	RF_CLIF_CFG_I_ACTIVE
0x10	0x33	04 03 40 04 80	RF_CLIF_CFG_I_ACTIVE
0x10	0x34	04 F7 7F 10 08	RF_CLIF_CFG_I_ACTIVE
0x10	0x35	01 0C	RF_CLIF_CFG_I_ACTIVE
0x10	0x40	02 00 00	RF_CLIF_CFG_I_ACTIVE
0x10	0x44	01 60	RF_CLIF_CFG_I_ACTIVE
0x10	0x45	04 80 40 00 00	RF_CLIF_CFG_I_ACTIVE
0x10	0x47	01 00	RF_CLIF_CFG_I_ACTIVE
0x10	0x48	01 10	RF_CLIF_CFG_I_ACTIVE
0x11	0x2F	04 00 00 00 01	Internal use
0x11	0x30	04 00 00 00 00	Internal use
0x11	0x48	01 00	Internal use
0x11	0x85	04 00 00 00 00	Internal use
0x12	0x16	01 00	RF_CLIF_CFG_T_ACTIVE
0x12	0x35	01 0C	RF_CLIF_CFG_T_ACTIVE
0x12	0x37	04 00 00 00 00	RF_CLIF_CFG_T_ACTIVE
0x1A	0x33	04 4B 02 01 00	RF_CLIF_CFG_TECHNO_I_RXB
0x1A	0x34	04 D5 92 E1 03	RF_CLIF_CFG_TECHNO_I_RXB
0x1C	0x85	04 25 03 00 00	RF_CLIF_CFG_TECHNO_T_RXF
0x1E	0x33	04 4B 02 01 00	RF_CLIF_CFG_TECHNO_I_RXF_P
0x1E	0x34	04 D5 92 E1 03	RF_CLIF_CFG_TECHNO_I_RXF_P
0x20	0x17	04 00 00 80 00	RF_CLIF_CFG_TECHNO_I_RX15693
0x20	0x2D	04 50 44 0C 00	RF_CLIF_CFG_TECHNO_I_RX15693
0x20	0x33	04 03 01 00 50	RF_CLIF_CFG_TECHNO_I_RX15693
0x20	0x34	04 00 00 EC 03	RF_CLIF_CFG_TECHNO_I_RX15693
0x22	0x2E	02 02 60	RF_CLIF_CFG_TECHNO_I_RXF_A
0x22	0x44	04 05 04 C4 00	RF_CLIF_CFG_TECHNO_I_RXF_A
0x22	0x85	04 25 03 00 00	RF_CLIF_CFG_TECHNO_I_RXF_A
0x28	0x16	01 00	RF_CLIF_CFG_TECHNO_T_TXB
0x2A	0x41	01 8E	RF_CLIF_CFG_TECHNO_I_TXB
0x2C	0x16	01 00	RF_CLIF_CFG_TECHNO_T_TXF_P

Table 38. Default PN7160 RF settings: Card/Listener and Reader/Poller mode registers set by NXP*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name
0x2E	0x41	01 8E	RF_CLIF_CFG_TECHNO_I_TXF
0x30	0x15	01 00	RF_CLIF_CFG_TECHNO_I_TX15693
0x30	0x16	04 1F 00 FF FF	RF_CLIF_CFG_TECHNO_I_TX15693
0x30	0x41	01 82	RF_CLIF_CFG_TECHNO_I_TX15693
0x30	0x42	02 88 40	RF_CLIF_CFG_TECHNO_I_TX15693
0x30	0x4A	04 00 00 00 00	RF_CLIF_CFG_TECHNO_I_TX15693
0x31	0x16	04 00 00 00 00	Internal use
0x34	0x2B	02 0C 00	RF_CLIF_CFG_BR_106_T_RXA
0x34	0x2E	02 20 69	RF_CLIF_CFG_BR_106_T_RXA
0x34	0x85	04 25 13 00 00	RF_CLIF_CFG_BR_106_T_RXA
0x36	0x2E	02 40 69	RF_CLIF_CFG_BR_212_T_RXA
0x36	0x2F	04 EF F9 80 08	RF_CLIF_CFG_BR_212_T_RXA
0x36	0x30	04 E0 00 30 00	RF_CLIF_CFG_BR_212_T_RXA
0x36	0x45	01 70	RF_CLIF_CFG_BR_212_T_RXA
0x37	0x45	01 60	Internal use
0x38	0x2E	02 60 69	RF_CLIF_CFG_BR_424_T_RXA
0x38	0x2F	04 AF 5C 80 08	RF_CLIF_CFG_BR_424_T_RXA
0x38	0x30	04 40 00 20 00	RF_CLIF_CFG_BR_424_T_RXA
0x38	0x85	04 25 03 00 00	RF_CLIF_CFG_BR_424_T_RXA
0x3A	0x2E	02 60 79	RF_CLIF_CFG_BR_848_T_RXA
0x3A	0x2F	04 51 0E 10 C1	RF_CLIF_CFG_BR_848_T_RXA
0x3A	0x30	04 26 00 08 00	RF_CLIF_CFG_BR_848_T_RXA
0x3A	0x85	04 0B 03 00 00	RF_CLIF_CFG_BR_848_T_RXA
0x3C	0x33	04 4B 02 01 70	RF_CLIF_CFG_BR_106_I_RXA_P
0x3C	0x34	04 D5 92 E0 03	RF_CLIF_CFG_BR_106_I_RXA_P
0x3E	0x2D	04 05 35 1E 01	RF_CLIF_CFG_BR_212_I_RXA
0x3E	0x33	04 0B 83 00 00	RF_CLIF_CFG_BR_212_I_RXA
0x3E	0x34	04 00 80 E1 03	RF_CLIF_CFG_BR_212_I_RXA
0x40	0x2D	04 05 45 1E 01	RF_CLIF_CFG_BR_424_I_RXA
0x40	0x33	04 0B 83 00 00	RF_CLIF_CFG_BR_424_I_RXA
0x40	0x34	04 00 80 E1 03	RF_CLIF_CFG_BR_424_I_RXA
0x42	0x2D	04 05 25 0F 01	RF_CLIF_CFG_BR_848_I_RXA
0x42	0x33	04 0B 83 00 00	RF_CLIF_CFG_BR_848_I_RXA
0x42	0x34	04 00 80 E1 03	RF_CLIF_CFG_BR_848_I_RXA
0x44	0x2F	04 E3 AD 80 04	RF_CLIF_CFG_BR_106_T_RXB
0x44	0x30	04 70 00 18 00	RF_CLIF_CFG_BR_106_T_RXB
0x44	0x85	04 25 13 00 00	RF_CLIF_CFG_BR_106_T_RXB
0x46	0x2F	04 E7 5D 80 08	RF_CLIF_CFG_BR_212_T_RXB
0x46	0x30	04 B0 00 45 00	RF_CLIF_CFG_BR_212_T_RXB
0x48	0x2F	04 EF 5D 80 08	RF_CLIF_CFG_BR_424_T_RXB
0x48	0x30	04 B0 00 45 00	RF_CLIF_CFG_BR_424_T_RXB
0x4A	0x2F	04 6F 5C 80 04	RF_CLIF_CFG_BR_848_T_RXB
0x4A	0x30	04 70 00 18 00	RF_CLIF_CFG_BR_848_T_RXB
0x4E	0x2D	04 05 35 1E 01	RF_CLIF_CFG_BR_212_I_RXB

Table 38. Default PN7160 RF settings: Card/Listener and Reader/Poller mode registers set by NXP*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name
0x50	0x2D	04 05 35 1E 01	RF_CLIF_CFG_BR_424_I_RXB
0x52	0x2D	04 05 25 0F 01	RF_CLIF_CFG_BR_848_I_RXB
0x56	0x2B	02 80 00	RF_CLIF_CFG_BR_212_T_RXF
0x56	0x2F	04 EF A9 80 01	RF_CLIF_CFG_BR_212_T_RXF
0x56	0x30	01 00	RF_CLIF_CFG_BR_212_T_RXF
0x57	0x30	01 00	Internal use
0x58	0x2B	02 80 08	RF_CLIF_CFG_BR_424_T_RXF
0x58	0x2F	04 0F 5D 20 08	RF_CLIF_CFG_BR_424_T_RXF
0x62	0x2B	02 0C 00	RF_CLIF_CFG_BR_106_I_RXA_A
0x62	0x2F	04 EF AD 80 01	RF_CLIF_CFG_BR_106_I_RXA_A
0x62	0x44	04 04 04 C4 00	RF_CLIF_CFG_BR_106_I_RXA_A
0x62	0x85	04 25 13 00 00	RF_CLIF_CFG_BR_106_I_RXA_A
0x64	0x2B	02 8D 00	RF_CLIF_CFG_BR_212_I_RXF_A
0x64	0x2F	04 EF A9 80 01	RF_CLIF_CFG_BR_212_I_RXF_A
0x66	0x2B	02 8E 08	RF_CLIF_CFG_BR_424_I_RXF_A
0x66	0x2F	04 0F 5D 20 08	RF_CLIF_CFG_BR_424_I_RXF_A
0x70	0x16	04 8E 00 1F 00	RF_CLIF_CFG_BR_848_T_TXA
0x72	0x03	01 3D	RF_CLIF_CFG_BR_106_I_TXA
0x72	0x0D	01 24	RF_CLIF_CFG_BR_106_I_TXA
0x72	0x14	01 24	RF_CLIF_CFG_BR_106_I_TXA
0x72	0x15	01 01	RF_CLIF_CFG_BR_106_I_TXA
0x72	0x41	04 82 07 00 00	RF_CLIF_CFG_BR_106_I_TXA
0x73	0x41	01 00	Internal use
0x74	0x0D	01 11	RF_CLIF_CFG_BR_212_I_TXA
0x74	0x14	01 11	RF_CLIF_CFG_BR_212_I_TXA
0x74	0x15	01 00	RF_CLIF_CFG_BR_212_I_TXA
0x74	0x16	01 00	RF_CLIF_CFG_BR_212_I_TXA
0x74	0x42	02 68 40	RF_CLIF_CFG_BR_212_I_TXA
0x74	0x4A	04 56 07 01 1B	RF_CLIF_CFG_BR_212_I_TXA
0x76	0x0D	01 08	RF_CLIF_CFG_BR_424_I_TXA
0x76	0x14	01 08	RF_CLIF_CFG_BR_424_I_TXA
0x76	0x15	01 00	RF_CLIF_CFG_BR_424_I_TXA
0x76	0x16	01 00	RF_CLIF_CFG_BR_424_I_TXA
0x76	0x42	02 68 40	RF_CLIF_CFG_BR_424_I_TXA
0x76	0x4A	04 56 07 01 1B	RF_CLIF_CFG_BR_424_I_TXA
0x78	0x0D	01 04	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x14	01 04	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x15	01 00	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x16	01 00	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x41	01 8E	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x42	02 F0 40	RF_CLIF_CFG_BR_848_I_TXA
0x78	0x4A	04 11 07 01 1B	RF_CLIF_CFG_BR_848_I_TXA
0x82	0x0F	04 6C 01 04 00	RF_CLIF_CFG_BR_106_I_TXB
0x82	0x15	01 00	RF_CLIF_CFG_BR_106_I_TXB

Table 38. Default PN7160 RF settings: Card/Listener and Reader/Poller mode registers set by NXP*...continued*

Transition ID	Register Address	Value Length and Register Value (first octet = value length, following octets = register value)	Transition Name
0x84	0x15	01 00	RF_CLIF_CFG_BR_212_I_TXB
0x84	0x16	01 00	RF_CLIF_CFG_BR_212_I_TXB
0x84	0x42	02 68 40	RF_CLIF_CFG_BR_212_I_TXB
0x84	0x4A	04 13 07 01 07	RF_CLIF_CFG_BR_212_I_TXB
0x86	0x15	01 00	RF_CLIF_CFG_BR_424_I_TXB
0x86	0x16	01 00	RF_CLIF_CFG_BR_424_I_TXB
0x86	0x42	02 68 40	RF_CLIF_CFG_BR_424_I_TXB
0x86	0x4A	04 12 07 01 07	RF_CLIF_CFG_BR_424_I_TXB
0x88	0x15	01 00	RF_CLIF_CFG_BR_848_I_TXB
0x88	0x16	01 00	RF_CLIF_CFG_BR_848_I_TXB
0x88	0x42	02 68 40	RF_CLIF_CFG_BR_848_I_TXB
0x88	0x4A	04 11 07 01 07	RF_CLIF_CFG_BR_848_I_TXB
0x92	0x33	01 04	RF_CLIF_CFG_ANTENNA_AGC
0x94	0x15	01 00	RF_CLIF_CFG_BR_212_I_TXF
0x96	0x15	01 00	RF_CLIF_CFG_BR_424_I_TXF
0x98	0x15	01 01	RF_CLIF_CFG_BR_106_T_TXA_A
0x98	0x16	01 01	RF_CLIF_CFG_BR_106_T_TXA_A
0x9A	0x15	01 00	RF_CLIF_CFG_BR_212_T_TXF_A
0x9A	0x16	01 00	RF_CLIF_CFG_BR_212_T_TXF_A

11 References

[1] NFC Forum – NCI 2.0 NFC Controller Interface specification (link)
[2] User manual - UM11495 - PN7160 NFC controller (link)
[3] Software tool - PN7160 - RF Settings GUI (link)
[4] Application note - AN13892 - PN7160 frequently asked questions (link)
[5] Specification - Book D - EMV Contactless Communication Protocol, Version 2.6, March 2016 (link)

12 Revision history

Table 39. Revision history

Document ID	Release date	Description
AN13218 v.1.4	31 July 2024	• Section 3 "PN7160 RF Settings Command Builder": updated. • Section 4.1 "Registers default values": updated. • Section 11 "References": updated.
AN13218 v.1.3	28 May 2024	• Section 2.3: Table 2 "Transition ID values": – Transition ID correction: RF_CLIF_CFG_BR_212_I_TXA → 0x72 → 0x74 – Added a new Transition ID: RF_CLIF_CFG_BR_106_I_TXA → 0x72 • Section 3 "PN7160 RF Settings Command Builder": added. • Section 5.1 "CLIF_TX_CONTROL_REG": Corrected NCI command. • Section 5.2 "Card mode ALM phase": Default value added. • Section 6.2 "CLIF_ANA_TX_AMPLITUDE_REG": Figure 19 "Modulation index adjustment " added. • Section 6.3 "CLIF_ANA_TX_SHAPE_CONTROL_REG": Figure 20 "CLIF_ANA_TX_SHAPE_CONTROL_REG type A rising edge illustration" updated. • Section 6.4 "CLIF_ANA_TX_UNDERSHOOT_CONFIG_REG": Figure 21 "TX_UNDERSHOOT_CONFIG_REG" updated. • Section 6.5 "CLIF_ANA_RX_REG": Warning added. • Section 9 "Annex 2: ALM Amplitude and TX shaping evaluation using a standard Scope": added. • Section 10 "Annex 3: Default PN7160 RF settings" added. • Section 11 "References": Reference to AN13892 added.
AN13218 v.1.2	13 September 2021	• Security status changed to "Company public", no content changes.
AN13218 v.1.1	20 August 2021	• Security status changed to "Company restricted".
AN13218 v.1.0	19 April 2021	• Initial version.

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