AN11847

BGU8061 700-1500MHz High linear bypass LNA

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Document information

Info	Content
Keywords	BGU8061, Evaluation board
Abstract	This application note provides circuit schematic, Layout, BOM and typical EVB performance of the BGU8061 bypass LNA.
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1. Introduction

NXPs semiconductors BGU8061 is a high performance integrated low noise amplifier with bypass function. The BGU8061 operates from 700 MHz to 1500 MHz .The BGU8061 is ideally as 3rd stage amplifier in the RX chain for wireless infrastructure application. Its bypass function enables higher dynamic range.

Being manufactured in NXPs high performance QUBiC RF Gen 8 SiGe:C technology, the BGU8061 combines high gain, low noise and high linearity with process stability and ruggedness, which are the characteristics of the SiGe:C technology.

The BGU8061 comes in a 3 x 3 x 0.85 mm 10 terminal plastic thermal enhanced thin outline package HVSON10 (SOT650-1). The LNA is ESD protected on all terminals.

This application note demonstrates the BGU8061 applied in the 900 MHz frequency range. In this document, the application circuit, board bill of materials, and typical performance parameters are given. In Fig 1 the evaluation board that is described in this application note is shown.

The BGU8061 performance information is available in the BGU8061 Datasheet.

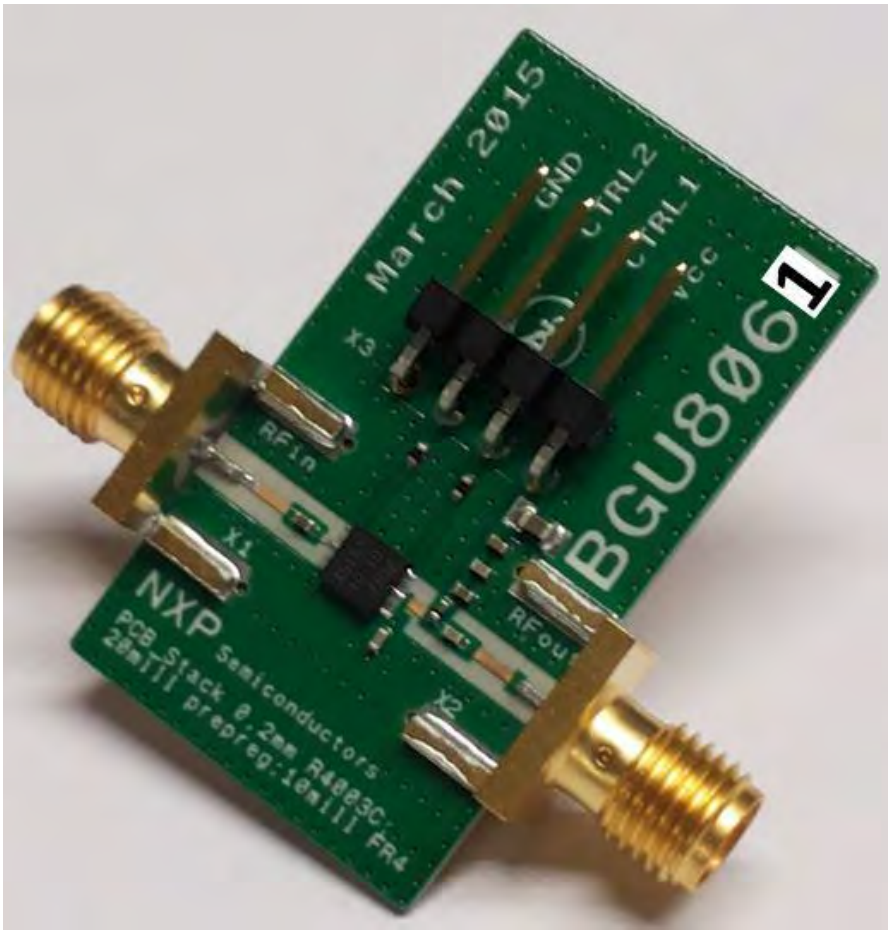


Fig 1. BGU8061 Customer evaluation board

2. Product description

The BGU8061 is a fully integrated high performance low noise amplifier with integrated bias circuit. The MMIC is internally matched to 50 Ω. The BGU8061 also features an integrated bypass circuit for higher dynamic range, as well as an integrated shutdown circuit with fast turn on/off time. This makes it suitable for switched mode applications (time domain duplexing TDD). The BGU8061 can be set in 3 modes: gain mode, bypass mode, and isolation mode (both LNA and bypass are disabled).

The BGU8061 key features and benefits (typical values at 900 MHz)

- Low noise figure of 1.1 dB
- 19.5 dB typical gain
- Frequency range of 700 MHz to 1500 MHz
- High linearity with an $IP3_O$ of 36.5 dBm (gain mode) , 44 dBm (bypass mode)
- Operating at single supply 5 V
- 50 Ω input and output impedance
- Unconditionally stable up to 20 GHz
- Fast turn off and turn on to support TDD systems

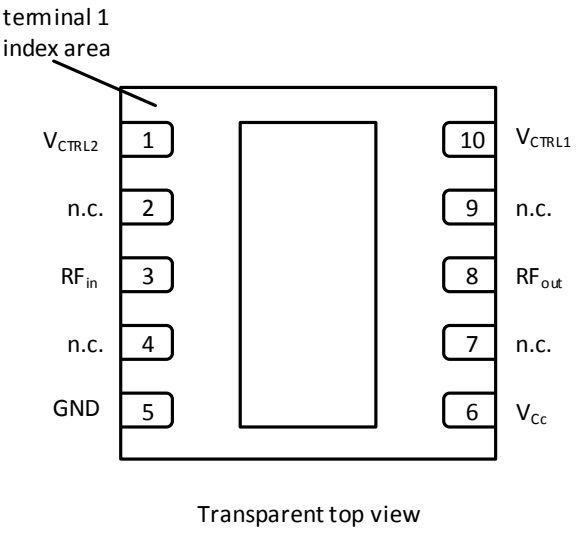


Fig 2. Pin description

3. BGU8061 Bypass LNA evaluation board.

The BGU8061 evaluation boards simplifies the RF evaluation of the BGU8061. The evaluation board enables testing the device RF performance and requires no additional support circuitry. The BGU8061 evaluation board is fabricated on a 35 x 20 mm 1mm thick 4 layer PCB. The 0.2 mm (8 mill) top layer uses ROGERS R4003C for optimal RF performance. The board is fully assembled with the BGU8061, including the external components. The board is supplied with two SMA connectors to connect input and output to the RF test equipment.

3.1 Application circuit.

The application board circuit diagram that is implemented on the EVB is shown in Fig 3

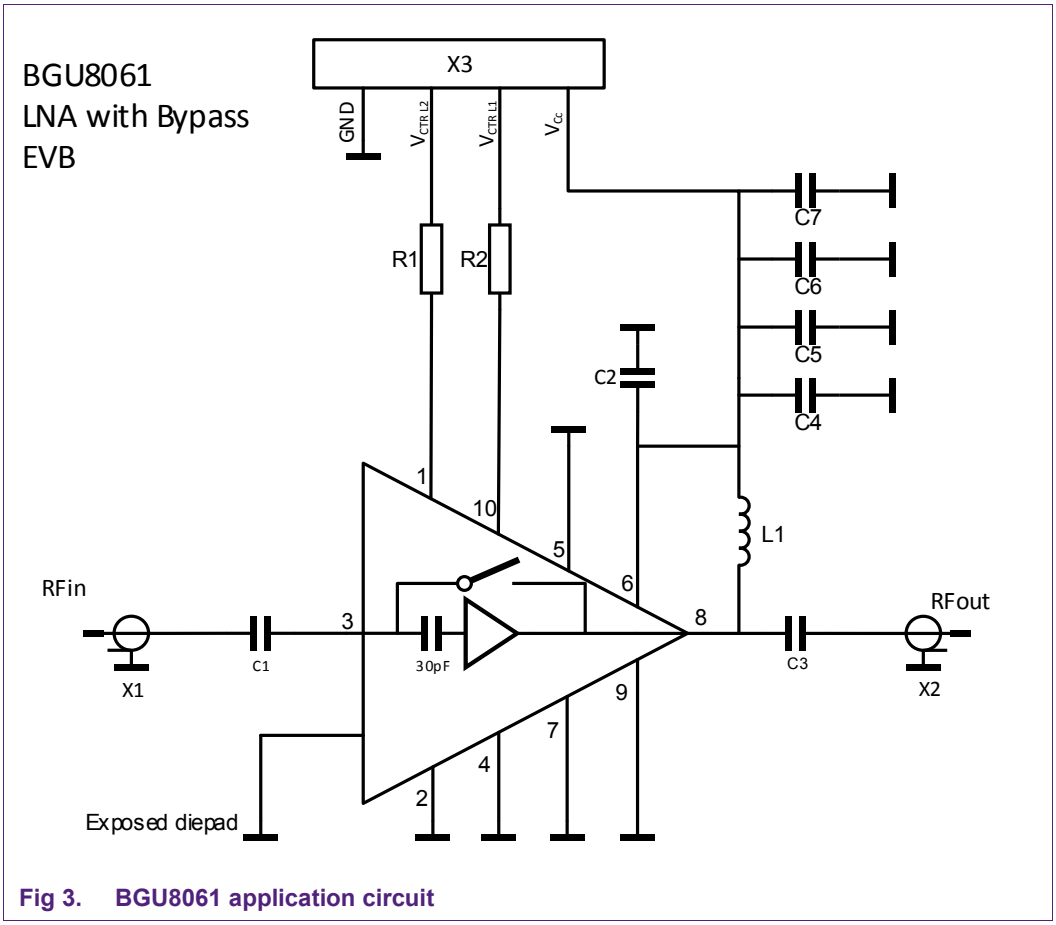


Fig 3. BGU8061 application circuit

When the power supply is connected to the V_{CC} pin of connector X3, the RF out (pin 8) is biased via inductor L1, which provides RF blocking to the supply line. Additionally the internal bias- and control circuitry is bias via pin 6. Capacitors C2, C4, C5, C6 and C7 are supply decoupling capacitors, where R1 and R2 are protection resistors for the digital control lines V_{CTRL1} and V_{CTRL2}. Both V_{CTRL} pins have internal high ohmic pull down resistors.

The RF input and output signals can be applied via SMA connector X1 and X2, where capacitors C1 and C3 are DC-blocking capacitors.

3.2 PCB layout information and component selection

- A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board can serve as a guideline for laying out a board using the BGU8061.
- The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output lines.
- V_{cc} is decoupled by C2 and C4. These capacitances should be located as close as possible to the device, to avoid AC leakage via the bias lines. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device.
- In this report as well as in the datasheet the value of C1 is stated as 100 nF. This values is not critical. Internally there is a DC blocking capacitor of 30 pF. So 30 pF in series with 100nF will result in ~ 30pF with a reactance of -7.5j @ 0.7GHz and -3.5j @ 1.5 GHz. So in a final application the value of C1 might be chosen lower e.g. 1nF with marginal influence on the total reactance. 1nF+30pF results in a complex reactance of -7.8j @ 0.7 GHz and -3.6j @ 2.7 GHz. Choosing C1 1nF is still low ohmic enough!
- The value for C3 is critical for power on/off settling time. This capacitor together with the output stage of the BGU8061 and the bias choke L1 create a time constant. So If the value of C3 is chosen to be too high >1 nF, it will be visible in the switching speed which will become >2us.
- The self-resonance frequency of inductor L1 should be chosen above frequency band of interest for good choking. In this case, the Murata LQG15 series has been used. Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BGU8061 evaluation board is given in Fig 4

3.3 Evaluation board layout

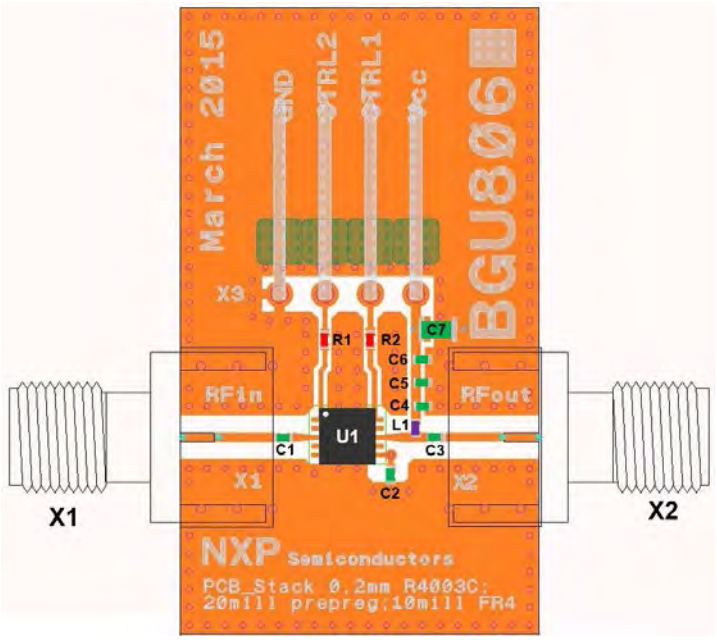
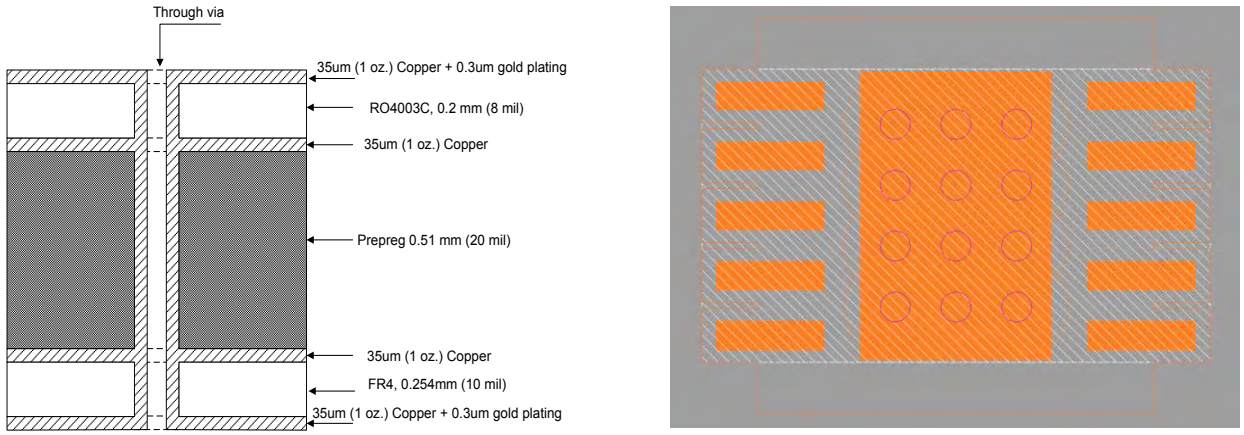


Fig 4. BGU8062 evaluation board layout and component placement

3.3.1 PCB stack and recommended footprint.

The PCB material used to implement the LNA is a 0.2 mm (8 mil) RO4003C low loss printed circuit board which is merged to a 0.51 mm (20 mil) prepreg and a 0.254 mm (10 mil) FR4 layer for mechanical stiffness. See Fig 5a

The official drawing of the recommended footprint can be found via following link. sot650-1.pdf. General reflow solder recommendations can be found via this link. If micro strip coplanar PCB technology is used it is recommended to use at least 12 ground-via holes of 300 um this is also used on the EVBs as shown in Fig 5b. For thermal reasons it is also recommended to resin-filled vias.



a. Cross section of the layer stack

b. Recommended footprint

Fig 5. PCB stack and footprint

3.4 Bill of materials

Table 1 gives the bill of materials as is used on the EVB.

Table 1. BOM

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
U1	BGU8061			NXP BGU8061	
PCB	20x35x1mm			KOVO	RO4003C
C1	Capacitor	0402	100 nF	Murata GRM1555	DC block
C2, C3	Capacitor	0402	100 pF	Murata GRM1555	RF decoupling, DC block
C5	-	0402		Murata GRM1555	Optional
C4	Capacitor	0402	1 nF	Murata GRM1555	Decoupling
C7	Capacitor	0806	1 uF	Murata GRM1555	LF Decoupling
C6	Capacitor	0402	10 nF	Murata GRM1555	Decoupling
L1	Inductor	0402	15 nH	Murata LQG15	Bias choke/Output match
R1, R2	resistor	0402	1 kΩ	Various	
X1,X2	SMA RF connector			Johnson, End launch SMA 142-0701-841	RF connections
X3	DC header			Molex, PCB header, right angle, 1 row 4 way	DC connections

4. Measurement results

Table 2. Mode settings

Mode	S11	S21	S12	S22	Icc
LNA Mode	Matched	Gain	Isolation	Matched	67 mA
Bypass mode	Matched	Low loss	Low loss	Matched	2.4 mA
Isolation mode	Unmatched	isolation	isolation	Unmatched	2.4 mA

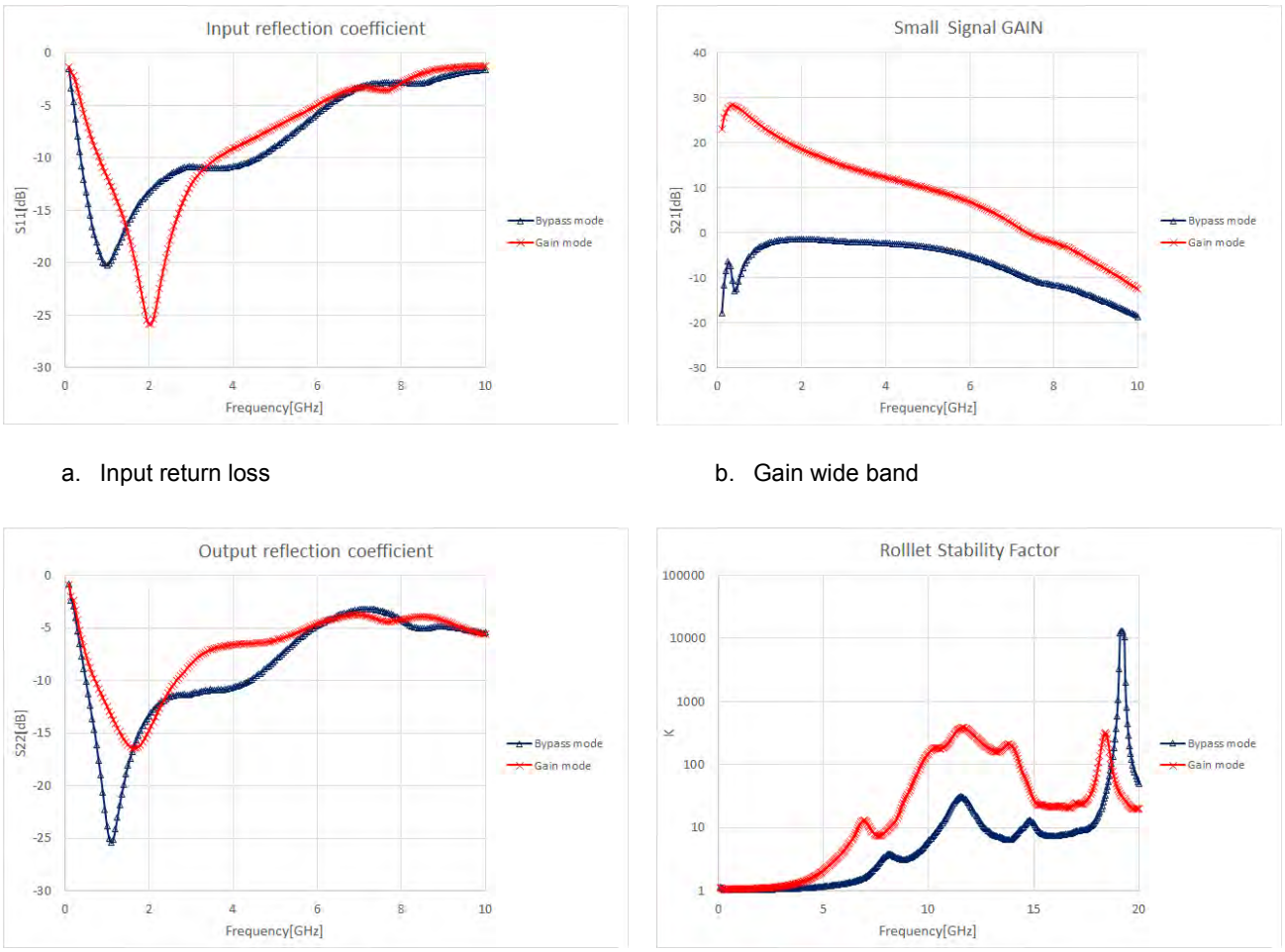
The table below shows the typical performance of the BGU8061 evaluation board, limited number of EVBs was used.

Vcc = 5 V; Tamb = 25°C input and output 50 Ω; unless otherwise specified. All RF parameters are measured in an application board					Evaluation		
					Min.	Avg.	Max.
Symbol	Parameter	Conditions		Unit			
I_{CC}	supply current	LNA ON - BYPASS OFF		mA	65.60	66.66	68.20
		LNA OFF - BYPASS ON		mA	2.40	2.40	2.40
G_{ass}	associated gain	LNA ON - BYPASS OFF	f = 700 MHZ	dB	22.56	22.63	22.71
			f = 900 MHZ	dB	20.81	20.88	20.96
			f = 1200 MHZ	dB	18.70	18.77	18.86
			f = 1500 MHZ	dB	17.05	17.13	17.22
		LNA OFF - BYPASS ON	f = 700 MHZ	dB	-1.20	-1.18	-1.14
			f = 900 MHZ	dB	-1.03	-1.01	-0.98
			f = 1200 MHZ	dB	-1.04	-1.01	-0.99
			f = 1500 MHZ	dB	-1.15	-1.12	-1.09
G_{flat}	gain flatness	LNA ON - BYPASS OFF	f = 700 MHZ	dB	0.88	0.90	0.91
			f = 900 MHZ		0.76	0.77	0.77
			f = 1200 MHZ		0.59	0.59	0.59
			f = 1500 MHZ		0.50	0.51	0.51
ΔG	gain variation	LNA ON - BYPASS OFF	700 MHz ≤ f ≤ 1500 MHz	dB	5.49	5.50	5.52
NF	noise figure	LNA ON - BYPASS OFF	f = 700 MHZ	dB	1.10	1.12	1.14
			f = 900 MHZ	dB	1.07	1.10	1.11
			f = 1200 MHZ	dB	1.12	1.15	1.16
			f = 1500 MHZ	dB	1.09	1.12	1.14
$P_{L(1dB)}$	ouput power at 1dB compression point	LNA ON - BYPASS OFF	f = 700 MHZ	dBm	20.40	20.58	20.81
			f = 900 MHZ	dBm	20.55	20.72	20.94
			f = 1200 MHZ	dBm	20.40	20.62	20.86
			f = 1500 MHZ	dBm	20.15	20.33	20.61
$IP3_O$	output third order intercept point	LNA ON - BYPASS OFF	f = 700 MHZ	dBm	35.99	36.13	36.37
			f = 900 MHZ	dBm	36.48	36.65	36.89
			f = 1200 MHZ	dBm	36.54	36.68	36.96
			f = 1500 MHZ	dBm	36.63	36.88	37.17
		LNA OFF - BYPASS ON	f = 700 MHZ	dBm	45.04	45.86	46.54
			f = 900 MHZ	dBm	44.67	45.33	45.78
			f = 1200 MHZ	dBm	43.62	44.23	44.75
			f = 1500 MHZ	dBm	43.95	44.58	44.97
RL_{in}	input return loss	LNA ON - BYPASS OFF	f = 700 MHZ	dB	-9.21	-8.95	-8.79
			f = 900 MHZ	dB	-11.18	-10.89	-10.66
			f = 1200 MHZ	dB	-14.06	-13.68	-13.31
			f = 1500 MHZ	dB	-17.50	-17.05	-16.53
		LNA OFF - BYPASS ON	f = 700 MHZ	dB	-18.20	-17.41	-16.91
			f = 900 MHZ	dB	-21.20	-19.81	-19.00
			f = 1200 MHZ	dB	-19.69	-18.66	-17.98
			f = 1500 MHZ	dB	-16.56	-16.01	-15.51
RL_{out}	output return loss	LNA ON - BYPASS OFF	f = 700 MHZ	dB	-9.84	-9.53	-9.35
			f = 900 MHZ	dB	-11.61	-11.27	-11.07
			f = 1200 MHZ	dB	-14.07	-13.59	-13.34
			f = 1500 MHZ	dB	-16.10	-15.66	-14.99
		LNA OFF - BYPASS ON	f = 700 MHZ	dB	-14.92	-14.55	-14.12
			f = 900 MHZ	dB	-21.41	-20.38	-19.52
			f = 1200 MHZ	dB	-26.67	-24.57	-23.54
			f = 1500 MHZ	dB	-18.78	-18.33	-18.10
			min	dB	-14.92	-14.55	-14.12
ISL	isolation	LNA OFF - BYPASS OFF	f = 700 MHZ	dB	43.59	43.70	43.91
			f = 900 MHZ	dB	41.33	41.45	41.66
			f = 1200 MHZ	dB	39.07	39.36	39.64
			f = 1500 MHZ	dB	37.81	38.18	38.42
		LNA ON - BYPASS OFF	f = 700 MHZ	dB	27.27	27.42	27.50
			f = 900 MHZ	dB	25.17	25.31	25.39
			f = 1200 MHZ	dB	22.81	22.93	23.02
			f = 1500 MHZ	dB	21.04	21.15	21.24
$t_{s(pon)}$	Power-On Settling Time	From LNA Mode to Bypass mode	Pin = -20 dBm	µS		0.50	
$t_{s(poff)}$	Power-Off Settling Time	From Bypass Mode to LNA mode	Pin = -20 dBm	µS		0.10	

Fig 6. Typical performance of the BGU8061 based on a limited number of evaluation boards

4.1 S-parameters.

The measured S-parameters and rollet stability factor K are given in Fig 7 . For the measurements, a typical BGU8061 EVB is used. All the S-parameter measurements have been carried out using the setup in Fig 14a



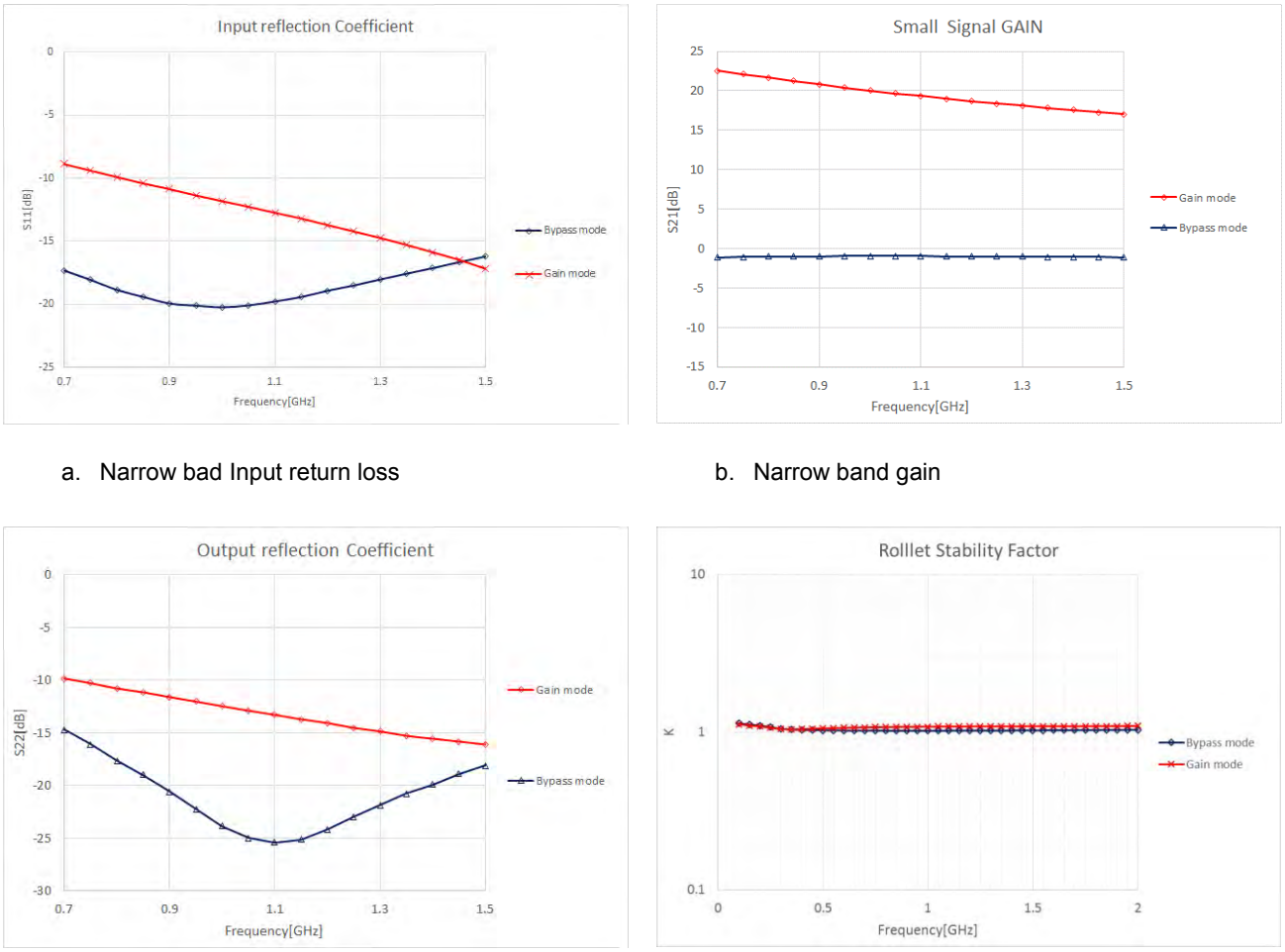
a. Input return loss

b. Gain wide band

c. Output return loss

d. Stability factor

Fig 7. BGU8061 wide band S-Parameters (typical values). V_{CC} = 5 V, Pin=-25 dBm. Gain mode and bypass mode



a. Narrow bad Input return loss

b. Narrow band gain

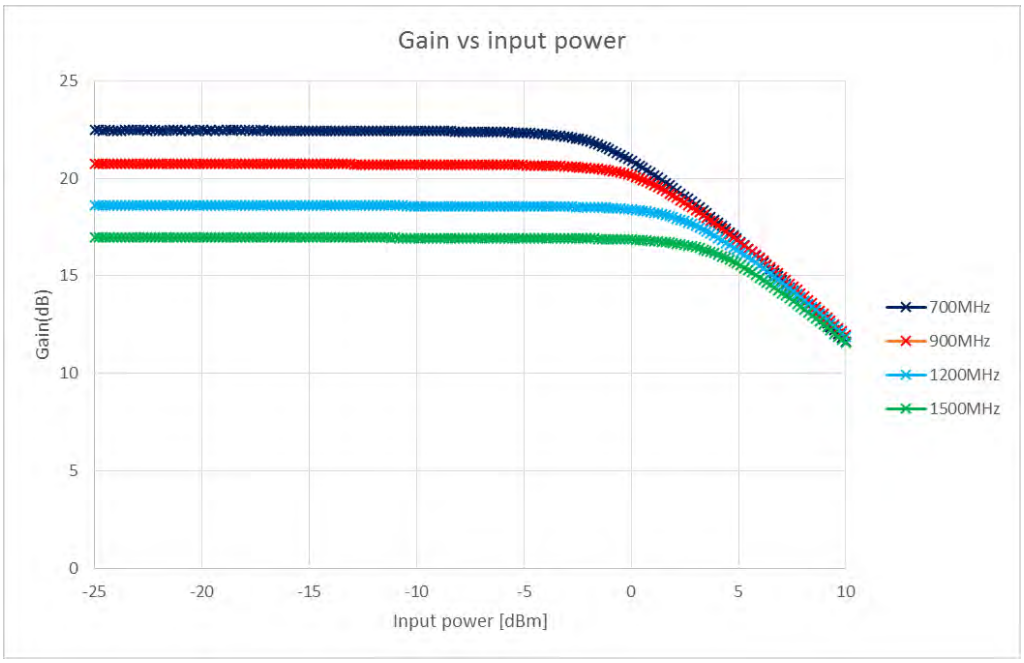
c. Narrow band Output return loss

d. Stability factor

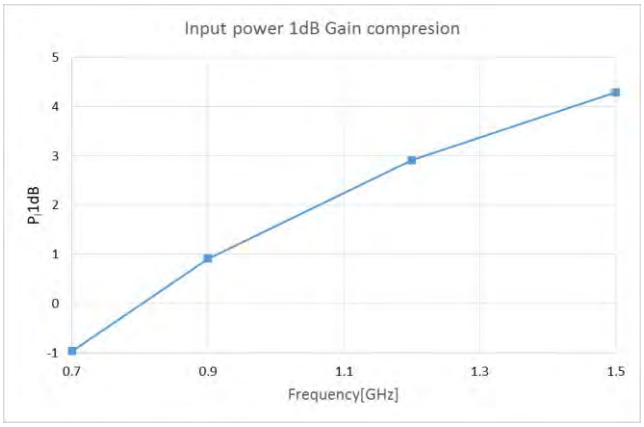
Fig 8. BGU8061 narrow band S-Parameters (typical values). Vcc=5V, Pin=-25dBm. Gain mode and bypass mode

4.2 1dB Gain compression point.

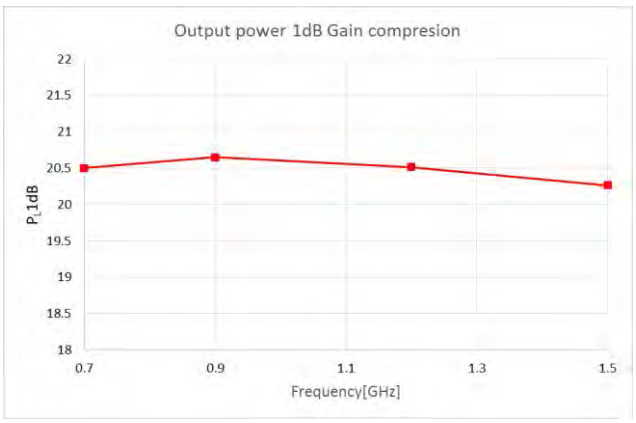
The 1dB gain compression point has been measured using the set up shown in Fig 14a



BGU8061 typical gain vs input power.



a. Input P1dB compression



b. Output P1dB compression

Fig 10. BGU8061 Typical input and output 1dB gain compression performance; gain mode

4.3 Noise figure

Noise figure is being measured using the setup given in Fig 14b

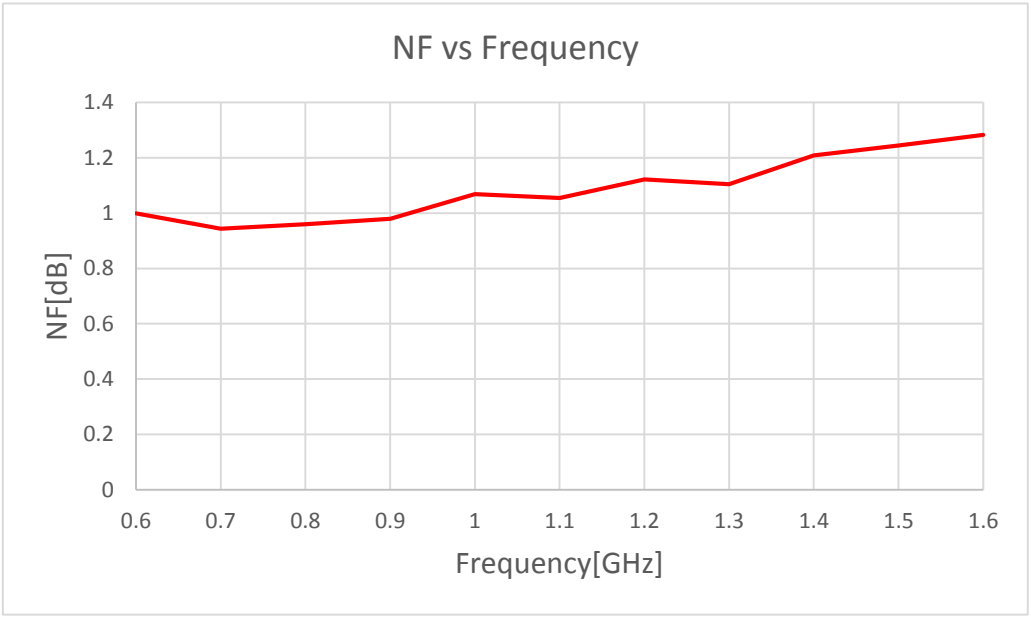
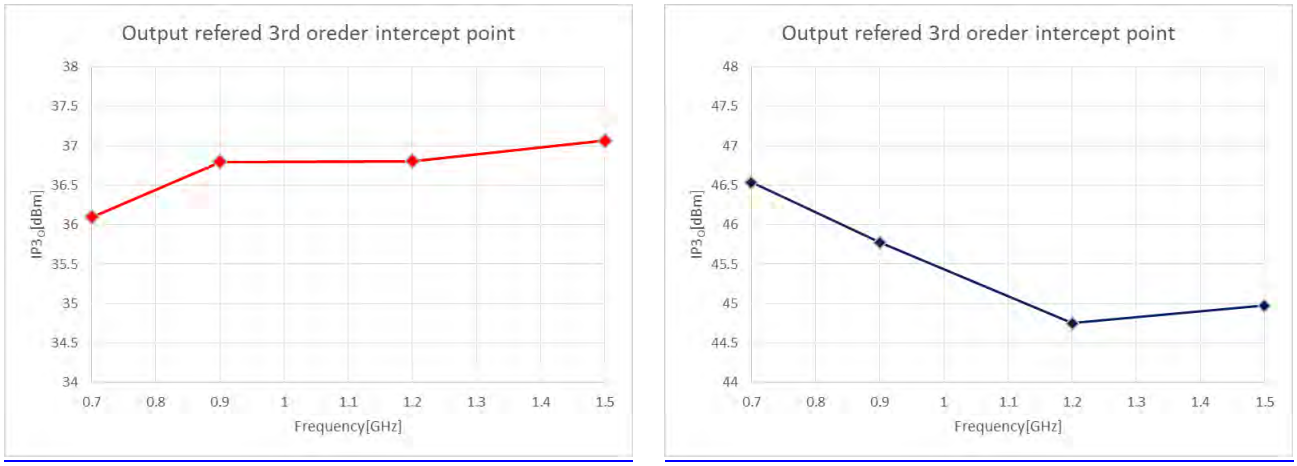


Fig 11. BGU8061 typical noise figure performance in gain mode.

4.4 Third order intercept point.

$IP3_O$ is being measured using the setup given in Fig 14c



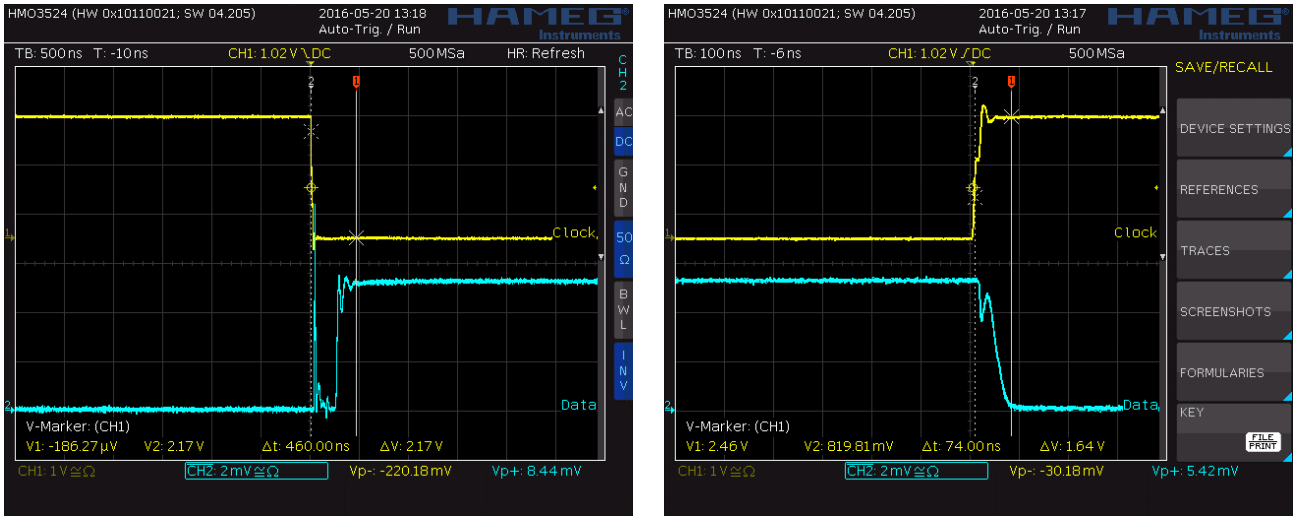
a. Gain mode

b. Bypass mode

Fig 12. BGU8061 $IP3_O$ performance

4.5 Power on/off settling time

The power on/off settling time curves shown in Fig 13 are being measured using the setup that is described in paragraph 5.5 .



a. From bypass to gain mode shows 460ns

b. From gain mode to bypass mode shows 74ns

Fig 13. Power on/off settling time of the BGU8061 evaluation board.

4.6 Typical board performance

Table 3. Typical board performance.

F =900 MHz; T_{AMB}=25 °C

Symbol	Parameter	Conditions		STD	Unit
V_{CC}	Voltage			5	V
I_{CC}	Supply current			68	mA
G_{ASS}	Associated gain	Gain mode		20.8	dB
	Insertion loss	Bypass mode		1.0	dB
NF	Noise figure		[1]	1.1	dB
$P_{L((1dB)}$	Output power at 1 dB gain compression			20.7	dBm
$IP3_O$	Output third-order intercept point	2-tone; tone spacing = 1 MHz; P_O = 5 dBm per tone			
		Gain mode		36.6	dBm
		Bypass mode		45.3	dBm
RL_{IN}	Input return loss	Gain mode		10.9	dB
		Bypass mode		19.8	
RL_{OUT}	Output return loss	Gain mode		11.2	dB
		Bypass mode		20.4	
ISL	Isolation	LNA off-by-pass on		25.3	dB
$T_{s(pon)}$	Power-on settling time	P_i = -20 dBm;		0.46	µs
$T_{s(poff)}$	Power-off settling time	P_i = -20 dBm;		0.07	µs

[1] Board losses of about 0.05 dB have NOT been de-embedded

5. Measurement methods

5.1 Required Measurement Equipment

In order to measure the evaluation board, the following is necessary:

- ✓ 2 or 3 (channel) DC Power Supply up to 100 mA at 5 V, to set V_{CC} and V_{CTRL1} and V_{CTRL2}.
- ✓ Two RF signal generators capable of generating RF signals up to 2 GHz
- ✓ Power combiner for IP3 measurements, for accurate IP3 measurements in the Bypass mode, 2 amplifiers and circulators are needed.
- ✓ An RF spectrum analyzer that covers at least the operating frequencies and a few of the harmonics. Up to 6 GHz should be sufficient.
- ✓ A network analyzer for measuring gain, return loss and reverse isolation
- ✓ Noise figure analyser and noise source
- ✓ Proper RF cables with male connectors.

5.2 Connection and setup

The typical values shown in this paragraph have been measured on the fully automated test setups shown in Fig 14

Please follow the steps below for a step-by-step guide to operate the LNA evaluation board and testing the device functions.

1. Connect the DC power supply to the V_{CC} and GND terminals. Set the power supply to 5 V. Set the V_{CTRL1} and V_{CTRL2} to the values needed for the mode of interest. As indicated in Table 4.

Table 4. Control truth table

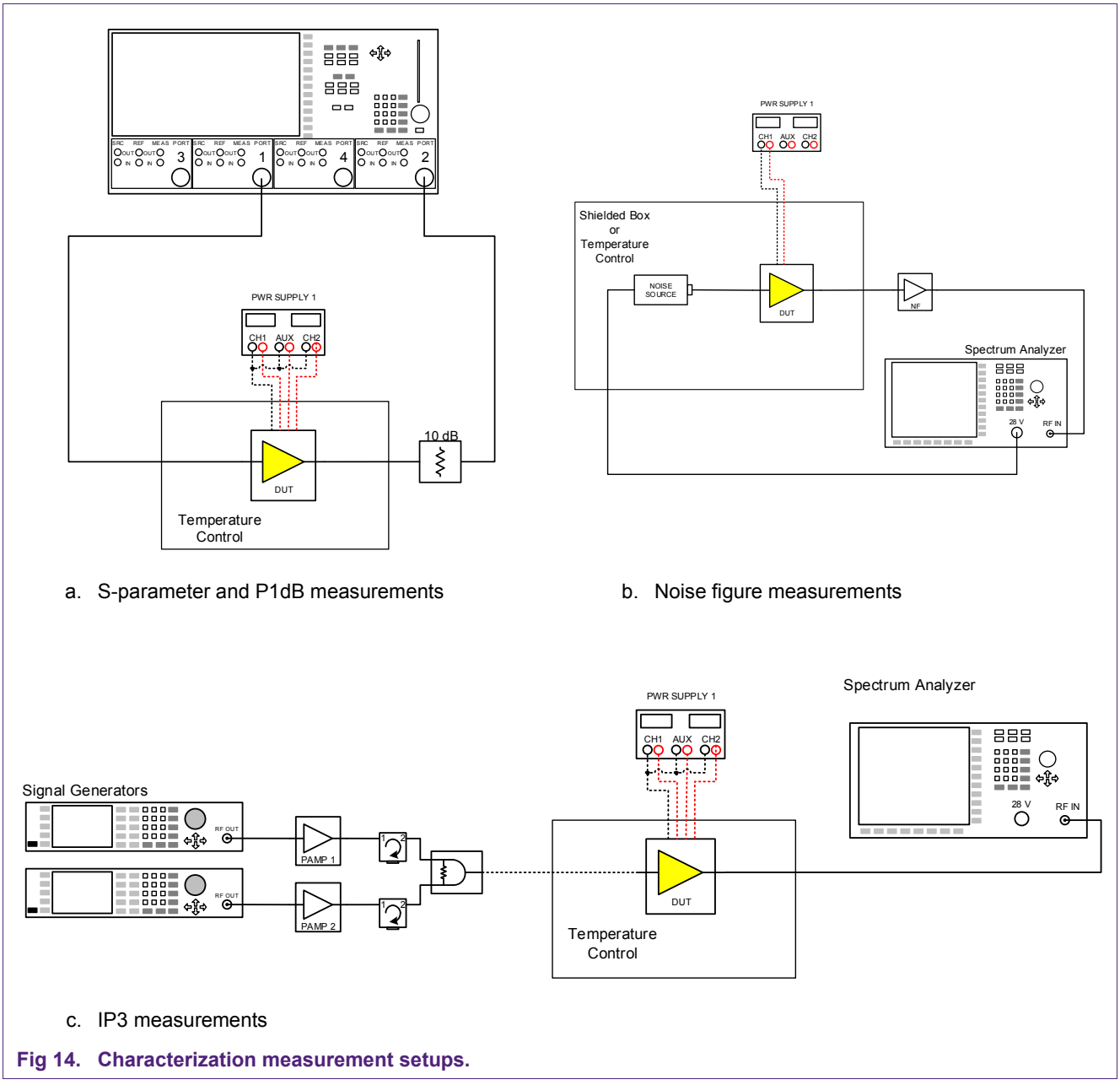
V_{CC} = 5 V; Tamb =25'C

Control signal setting [1]				
CTRL2	CTRL1	LNA	bypass	**Mode**
High	Low	Disable	On	**bypass**
High	High	Disable	On	**bypass**
Low	Low	Enable	Off	**gain**
Low	High	Disable	Off	**isolation**

[1] A logic low is the result of an input voltage specified between - 0.3 V and + 0.7 V
A logic high is the result of an input voltage specified between 1.2 V and 3.6 V

2. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the evaluation board, respectively. Do not turn on the RF output of the signal generator yet, set it to approximately -30 dBm output power at the center frequency of the wanted frequency band and set the spectrum analyzer at the same center frequency and a reference level of 0 dBm.
3. Turn on the DC power supply and it should read approximately 68 mA.
4. Enable the RF output of the generator: The spectrum analyzer displays a tone around –11 dBm.
5. Instead of using a signal generator and spectrum analyzer one can also use a network analyzer in order to measure gain as well as in- and output return loss and P1dB (see Fig 14a)

6. For noise figure evaluation, either a noise figure analyzer or a spectrum analyzer with noise option can be used. The use of a 5 dB ENR noise source, like the Agilent 364B, is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc. between the noise source and the evaluation board should be minimized, since this affects the noise figure (see Fig 14b).



a. S-parameter and P1dB measurements

b. Noise figure measurements

c. IP3 measurements

Fig 14. Characterization measurement setups.

5.3 Third order intercept

The evaluation boards used for this application note are automatically measured on linearity using the set-up shown in Fig 14c

The bias choke L1 on the application board was determined empirically in order to get the best $IP3_O$ as well as keeping good output return loss. $IP3_O$ is determined with 2 tone measurement with 1 MHz tone spacing and the fundamental tone have an output power of 5 dBm. When measuring the high $IP3_O$ values it is essential to check the capabilities of the used measurement equipment. Be aware that the measurement set-up itself is not generating dominating IM3 levels. Advised is to do a THRU measurement without a DUT first. This is very critical when measuring the bypass mode of the BGU8061. For this reason the amplifiers and circulators are implemented in the Set-up.

5.4 Noise figure measurement setup

In Fig 14c the noise figure measurement set-up is shown, this is also intended as a guide only. Substitutions can be made. For noise levels of the BGU8061 it is recommended to perform the noise-measurements in a Faraday's cage or at least put the DUT in a shielded environment. This is recommended to avoid any interference of cellular frequencies that are in the same frequency range.

5.5 Power on/off settling time.

When using the BGU8061 in TDD applications power on/off switching needs to be controlled via the V_{CTRL} pins. Following the truth table in Table 4 to switch from LNA Gain mode to bypass mode and visa versa. V_{CTRL1} and V_{CTRL2} should switch from logic low to logic high simultaneously. Switching between gain mode and isolation mode can be done by only toggling V_{CTRL1} and keeping V_{CTRL2} low.

The setup used to measure the power on/off settling time is shown in Fig 15. This can be used as a guidance to determine the power on/off settling time. The waveform generator is used to provide the control voltage on V_{CTRL1} (pin 10) and V_{CTRL2} (pin 1)

Set the waveform generator Agilent 33250 to square-wave mode and the output amplitude to required voltage for the used control pin, with 50 Ω output impedance. Set the RF signal generator output level to -25 dBm at 1900 GHz and increase its level until the peak detector output level is about 5 mV on 1mV/division, the signal generator RF output level is approximately -20 dBm.

A peak detector is needed to detect the high frequency AC signal at the output of the DUT, representing it as a DC voltage equal to the peak level of the applied AC signal.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized. It is also critical to set the oscilloscope input impedance to 50 Ω on channel 2 so the diode detector can discharge quickly to avoid a false result on the turn off time testing.

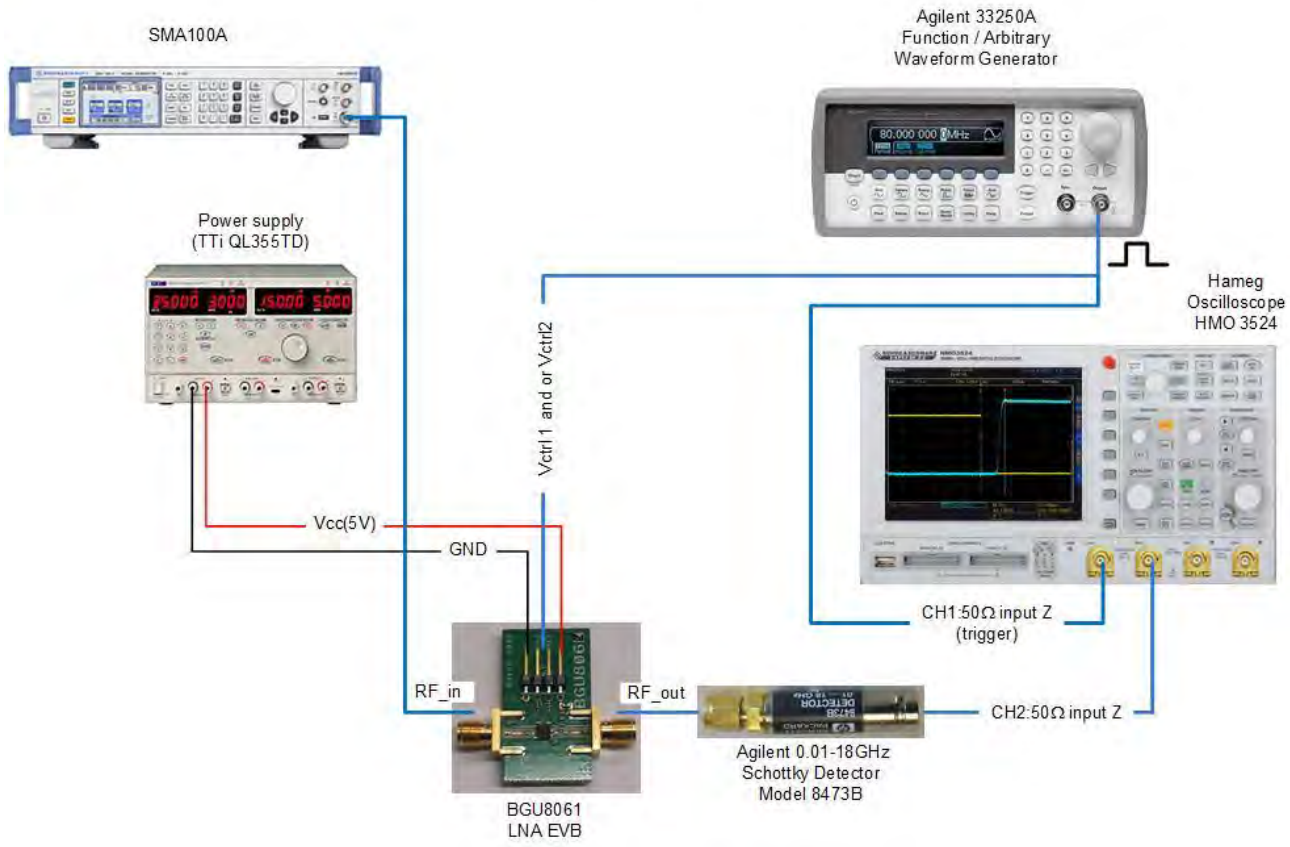


Fig 15. Power on/off settling time measurement setup.

6. Customer Evaluation Kit

In the customer evaluation kit you will find;

- 1 EVB
- 7 loose samples of the BGU8061.

a. b.

Fig 16. Customer evaluation KIT

7. Abbreviations

Table 5. Abbreviations

Acronym	Description
AC	Alternating Current
DC	Direct Current
ESD	Electro Static Discharge
MMIC	Monolithic Microwave Integrated Circuit
PCB	Printed Circuit Board
RF	Radio Frequency
SMD	Surface Mounted Device

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