# AN11559

## LNA for 450 MHz using BGU8051

Rev. 1 — 3 September 2015 Application note

**Document information**

| Info | Content |
|---|---|
| **Keywords** | BGU8051, 450 MHz, LNA, BTS, FDD LTE band 31 |
| **Abstract** | This application note provides circuit schematic, layout, BOM, and typical EVB performance of a 450MHz LNA with the use of the BGU8051. The performance is given at 3.3 and 5 V supply supporting small cell respectively large cell applications. |
| **Ordering info** | Demonstrator board: OM7873,<br>12NC: 9340 690 58598 |
| **Contact information** | For more information, please visit: http://www.nxp.com |

### Revision history

| Rev | Date | Description |
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## 1. Introduction

NXPs semiconductors BGU805X series is a family of integrated low noise amplifiers for the 300 MHz to 6000 MHz range. The series consists of the:

- BGU8051 recommended 300 MHz to 1500 MHz
- BGU8052 recommended 1500 MHz to 2700 MHz
- BGU8053 recommended 2500 MHz to 6000 MHz

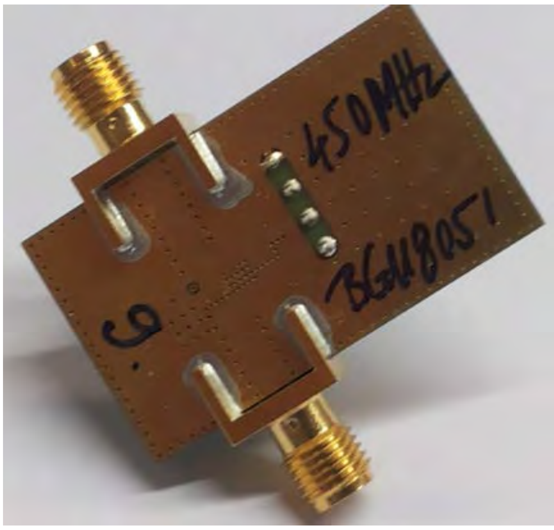
The BGU805X series is a low noise high linearity amplifier family intended for wireless infrastructure applications like BTS, RRH, small cells, but can also be used in other general low noise applications, e.g. active antennas for automotive.

Being manufactured in NXPs high performance QUBiC RF Gen 8 SiGe:C technology, the BGU805X combines high gain, ultra-low noise and high linearity with the process stability and ruggedness which are the characteristics of SiGe:C technology.

BGU805X series comes in the industry standard 2 x 2 x 0.75 mm 8 terminal plastic thin small outline package HVSON8 (SOT1327). The LNA is ESD protected on all terminals.

This application note demonstrates how to optimize the BGU8051 for use in the 450 MHz frequency range. Enabling the 450MHz wireless communication bands. In Fig 1, the evaluation board which is described in this application note, is shown.


a. Front side




b. Back side

**Fig 1. BGU8051 Evaluation board**

## 2. Product description

The BGU8051 is a fully integrated low noise amplifier with integrated bias circuit. The MMIC is internally matched to 50 Ω. The BGU8051 also features an integrated shutdown circuit with fast turn on/off time. This makes it suitable for switched mode applications (time domain duplexing TDD). The device bias current can be set by the value of an external bias resistor $R_{BIAS}$, which connects the supply voltage to the $V_{BIAS}$ pin, or by an external control voltage applied directly to $V_{BIAS}$ pin 1. This adjustable bias current gives flexibility in biasing the device for the optimum performance on NF or linearity. This feature can be useful in case more than one BGU8051 are cascaded. This bias resistor value changes the bias current directly which can be used to trade of linearity for power saving in battery operated applications.

The BGU8051 key features and benefits (typical values at 450 MHz)

- Low noise performance: NF = 0.46 dB
- High linearity performance: $IP3_O$ = 35 dBm
- High output power at 1dB gain compression $P_L$1dB = 19 dBm
- High input return loss $RL_{in}$ 20 dB
- High out return loss $RL_{out}$ 20 dB
- Unconditionally stable up to 20 GHz
- Max RF input power of +20 dBm
- ESD protection on all pins
- Fast turn on and off to support TDD system.

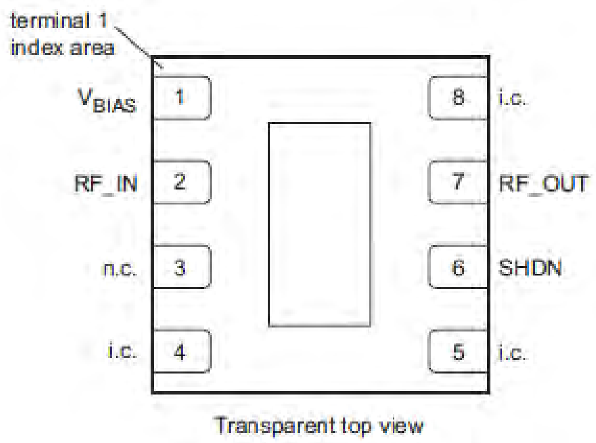



**Fig 2. BGU8051 Pin description**

In Fig 2 the pin out of the BGU8051 is given, the n.c. and i.c pin are recommended to connect to ground, which is the case on the evaluation boards.

## 3. 450MHz LNA Evaluation board

The 450 MHZ evaluation board simplifies the RF evaluation of the BGU8051. The evaluation board enables testing the device RF performance and requires no additional support circuitry. The BGU8051 450 MHz evaluation board is fabricated on a 35 x 20 x 1 mm thick 4 layer PCB. The 0.2 mm (8 mill) top layer uses ROGERS R4003C for optimal

RF performance. The board is fully assembled with the BGU8051, including the external components. The board is supplied with two SMA connectors to connect input and output to the RF test equipment.

## 3.1 Application circuit

The BGU8051 has been characterized for S-parameter and Noise-parameters at different bias settings in a 50 Ω environment. This data can be downloaded from NXPs website as a zip file, BGU8051_S_N_par.zip. The S2P files you can find in this zip file have been used as a small signal model to design this 450 MHz LNA. Although the BGU8051 already has good, gain noise and IRL performance at 450 MHz without any matching, the high-pass matching structure that is created by means of L2 and C8, has the advantage that it cuts of the low frequency gain which increases the stability.

The application board circuit diagram that is implemented on the EVB is shown in Fig 3

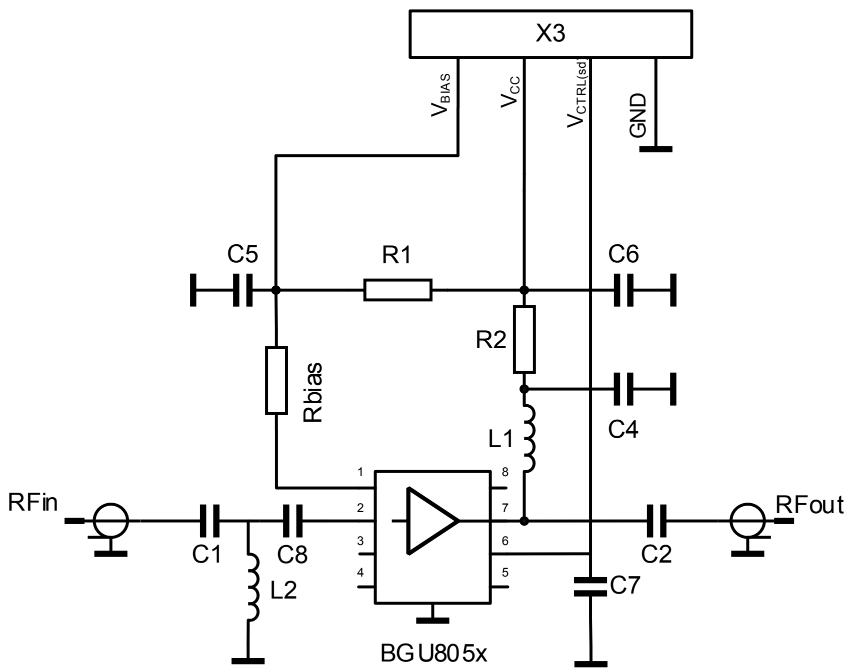
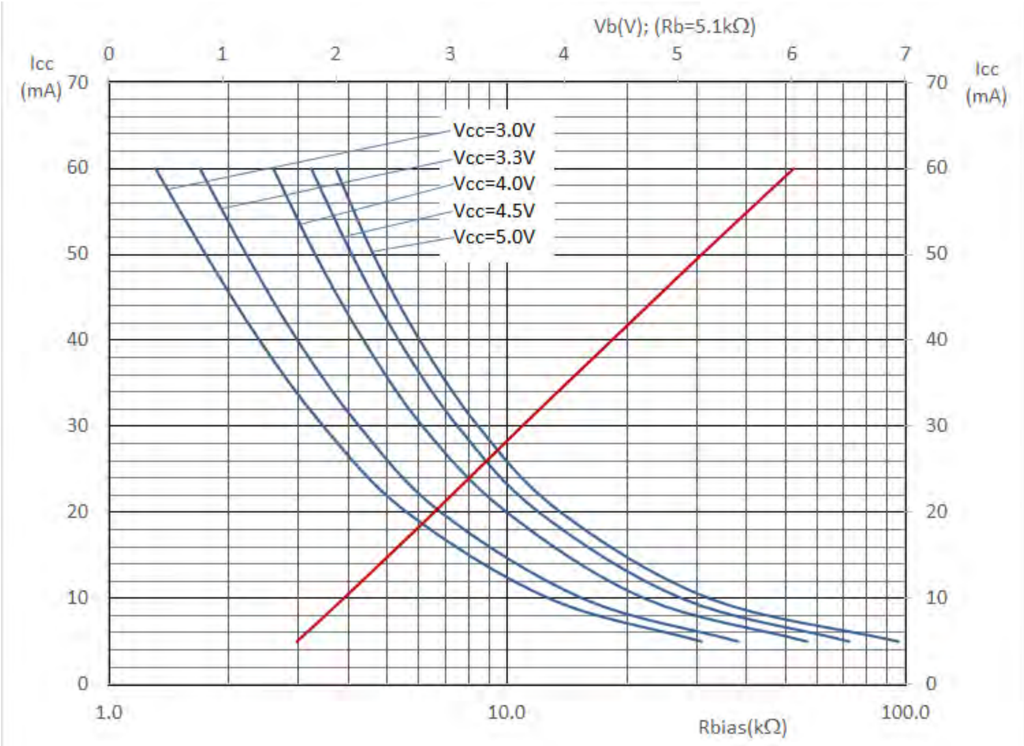



**Fig 3. BGU8051 450 MHz application circuit diagram**

As already indicated the bias current of the BGU8051 can be set by the value $R_{BIAS}$. The evaluation boards are supplied with a 5.1 kΩ bias resistor ($I_{CC}$ = 48 mA +/-5 mA @ $V_{CC}$ = 5 V). If however it is required to evaluate the BGU8051 at different bias currents, resistor R1 which is 0 Ω can be removed and an external control voltage can be applied to $V_{BIAS}$ ($V_b$ pin) on the bias header X3, see Fig 3.

By applying this separate bias voltage on the $V_{BIAS}$ pin of the bias header X3, the $I_{CC}$ current can be swept without changing $R_{BIAS}$. With bias voltage window from 1.5 to 6 V on $V_{BIAS}$ while keeping the $V_{CC}$ pin on 5 V, $I_{CC}$ can be varied from 5-60 mA. In Fig 4 the relation between $I_{cc}$ and $R_{BIAS}$ at $V_{CC}$ = 5 V as well as the relation between $I_{CC}$ and $V_{BIAS}$ with $R_{BIAS}$ = 5k1 is shown. In Fig 4 you can also find the bias resistor values when applying the BGU8051 at lower supply voltages. Which indicates the BGU805x series can also be biased with lower voltage e.g. 3.3 V and makes it excellent suitable for small cells. In paragraph 4.1 typical performance of the LNA @ 3.3 V 48 mA is also included.




(1) Blue curve corresponds with the left Y axis and the lower X axis. Giving the $I_{CC}$ versus the value of $R_{BIAS}$.

(2) Red curve corresponds with the right Y axis and the upper X axis. Giving the $I_{CC}$ versus the voltage applied to the $V_b$ pin with $R_{BIAS}$ = 5k1 in place.

**Fig 4. Relation of $I_{CC}$ with $R_{BIAS}$ and $V_b$ of the BGU8051**

## 3.2 PCB Layout information & component selection.

- A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board can serve as a guideline for laying out a board using the BGU8051.
- The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output lines.
- $V_{CC}$ is decoupled by C4 and C6 decoupling capacitors, C4 should be located as close as possible to the device, to avoid AC leakage via the bias lines. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device.
- The self-resonance frequency of inductor L1 should be chosen above frequency band of interest for good choking. In this case the Murata LQW15 series has been used.
- Inductor L2 and capacitor C8 are creating the high pass matching structure and are in that sense critical, to the input return loss at the frequency of interest.
- C1 and C2 are DC blocking capacitors, and not critical, C1 might not be necessary if a previous stage is not driving DC current. If C1 however is used and it should be <100 pF for short turn on/off time.
- C5 is not mounted on the evaluation boards, but can be used as additional $V_{CC}$ decoupling, but is not critical to the RF performance.

- C7 is used to decouple the shutdown pin.
- R2 increases the low frequency stability.
- Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BGU8051 evaluation board is given in Fig 5

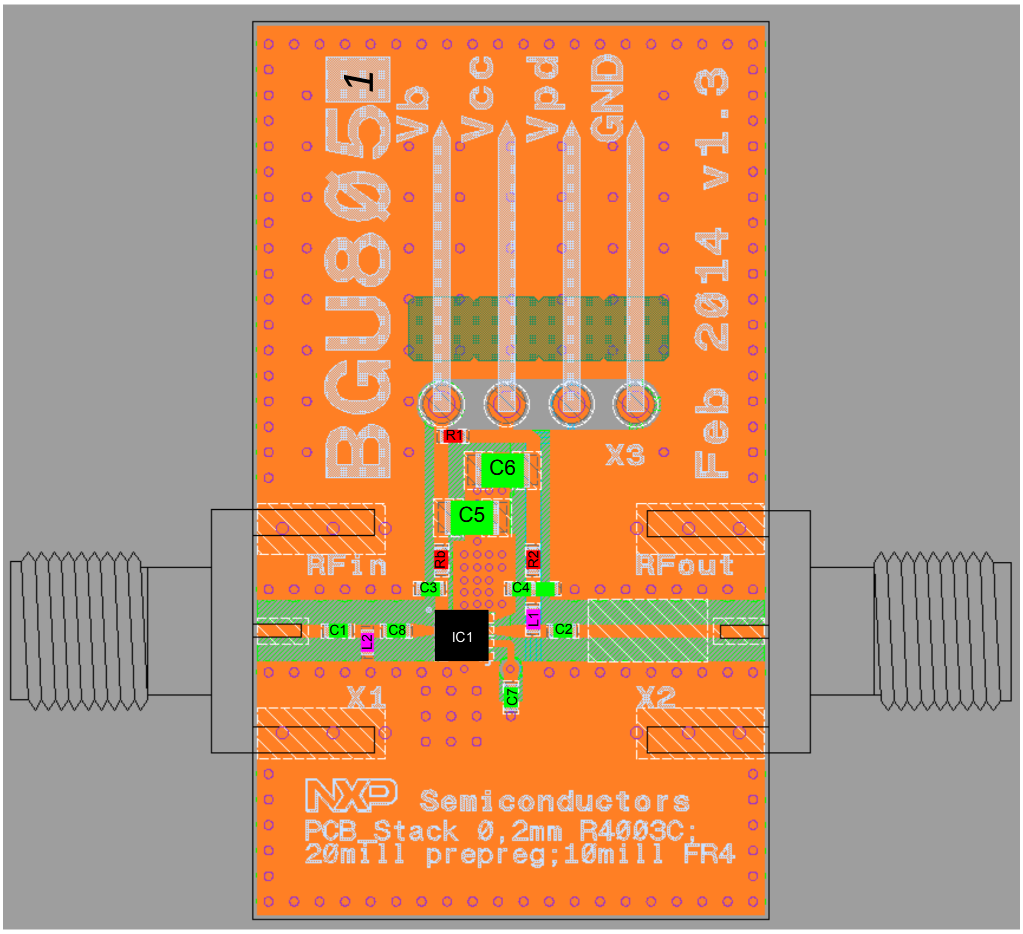
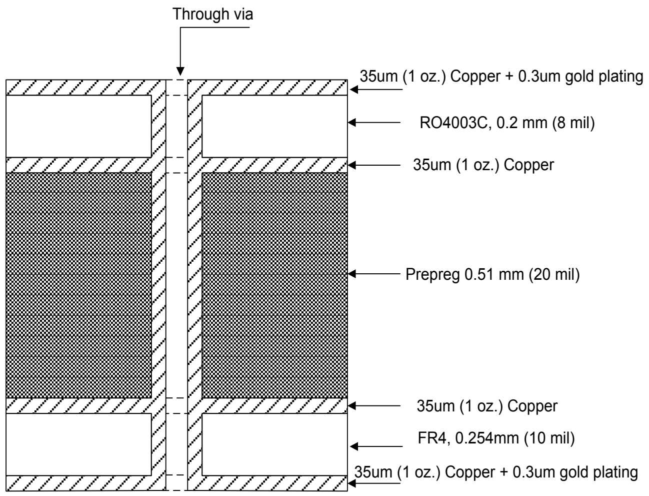



**Fig 5. BGU8051 450MHz evaluation board component placement**

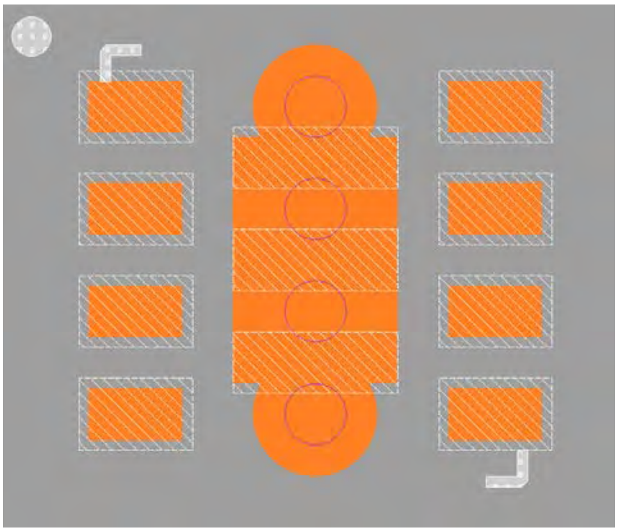
### 3.2.1 PCB stack and recommended footprint.

The PCB material used to implement the LNA is a 0.2 mm (8 mil) RO4003C low loss printed circuit board which is merged to a 0.51 mm (20 mil) prepreg and a 0.254 mm (10 mil) FR4 layer for mechanical stiffness. See Fig 6a

The official drawing of the recommended footprint can be found via following link, sot1327-1_fr.pdf. If micro strip coplanar PCB technology is used it is recommended to use at least 4 ground-via holes of 300 um, this is also used on the EVBs as shown in Fig 6b.




a. Cross section of the PCB Layer stack.



b. Recommended footprint.

**Fig 6. PCB stack and footprint information.**

## 3.3 Bill of materials

Table 1 gives the bill of materials as used on the EVB.

**Table 1. BOM**

| Designator | Description | Footprint | Value | Supplier Name/type | Comment/function |
|---|---|---|---|---|---|
| IC1 | BGU8051 | | | | |
| PCB | 20 x 35 x 1 mm | | | KOVO | RO4003 PCB v1.3 |
| C1,C2 | Capacitor | 0402 | 100pF | Various | DC block |
| C4 | Capacitor | 0402 | 1nF | Various | RF decoupling |
| C5 | Capacitor | 0806 | 4.7uF | Various | Optional |
| C6 | Capacitor | 0806 | 4.7uF | Various | LF Decoupling |
| C7 | Capacitor | 0402 | 10pF | Various | Decoupling |
| C8 | Capacitor | 0402 | 100pF | Various | Input matching |
| L1 | Inductor | 0402 | 47nH | Murata LQW15 | Bias choke/Output match |
| L2 | Inductor | 0402 | 39nH | Murata LQW15 | Input matching |
| R1 | Resistor | 0402 | 0Ohm | Various | |
| R2 | Resistor | 0402 | 10Ohm | Various | stability |
| Rbias | Resistor | 0402 | 5k1 | Various | Bias setting |
| X1,X2 | SMA RF connector | | | Johnson, End launch SMA 142-0701-841 | RF connections |
| X3 | DC header | | | Molex, PCB header, right angle, 1 row 4 way | DC connections |

# 4. Measurement results

## 4.1 Typical board performance

The values given in Table 2 are typical values of >25 boards measured on the fully automated test setups shown in Fig 13.

**Table 2. Typical board performance.**

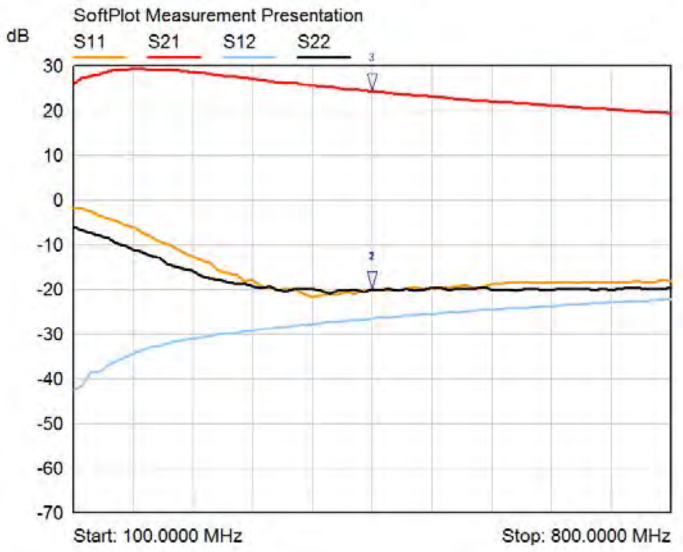
*F = 450 MHz; $T_{AMB}$=25 °C; input and output 50 Ω; $R_{BIAS}$ = 5.1 kΩ.*

| Symbol | Parameter | Conditions | Typ | Typ | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Voltage | | 5 | 3.3 | V |
| $I_{cc}$ | Supply current | | 48 | 48 | mA |
| $G_{ass}$ | Associated gain | | 24.4 | 24.3 | dB |
| NF | Noise figure | [1] | 0.46 | 0.46 | dB |
| $P_{L((1dB)}$ | Output power at 1 dB gain compression | | 19 | 16.1 | dBm |
| $IP3_O$ | Output third-order intercept point | 2-tone; tone spacing = 1 MHz; $P_i$ = -22 dBm per tone | 35 | 34.8 | dBm |
| $RL_{in}$ | Input return loss | | 20 | 19.6 | dB |
| $RL_{out}$ | Output return loss | | 20 | 20.8 | dB |
| ISL | Isolation | | 27.2 | 26.4 | dB |
| $T_{s(pon)}$ | Power-on settling time | $P_i$ = -20 dBm; SHDN(pin 6) from High to Low | 1.6 | 1.6 | μs |
| $T_{s(poff)}$ | Power-off settling time | $P_i$ = -20 dBm; SHDN(pin 6) from Low to High | 0.05 | 0.05 | μs |

[1] Board losses of about 0.05 dB have been de-embeded

## 4.2 S-parameters.

The measured S-parameters are given in Fig 7. For the measurements, a typical BGU8051 450 MHz EVB is used. All the S-parameter measurements have been carried out using the setup in Fig 13a



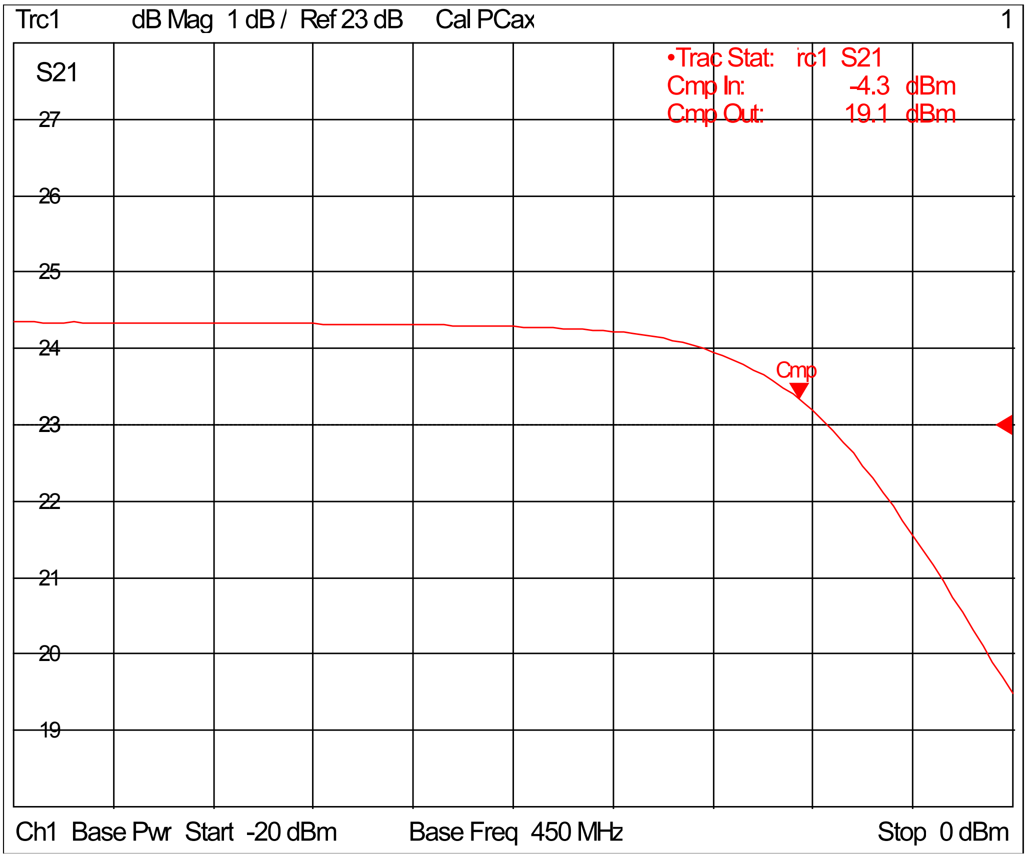

| Mkr | Trace | X-Axis | Value | Notes |
|---|---|---|---|---|
| 1 ∇ | S11 | 450.0000 MHz | -20.02 dB | |
| 2 ∇ | S22 | 450.0000 MHz | -20.00 dB | |
| 3 ∇ | S21 | 450.0000 MHz | 24.36 dB | |

(1) $V_{CC}$ = 5 V, $I_{CC}$ = 48 mA; $T_{amb}$=25' C

**Fig 7. BGU8051 450 MHz LNA narrow band S-parameters**

## 4.3 1dB Gain compression point.

The measured Gain versus input power is given in Fig 8. For the measurements, a typical BGU8051 450MHz EVB is used. All the P1dB measurements have been carried out using the setup in Fig 13a



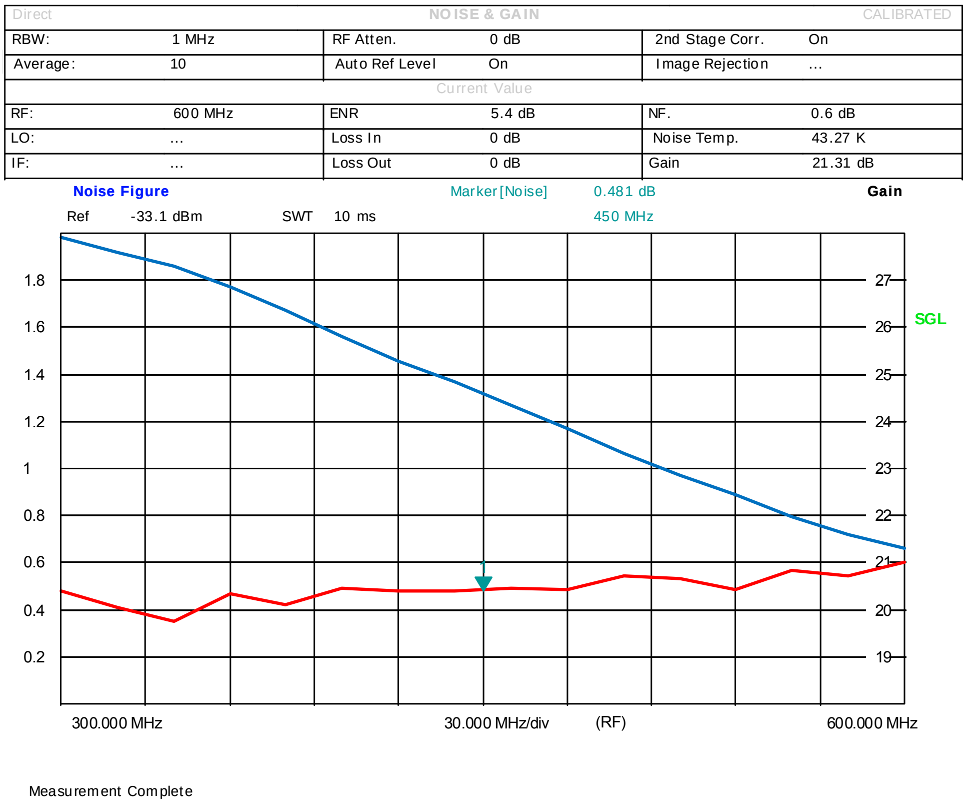

(1) $V_{CC}$ = 5 V; $T_{AMB}$ = 25 °C; $I_{CC}$ = 48 mA

(2) $P_i$1dB = -4.3 dBm; $P_L$1dB = 19.1 dBm

**Fig 8. BGU8051 450MHz LNA 1dB gain compression**

## 4.4 Noise figure

The measured noise figure are given in Fig 9. For the measurements, a typical BGU8051 450 MHz EVB is used. All the S-parameter measurements have been carried out using the setup in Fig 13b



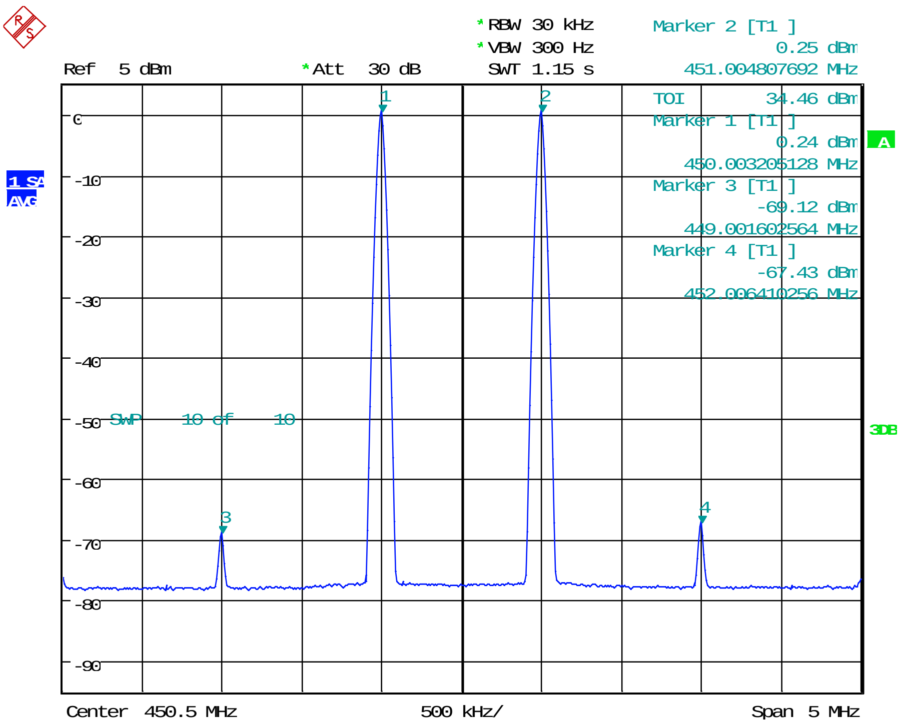

(1) $V_{CC}$ = 5 V; $T_{AMB}$ = 25 °C; $I_{CC}$ = 48 mA

(2) Measured at the evaluation boards SMA connectors, so PCB losses are not corrected.

**Fig 9. BGU8051 450MHz LNA typical noise figure performance**

## 4.5 3rd order intercept point, output referred

The evaluation board provided in the customer evaluation kit is automatically measured on linearity using the set-up shown in Fig 13 a Alternatively the setup given in Fig 13 c can be used, which is done for the spectrum plot in Fig 10. For the measurements, a typical BGU8051 450MHz EVB is used.



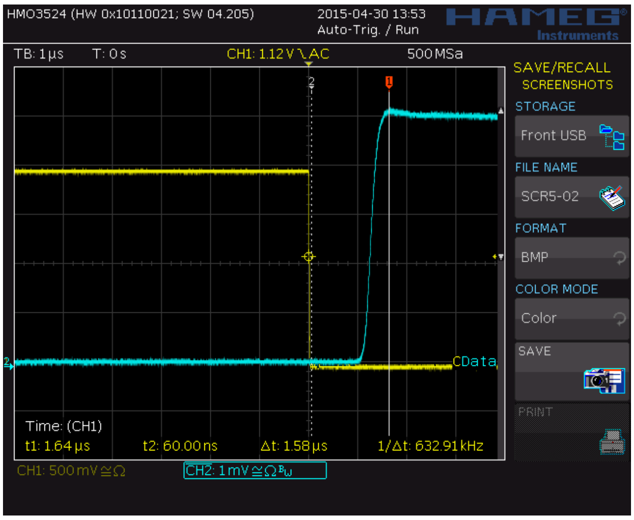

(1) $IP3_O$ (LSB) = (69.12+0.24)/2+0.24=34.9 dBm; $IP3_O$ (USB)=(67.43+0.25)/2+0.25=34.1 dBm

(2) $IP3_i$ = $IP3_O$ -Gain=34.5-24.5 = 10 dBm

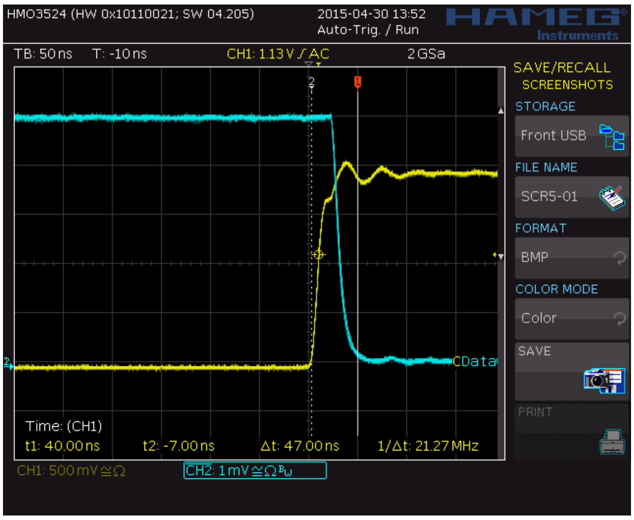
**Fig 10. BGU8051 450MHz LNA Typical OIP3 spectrum**

### 4.6 Power on/off settling time.

The power on/off settling time curves shown in Fig 11 and Fig 12 are being measured using the setup shown in Fig 13d and described in paragraph 5.5



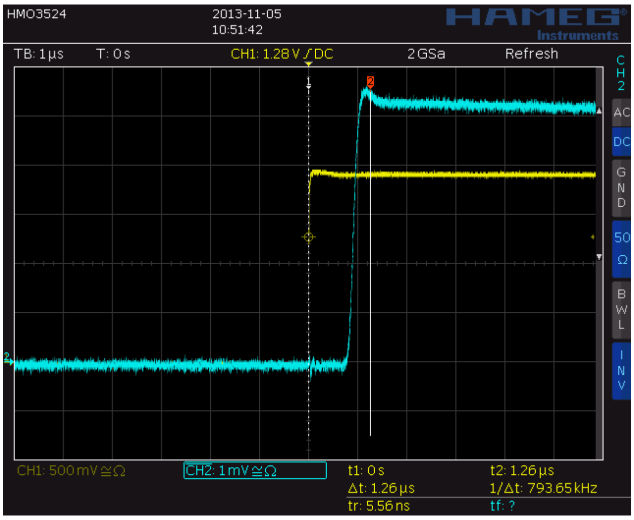

a. $T_{on}$ 1.58 µs



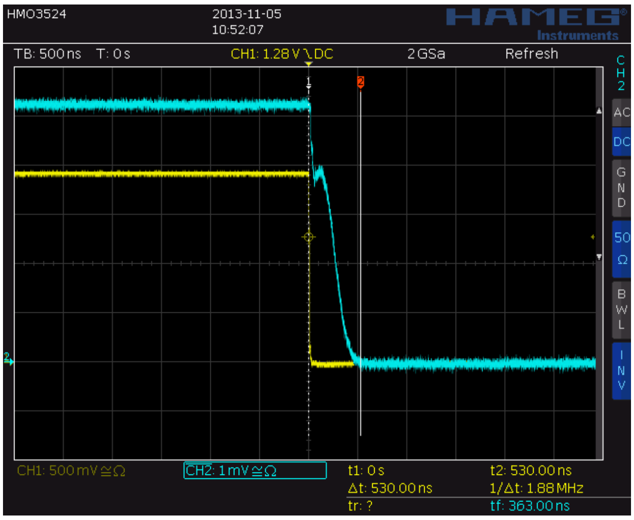

b. $T_{off}$ 47 ns

Yellow curve SHDN control voltage
Blue curve output of the detector diode

**Fig 11. Power on/off settling time using the SHDN pin(6)**




c. $T_{on}$ 1.26 µs




d. $T_{off}$ 530 ns

Yellow curve $V_{BIAS}$ control voltage
Blue curve output of the detector diode

**Fig 12. Power on/off settling time using the $V_{BIAS}$ pin(1)**

**Table 3. Typical power on/off settling time**
*Measured on BGU8051 450MHz EVB*

| Control pin | Power on | Power off | Units |
|---|---|---|---|
| SHDN | 1.6 | 0.05 | µs |
| $V_{BIAS}$ | 1.3 | 0.53 | µs |

# 5. Measurement methods and setups.

## 5.1 Required Measurement Equipment

In order to measure the evaluation board, the following is necessary:

- ✓ 2 (channel) DC Power Supply up to 100 mA at 5 V, to set $V_{CC}$ and eventual Vbias.
- ✓Two RF signal generators capable of generating RF signals up to 2 GHz
- ✓An RF spectrum analyzer that covers at least the operating frequencies and a few of the harmonics. Up to 6 GHz should be sufficient.
- ✓A network analyzer for measuring gain, return loss and reverse isolation
- ✓Noise figure analyser and noise source
- ✓Proper RF cables with male SMA connectors.

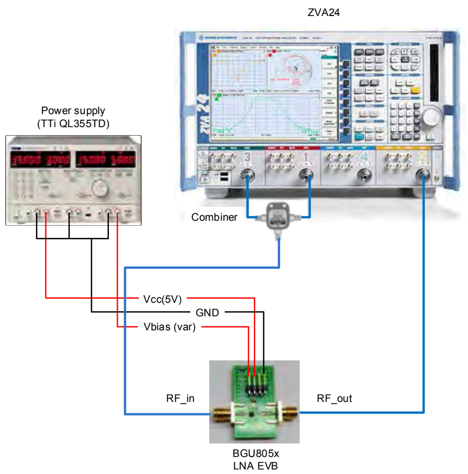
## 5.2 Connection and setup

The typical values shown in this report have been measured on the fully automated test setups shown in Fig 13.

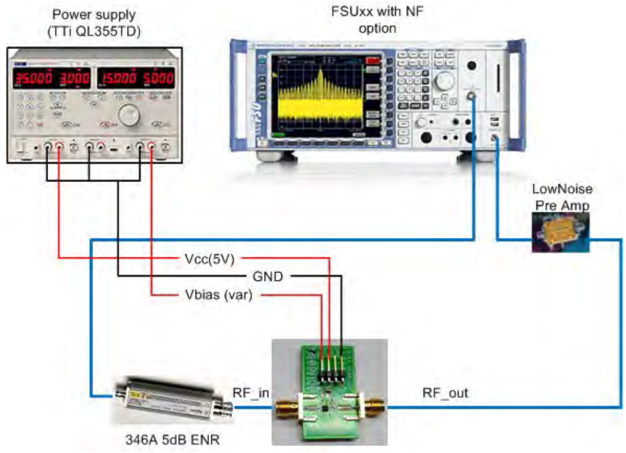
Please follow the steps below for a step-by-step guide to operate the LNA evaluation board and testing the device functions.

1. Connect the DC power supply to the $V_{CC}$ and GND terminals. Set the power supply to 5 V.
2. Connect the RF signal generator and the spectrum analyzer to the RF input and the RF output of the evaluation board, respectively. Do not turn on the RF output of the signal generator yet, set it to approximately -30 dBm output power at the center frequency of the wanted frequency band and set the spectrum analyzer at the same center frequency and a reference level of 0 dBm.
3. Turn on the DC power supply and it should read approximately 48 mA.
4. Enable the RF output of the generator: The spectrum analyzer displays a tone around –5.4 dBm.
5. Instead of using a signal generator and spectrum analyzer one can also use a network analyzer in order to measure gain as well as in- and output return loss and P1dB (see Fig 13a)
6. For noise figure evaluation, either a noise figure analyzer or a spectrum analyzer with noise option can be used. The use of a 5 dB noise source, like the Agilent 364B, is recommended. When measuring the noise figure of the evaluation board, any kind of adaptors, cables etc. between the noise source and the evaluation board should be minimized, since this affects the noise figure (see Fig 13b).

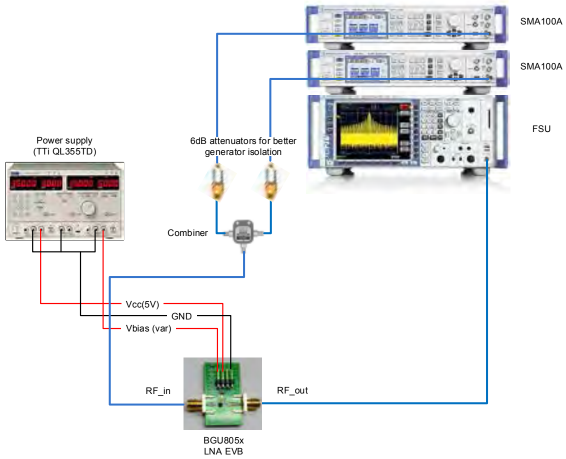
 



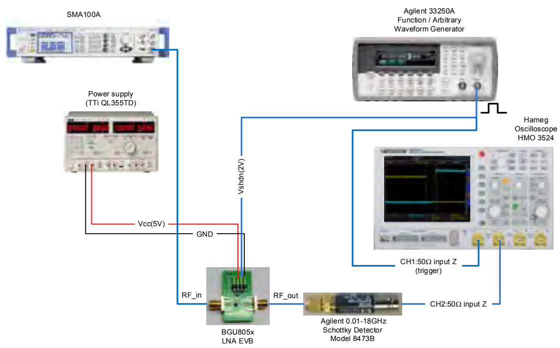

a. S_ parameter; P1dB and IP3o test setup




b. Noise figure test setup




c. Third order intercept point test setup




d. Power on/off settling time test setup

**Fig 13. Characterization measurements setups.**

## 5.3 Noise figure measurement setup

In Fig 13b the noise figure measurement set-up is shown, this is intended as a guide only, substitutions can be made. For sub 1 dB noise figure levels like the BGU8051 has it is recommended to perform the noise-measurements in a Faraday's cage or at least put the DUT in a shielded environment. This is recommended to avoid any interference of cellular frequencies that are in the same frequency range. A spectrum analyzer with noise option. A 5dB ENR noise source was used. To achieve the lowest possible setup noise figure an external pre amplifier is also recommended. The Noise figure value in Fig 9 is the value measured at the evaluation board SMA connectors. Correcting for the connector and PCB loss will end up in 0.05dB lower noise figure.

## 5.4 Third order intercept

The bias choke L1 on the application board is determined empirically in order to get the best OIP3 as well as keeping good output return loss. The low ohmic source impedance provided by the matching circuit L1 and C8 also improves the linearity. In [1] the effect on linearity of SiGe BiCMOS BJTs and the advantage of using low source impedances at the low frequencies of the 2$^{nd}$ order mixing terms is described. When measuring the high OIP3 values it is essential check the capabilities of the used measurement equipment. Be aware that the measurement set-up itself is not generating dominating IM3 levels. Advised is to do a THRU measurement without a DUT first.

## 5.5 Power on/off settling time

When using the BGU8051 in TDD applications power on/off switching can be controlled via both the SHDN pin as well as the $V_{bias}$ pin. It is preferred to use the SHDN pin. Both pins require less than 1 mA driving current which means they are CMOS compatible. This enables LNA switching directly via a micro controller.

The setup used to measure the power on/off settling time is shown in Fig 13d. This can be used as a guidance to determine the power on/off settling time. The waveform generator is used to provide the control voltage on either the SHDN pin (6) or the $V_{BIAS}$ pin (1).

Set the waveform generator Agilent 33250 to square mode and the output amplitude to required voltage for the used control pin, with 50 Ω output impedance. Set the RF signal generator output level to -25 dBm at 450 MHz and increase its level until the peak detector output level is about 5 mV on 1 mV/division, the signal generator RF output level is approximately -20 dBm.

A peak detector is needed to detect the high frequency AC signal at the output of the DUT, representing it as a DC voltage equal to the peak level of the applied AC signal.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized. It is also critical to set the oscilloscope input impedance to 50 Ω on channel 2 so the diode detector can discharge quickly to avoid a false result on the Turn OFF time testing.

## 6. References

[1] Vladimir Aparin, Lawrence E. Larson, “Linearization of monolithic LNAs Using Low-Frequency Low-Impedance Input Termination”. IEEE 0-7 803-8 108-4/03 ©2003

## 7. Customer Evaluation Kit

In the customer evaluation kit you will find;

- One 450 MHZ BGU8051 EVB
- 10 loose BGU8051 samples.


a. b.

**Fig 14. BGU8051 450MHz LNA Customer evaluation KIT**

# 8. Legal information

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