AN11374

Pin FMEA for NX3P switches

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Document information

Info	Content
Keywords	FMEA
Abstract	This application note provides a Failure Modes and Effects Analysis (FMEA) for the device pins of NXP Semiconductors logic controlled high side NX3P series power switches

Revision history

Rev	Date	Description
v.1	20130805	initial version

Contact information

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1. Introduction

The NX3P high-side load switch family, features a low ON resistance P-channel MOSFET that supports more than 500 mA of continuous current. Designed for operation from 1.1 V to 3.6 V, it is used in power domain isolation applications to reduce power dissipation and extend battery life. The enable logic includes integrated logic level translation making the device compatible with lower voltage processors and controllers. Low ground current and ultra-low shutdown current make it ideal for portable, battery operated applications. Some devices have a discharge resistor connected to V_{out} to discharge the output capacitance when disabled.

2. Pin FMEA

This chapter provides an FMEA (Failure Mode and Effect Analysis) for typical failure situations for the NX3P high-side load switch family. The failure occurs when the pins in the logic controlled power switch, are short circuited to supply IO, GND or neighboring pins or simply left open.

The individual failures are classified, according to their corresponding effects on a device and the functionality; see Table 1.

Table 1. Classification of failure effects

Class	Failure effect
A	damage to this device
	functionality of application affected
B	no damage to this device
	functionality of application may be affected
C	no damage to this device
	functionality of application not affected

Table 2. FMEA matrix for pin short-circuit to Supply IO

Pin	Class	Remarks
Input	B	no damage to this device, functionality is affected
GND	A	short-circuits and high currents can damage device, functionality is affected

Table 3. FMEA matrix for pin short-circuit to GND

Pin	Class	Remarks
Input	B	no damage to this device, no leakages, functionality may be affected
Supply IO	-	see Table 2

Table 4. FMEA matrix for pin left open

Pin	Class	Remarks
Input	B	undefined operating condition, no damage, increased leakage, functionality may be affected
GND	B	undefined operating condition, no damage, increased leakage, functionality is affected
Supply IO	B	undefined operating condition, no damage, increased leakage, functionality is affected

Table 5. FMEA matrix for pin short-circuits between neighbor pins

Pin	Class	Remarks
Input to supply IO	-	see Table 2
GND to supply IO	-	see Table 3
Supply input to supply output	B	no damage to this device, functionality is affected, types with discharge resistor have increased leakage

2.1 Pin name mapping

Supply IO: VIN, VOUT

Input: EN, /EN

3. Abbreviations

Table 6. Abbreviations

Acronym	Description
FMEA	Failure Mode and Effect Analysis

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