AN11266

Application and soldering information for the PCF2127 TCXO RTC

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Document information

Info	Content
Keywords	PCF2127, application, timekeeping, timestamp, soldering
Abstract	This application note gives additional information about soldering and application configuration of the PCF2127 TCXO RTC

Revision history

Rev	Date	Description
v.2	20141218	revised version
v.1	20130208	new application note, initial release

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1. Introduction

This application note provides additional information on the PCF2127 TCXO RTC.

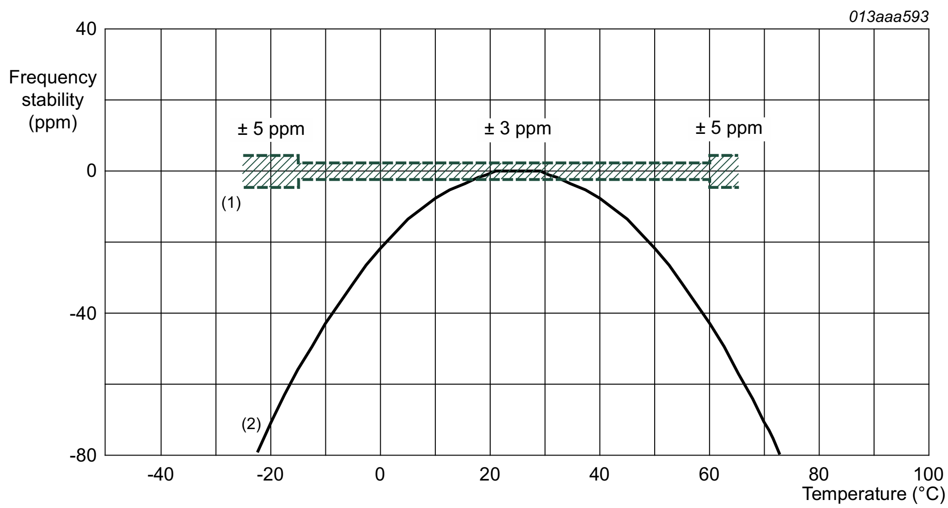
The accuracy of time given by an RTC is mostly depending on the accuracy of the crystal used. For example, a tuning fork crystal resonates at room temperature at its nominal frequency but slows down when the temperature deviates (see graph no. 2 in Figure 1 and Figure 2).

The PCF2127 is a CMOS Real Time Clock (RTC) and calendar IC. It has an integrated Temperature Compensated Crystal (Xtal) Oscillator (TCXO) based on an integrated 32.768 kHz tuning fork quartz crystal. The PCF2127 is optimized for very high accuracy and very low power consumption. It compensates automatically for temperature-dependent frequency deviations (see Figure 1 and Figure 2).

For further information (e.g. pinning diagram and register organization), refer to the data sheet Ref. 5 "PCF2127".

2. Frequency stability and time accuracy

Figure 1 and Figure 2 show the typical frequency stability of the PCF2127 with respect to the temperature in comparison to an uncompensated tuning fork crystal.

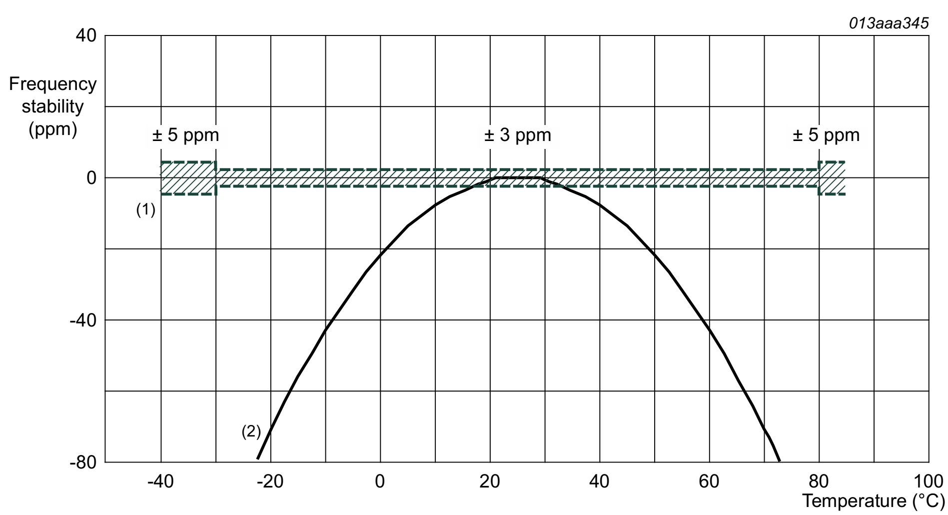


V_{DD} or V_{BAT} = 3.3 V.

(1) Typical temperature compensated frequency response.

(2) Uncompensated typical tuning-fork crystal frequency.

Fig 1. Typical characteristic of frequency with respect to temperature of PCF2127AT



V_{DD} or V_{BAT} = 3.3 V.

(1) Typical temperature compensated frequency response.

(2) Uncompensated typical tuning-fork crystal.

Fig 2. Typical characteristic of frequency with respect to temperature of PCF2127T

Remark:

- For V_{DD} or V_{BAT} other than 3.3 V, a frequency shift of ±1 ppm/V has to be expected.
- For information about frequency correction, see Section 4.4.

3. Frequency measurement

The frequency stability can be evaluated by measuring the frequency of the square wave signal available at the output pin CLKOUT.

The frequency signal at pin CLKOUT is controlled by the COF[2:0] control bits in register CLKOUT_ctl (0Fh) according to Table 1.

Table 1. CLKOUT frequency selection

COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]
000	32768	60 : 40 to 40 : 60
001	16384	50 : 50
010	8192	50 : 50
011	4096	50 : 50
100	2048	50 : 50
101	1024	50 : 50
110	1	50 : 50
111	CLKOUT = high-Z	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

The selection of f_{CLKOUT} = 32.768 kHz (COF[2:0] = 000, default value) leads to lower accuracy. It is therefore recommended to select a frequency other than the default value of 32.768 kHz for accurate frequency measurements. The most accurate frequency measurement occurs when 1 Hz is selected.

In order to be able to adjust the clock with accuracy better than 1 ppm, the frequency counter used to check the output at CLKOUT should have at least an 8-digit reading.

Furthermore, for accurate evaluation of the frequency stability over temperature, it is important that the frequency measurement is executed when the temperature is stable and the PCF2127 performed the temperature measurement. The PCF2127 measures the temperature immediately after power-on and then periodically with a period set by the temperature conversion rate bits TCR[1:0] in register CLKOUT_ctl (0Fh):

Table 2. Temperature measurement interval

TCR[1:0]	Temperature measurement interval
00[1]	4 min
01	2 min
10	1 min
11	30 seconds

[1] Default value.

Once the temperature is set and is stable, it is necessary to wait until the PCF2127 has performed the temperature measurement, then the frequency can be measured at the CLKOUT pin. To perform quicker measurements, it is recommended to select the temperature measurement period of 30 seconds (TCR[1:0] = 11).

In summary, for an accurate evaluation of the frequency stability the following operating flow is recommended:

- Power-on with V_{DD} = 3.3 V
- Wait until the 32.768 kHz signal is available at the CLKOUT pin
- Program a COF[2:0] value other than the default, for example COF[2:0] = 110, which corresponds to f_{CLKOUT} = 1 Hz
- Program TCR[1:0] = 11, which corresponds to a temperature measurement period equal to 30 seconds
- Set the target temperature
- Wait until temperature is stable
- Wait until the temperature measurement is executed (~30 seconds after the temperature is stable)
- Measure the frequency at the CLKOUT pin.

4. Reflow soldering

4.1 Introduction to reflow soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs) to form electrical circuits. The soldered joint provides both, the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one Printed-Circuit Board (PCB); however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

The PCF2127 is intended for use in a reflow soldering process.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile (see Figure 3); this profile includes preheat (T_s), reflow (in which the board is heated to the peak temperature (T_p)) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged.

For further information on reflow soldering IC, refer to Ref. 1 “AN10365”.

4.2 Reflow soldering of PCF2127

The PCF2127 is intended for use in a lead-free reflow soldering process, classified in accordance with the Ref. 3 “IPC/JEDEC J-STD-020”.

Figure 3 shows the reflow soldering temperature profile according to Ref. 3 “IPC/JEDEC J-STD-020” used for the qualification of the PCF2127.

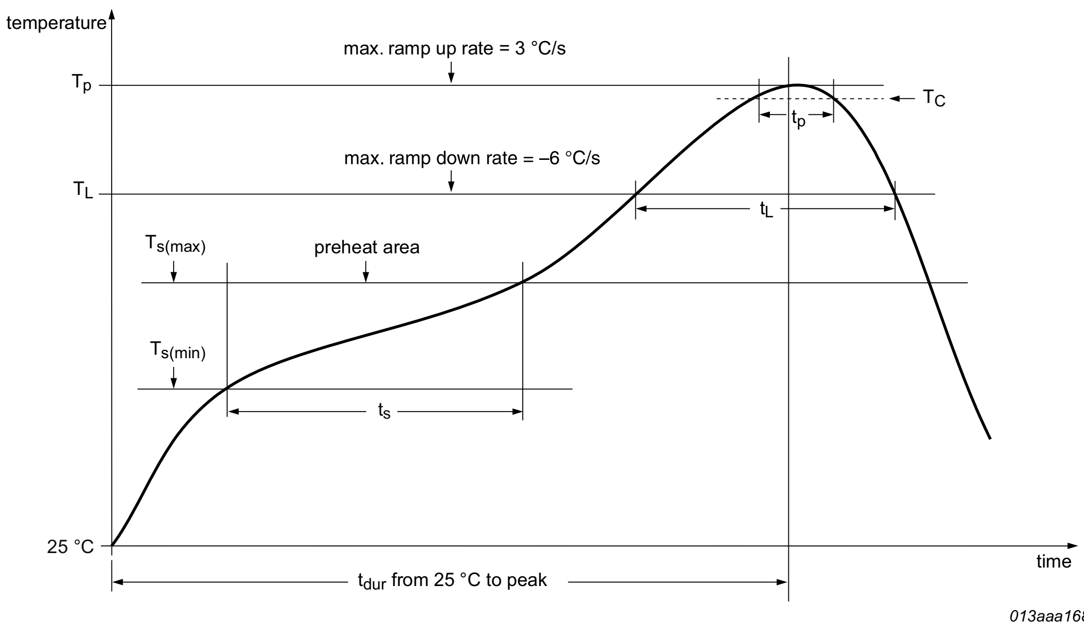


Figure not drawn to scale.

The appropriate values for this graph are shown in Table 3.

Remark: The reflow profile in this document is for classification/preconditioning and not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs, but must not exceed the parameters shown in Table 3.

Fig 3. Reflow temperature profile

Table 3. Values of reflow temperature profile

All temperatures refer to the center of the package, measured on the package body surface that is facing up during the reflow soldering process.

Symbol	Value	Unit
T_p	260	°C
T_L	217	°C
T_C	255	°C
$T_{s(max)}$	200	°C
$T_{s(min)}$	150	°C
t_p	30	s
t_L	60 to 150	s
t_s	60 to 120	s
t_{dur}	max 480	s

Recommendations:

1. The reflow soldering profile shown in Figure 3 is recommended. A full convection reflow system, capable of maintaining the reflow profile of Figure 3, is recommended.
2. The peak temperature (T_p) of the reflow soldering process must not exceed 260 °C. If the temperature exceeds 260 °C, the characteristics of the crystal oscillator is degraded or the device may even be damaged.

3. The time, while the PCF2127 is heated above T_C = 255 °C, must not exceed 30 s (t_p), otherwise the characteristics of the crystal oscillator is degraded or the device may even be damaged.

4.3 Effect of reflow soldering on the frequency characteristics

The reflow soldering process is typically generating a negative frequency shift.

After one-time reflow soldering, processed in accordance with the recommended temperature profile shown in Figure 3 and Table 3, a frequency shift of −2 ppm is typical. Any other reflow temperature profile or multiple soldering may cause a different frequency shift after soldering. The frequency shift after soldering can be reduced by lowering the peak temperature T_p and shortening the time t_p of the soldering process (see Figure 3 and Table 3).

4.4 Frequency correction after reflow soldering

In order to compensate for a shift in frequency due to reflow soldering, a frequency offset can be programmed through bits AO[3:0] of register address 19h. In the typical case and under consideration of the temperature profile as given in Figure 3, an offset of +2 ppm is considered to be most suitable. However, this may vary on a per case basis and in dependence of the actual soldering profile used.

Remark:

1. The typical frequency shift of −2 ppm, that occurs after a one-time reflow soldering processed in accordance with the recommended temperature profile shown in Figure 3 and Table 3, can be corrected by programming AO[3:0] = 0110.
2. A frequency measurement (see Section 3) should be performed after the final assembly of the board if
   - the soldering was processed multiple times,
   - the soldering was not made according to the recommended temperature profile,
   - the best result in accuracy should be achieved.

   Then the offset with the appropriate value given in Table 4 should be programmed into AO[3:0]. Deviations caused by assembly steps or due to production tolerances can be compensated with it.

Table 4. Typical frequency correction at 25 °C

AO[3:0]		ppm
Decimal	Binary	
0	0000	+8
1	0001	+7
2	0010	+6
3	0011	+5
4	0100	+4
5	0101	+3
6	0110	+2
7	0111	+1
8	1000[1]	0
9	1001	–1
10	1010	–2
11	1011	–3
12	1100	–4
13	1101	–5
14	1110	–6
15	1111	–7

[1] Default value.

4.5 Optimization at room temperature

Many applications operate in a temperature range of 15 °C to 35 °C most of the time. Therefore it is preferred to optimize the accuracy for this range.

There is a simple way to do this fine-tuning:

1. Measure the frequency at about 25 °C.
2. Calculate the offset to the nominal frequency of 32768.000 Hz.
3. Program the correction value into AO[3:0].

With this method, it is possible to fine-tune the RTC in steps of 1 ppm and ensure an accuracy of ±1 ppm at room temperature.

5. Application information

5.1 Assembly recommendations

It is recommended to

- take precautions when using the PCF2127 with general-purpose mounting equipment in order to avoid excessive shocks that could damage the integrated quartz crystal
- avoid ultrasonic cleaning that could damage the integrated quartz crystal
- avoid in the board layout running signal traces under the package unless a ground plane is placed between the package and the signal line.

5.2 General application information

In general, it can be said that

- the integration of the quartz crystal in the same package as the RTC has the following advantages:
  - elimination of crystal procurement issues
  - elimination of concerns regarding the crystal parameters matching those of the RTC
  - no more crystal PCB layout issues
- the IFS pin must be connected to ground (V_{SS}) to select the SPI-bus
- the IFS pin must be connected to the BBS pin to select the I^2C-bus
- a backup battery can be attached to the V_{BAT} pin to enable the battery switch-over when the main power V_{DD} fails. If V_{BAT} is not used, it has to be connected to ground. If V_{BAT} is used, one of the supplies (V_{BAT} or V_{DD}) has to be turned on before the other
- the battery backed voltage V_{BBS} can be used to supply an external RAM to retain RAM data in battery backup mode. A low leakage decoupling capacitor should be connected from BBS to V_{SS}: suggested value is 1 nF, max 100 nF. If BBS is not used to supply an external IC, the decoupling capacitor between the BBS and V_{SS} pins must always be connected
- CLKOUT and $\overline{\text{INT}}$ are open-drain, active LOW outputs which require external pull-up resistors: maximum pull-up voltage is 5.5 V
- the timestamp input pin $\overline{\text{TS}}$ can be connected to a push button for tamper detection (see Section 5.4).

5.2.1 Current consumption

Current consumption is reduced if the power management functions are disabled (PWRMNG[2:0] = 111). In that case, the

- battery switch-over function is disabled
- battery low detection is disabled
- only one power supply (V_{DD}) is used.

5.3 Battery switch-over applications

The functionality of the battery switch-over is limited by the fact that the power supply V_{DD} is monitored every 1 ms in order to save power consumption. Considering that the battery switch-over threshold value ($V_{th(sw)bat}$) is typically 2.5 V, the power management operating limit ($V_{DD(min)}$) is 1.8 V and that V_{DD} is monitored every 1 ms, the battery switch-over works properly in all cases where V_{DD} falls with a rate lower than 0.7 V/ms, as shown in Figure 4:

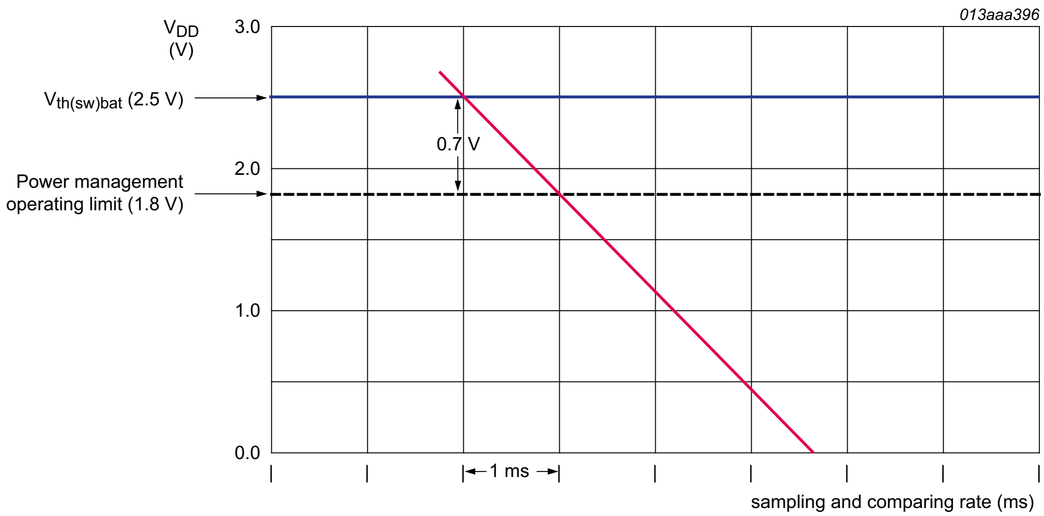


Fig 4. Supply voltage with respect to sampling and comparing rate

In an application, where during power-down, the current consumption on pin V_{DD} is

- in the range of a few µA a capacitor of 100 nF on pin V_{DD} is enough to allow a slow power-down and the proper functionality of the battery switch-over[1]
- in the range of a few hundreds of µA, the value of the capacitor on pin V_{DD} must be increased to force a falling gradient of less than 0.7 V/ms on pin V_{DD} to assure the proper functionality of the battery switch-over[2]
- higher than some mA it is recommended to add an RC network on the V_{DD} pin, as shown in Figure 5.

A series resistor of 330 Ω and a capacitor of 6.8 µF assure the proper functionality of the battery switch-over even with very fast V_{DD} slope.

Note that:

- it is not suggested to assemble a series resistor higher than 1 kΩ because it would cause a large voltage drop
- lower values of capacitors are possible, depending on the V_{DD} slope in the application.

1. Like in the case of no interface activity and/or early power fail detection functions that allow the microcontroller to perform early backup operations and to set power-down modes.
2. Like in the case of interface activity.

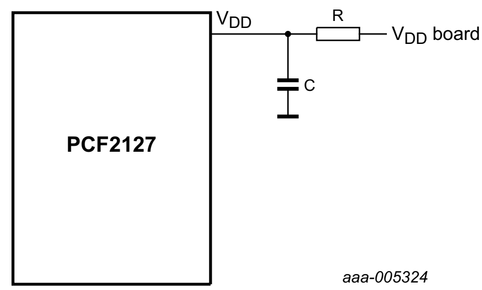


Fig 5. RC network on pin V_{DD}

5.4 Timestamp applications

The most common application of the timestamp function is a tamper detection: date and time are stored when the cover of the equipment is opened. A push button is attached to the cover in such a way, that when the cover is opened, the button is pushed (mechanical connection); the button is connected to the timestamp input pin so that when the button is pushed, the timestamp circuit detects the event, sets a flag and stores the date and time in internal registers.

The timestamp function integrated in the PCF2127 allows double tamper detection in an application, although with a single timestamp input pin. Two push-buttons can be connected to the timestamp input pin. Time and date are stored when one of the push-buttons is pushed.

A typical application is an electrical meter, where one cover protects the terminal (terminal case) and another cover protects the electronics (electronic case) and an opening of each of them should be registered.

Figure 6 shows the double tamper detection application.

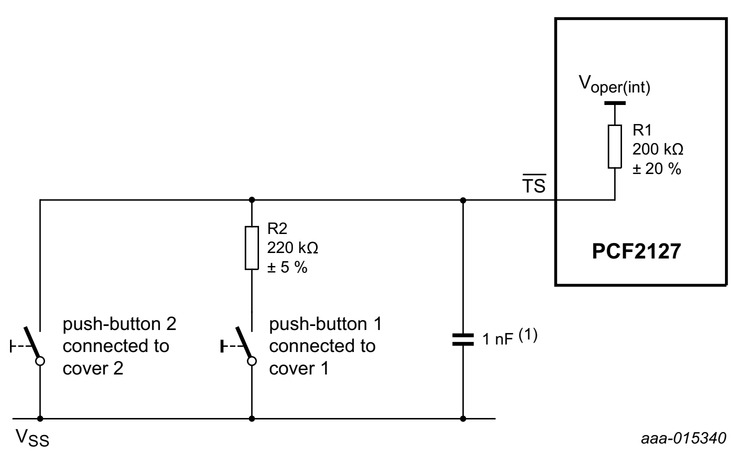


Fig 6. Tamper detection circuit with two push-buttons

- When cover 1 is opened, the push button 1 is closed and the $\overline{TS}$ pin is driven to the intermediate level $V_{TS\_n} = \frac{R2}{R1 + R2} \times V_{DD} \cong \frac{V_{DD}}{2}$. For proper functionality R2 = 220 kΩ with a maximum variation of ±5 %, and a low resistive push button must be used.

  Event 1: TSF1 is set, date and time is registered.
- When cover 2 is opened, the push button 2 is closed and the $\overline{TS}$ pin is driven to ground.

  Event 2: TSF1 and TSF2 are both set, date and time is registered.

5.5 Timekeeping applications

For using the time keeping functions of the PCF2127, see Figure 7:

- CLKOUT is disabled (COF[2:0] = 111)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)

Timekeeping is very accurate due to the temperature compensation. The power consumption is minimized.

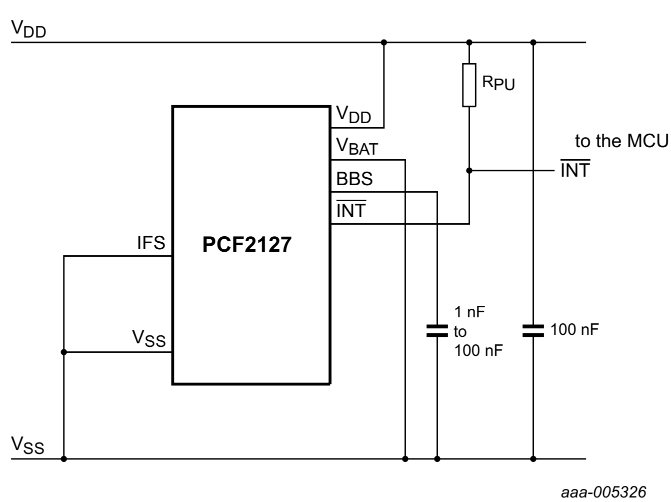


Fig 7. Application diagram: timekeeping

If CLKOUT is enabled during time keeping as described in sections 5.6 to 5.10, the best accuracy is achieved if a CLKOUT frequency other than the default value of 32.768 kHz is selected.

5.6 Timekeeping and CLKOUT

Figure 8 shows the PCF2127 used for timekeeping and CLKOUT functions:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is disabled (TSOFF = 1)

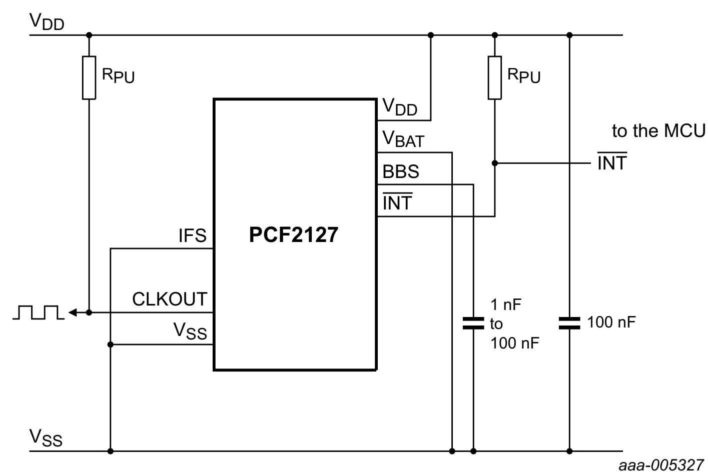


Fig 8. Application diagram: timekeeping and CLKOUT

5.7 Timekeeping, CLKOUT and power management

For using the timekeeping and power management functions of the PCF2127, see Figure 9:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is disabled (TSOFF = 1)

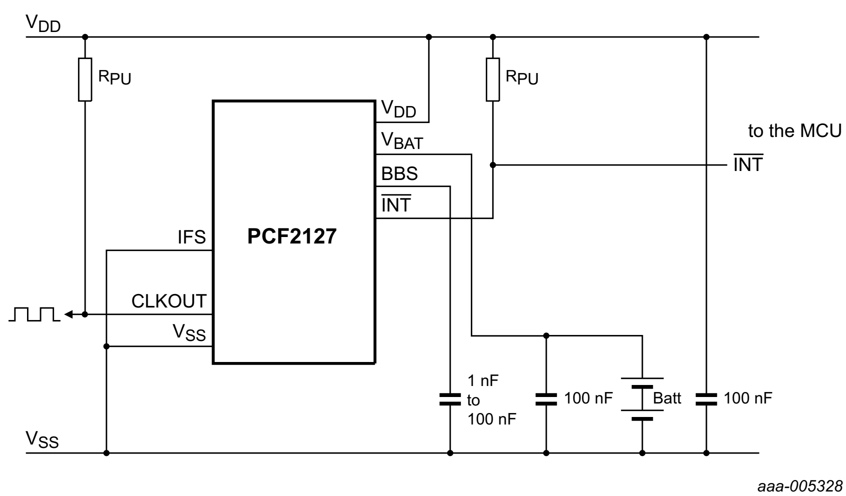


Fig 9. Application diagram: timekeeping, CLKOUT and power management

5.8 Timekeeping, CLKOUT and timestamp

Figure 10 shows the PCF2127 used for timekeeping, CLKOUT and timestamp functions:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- The power management functions are disabled (PWRMNG[2:0] = 111) and pin V_{BAT} is tied to ground
- The timestamp detection is enabled by default (TSOFF = 0), see Figure 6

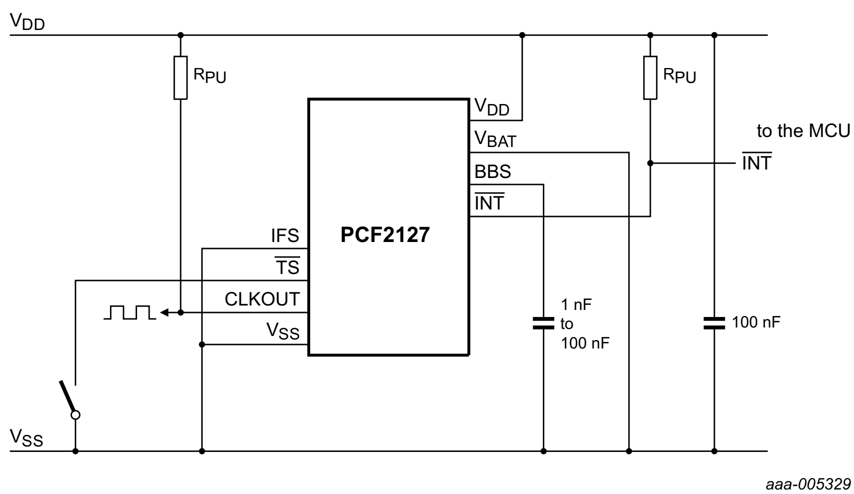


Fig 10. Application diagram: timekeeping, CLKOUT and timestamp

5.9 Timekeeping, CLKOUT, power management and timestamp

For using the timekeeping, power management, CLKOUT and timestamp functions of the PCF2127, see Figure 11:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin, see Section 5.3
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0), see Figure 6

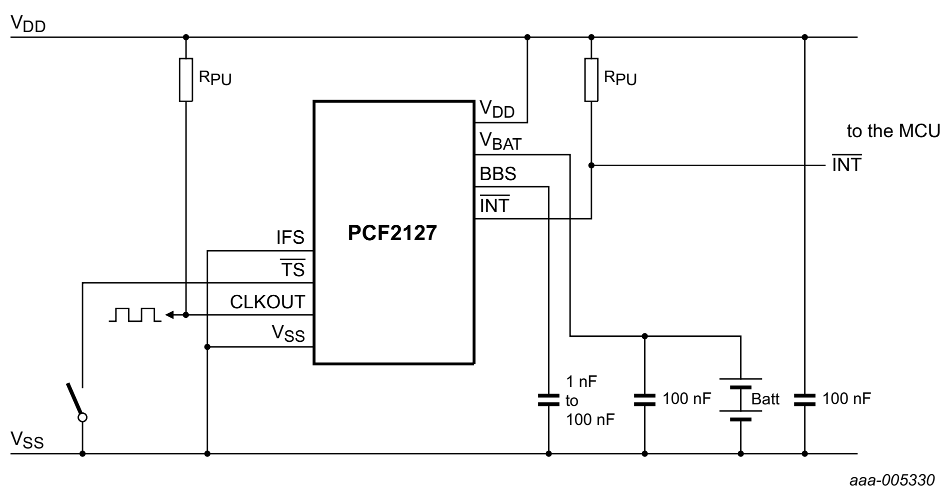


Fig 11. Application diagram: timekeeping, CLKOUT, power management and timestamp

5.10 Timekeeping, CLKOUT, power management, timestamp, battery connected and supply of an external device

Figure 12 shows the PCF2127 used for timekeeping, power management, CLKOUT with a battery connected and supplying an external device:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000), see Section 5.3
- The timestamp detection is enabled by default (TSOFF = 0), see Figure 6
- BBS supplies an external device (SRAM)

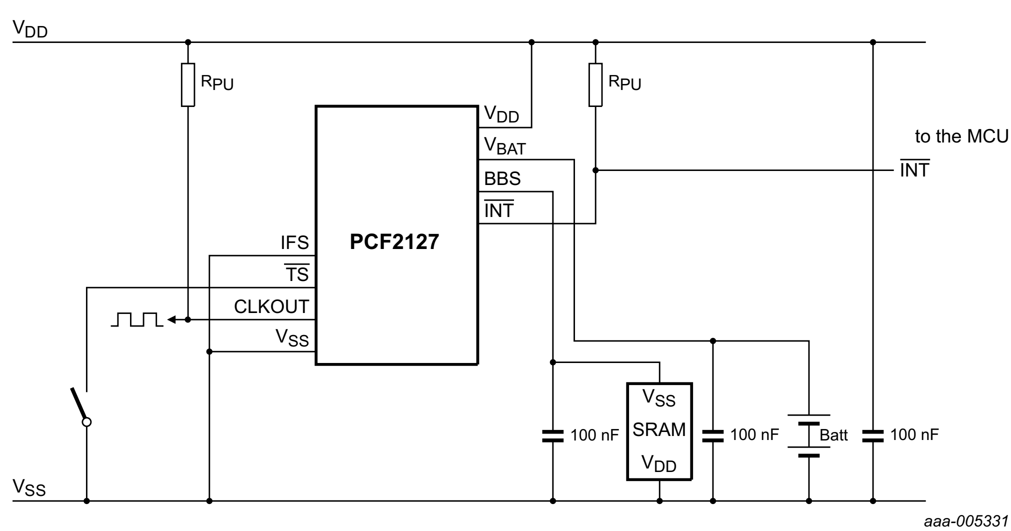


Fig 12. Application diagram: timekeeping, CLKOUT, power management, timestamp, battery connected and supply of an external device

For using the PCF2127 for timekeeping, power management, CLKOUT with a battery connected and supplying a microcontroller, see Figure 13:

- CLKOUT is connected to V_{DD} using a pull-up resistor
- CLKOUT is enabled at 32.768 kHz by default after start-up (COF[2:0] = 000)
- A battery is attached to the V_{BAT} pin
- The battery switch-over and the battery low detection functions are enabled by default (PWRMNG[2:0] = 000)
- The timestamp detection is enabled by default (TSOFF = 0)
- BBS supplies a microcontroller (see Figure 13)

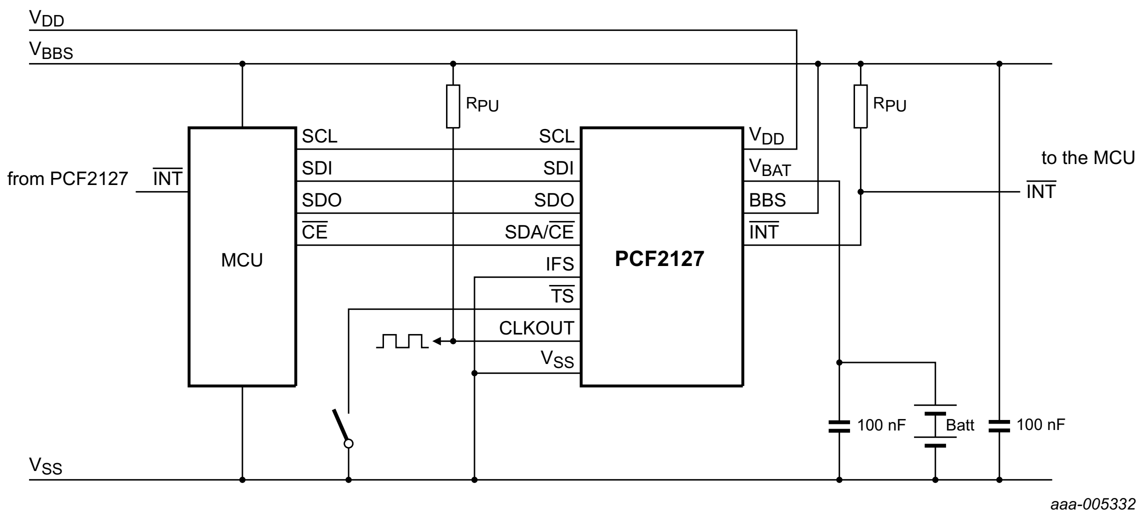


Fig 13. Application diagram: timekeeping, CLKOUT, power management, timestamp, battery connected and supply of a microcontroller

6. Abbreviations

Table 5. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
I^2C	Inter-Integrated Circuit
IC	Integrated Circuit
MCU	Microcontroller Unit
PCB	Printed-Circuit Board
PPM	Parts Per Million
RAM	Random Access Memory
RTC	Real-Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
TCXO	Temperature Compensated Xtal Oscillator
Xtal	crystal

7. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[3] **IPC/JEDEC J-STD-020 —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[4] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[5] **PCF2127 —** Accurate RTC with integrated quartz crystal for industrial applications, Data Sheet

[6] **UM10204 —** I^2C-bus specification and user manual

[7] **UM10301 —** User Manual for NXP Real-Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125

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9. Tables

10. Figures

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