AN11082

PCB design and layout guidelines for CBTL04083A/CBTL04083B

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Document information

Info	Content
Keywords	high-speed signal, PCB, layout, loss, jitter
Abstract	This document provides a practical guideline for PCB design and layout in CBTL04083A/B applications.

Revision history

Rev	Date	Description
v.1	20110722	Application note; initial release

Contact information

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1. Introduction

NXP's CBTL04083A/B (shown in Figure 1) is a 3.3 V, 4 differential channel, 2-to-1 multiplexer/de-multiplexer specially designed for switching the high-speed serial interface signals, up to 8 Gbit/s, such as, PCIe Gen 3, DisplayPort 1.2, USB 3.0, and SATA 6 Gbit/s. CBTL04083A/B offers numerous benefits, such as low insertion loss (–1.3 dB at 4 GHz), low crosstalk (–35 dB at 4 GHz), low return loss (–20 dB at 4 GHz), and the –3 dB bandwidth higher than 8 GHz. The CBTL04083A/B can be used on the motherboard for multiplexing between two PCIe Gen 3, or other high-speed serial interface signals. This document provides the PCB design guidelines and considerations while using CBTL04083A/B.

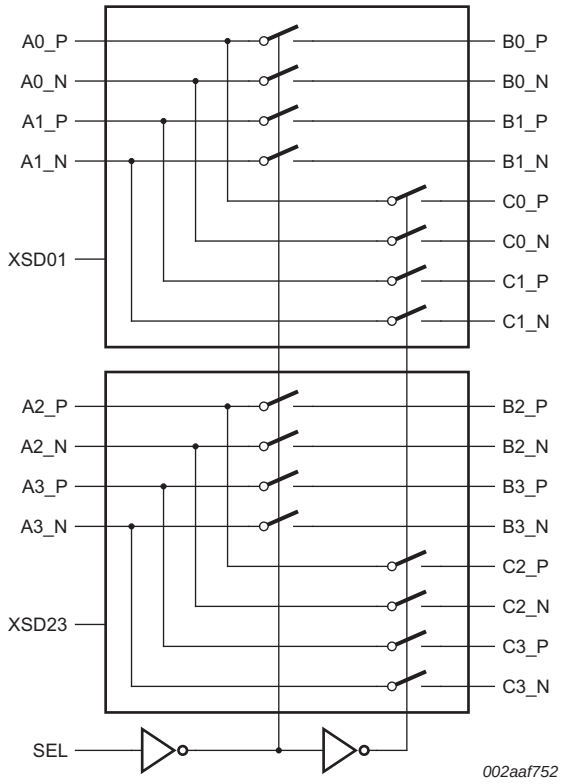

Fig 1. CBTL04083A/CBTL04083B functional block diagram

2. CBTL04083A/B pinouts and motherboard topology

CBTL04083 provides two pinout options for better fitting different motherboard topology. CBTL04083A is the flow-through pin arrangement, and CBTL04083B is a loopback pin arrangement. Figure 2 shows the different CBTL04083 pinouts for different motherboard topology.

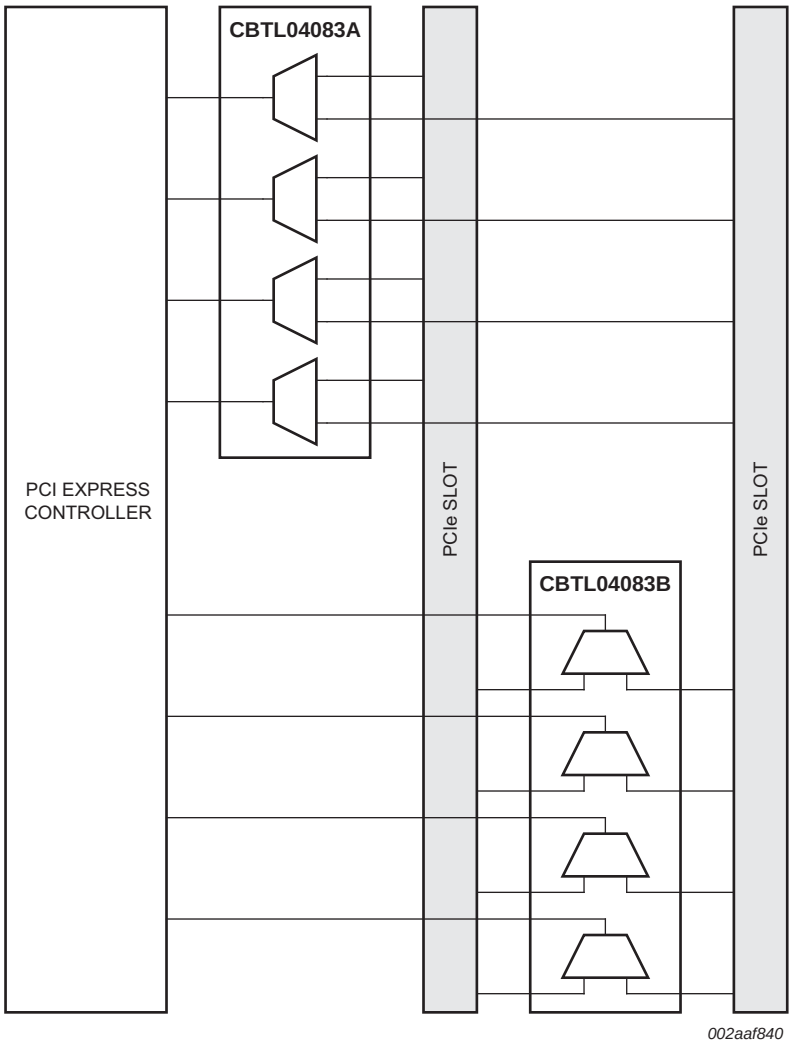

Fig 2. CBTL04083 A-pinout and B-pinout for different topology

3. AC coupling and DC bias

PCIe, DP, USB3, and SATA electrical signals require AC coupling between the transmitter and receiver. The AC coupling capacitors are usually placed close to the transmitter.

CBTL04083A/B requires a bias voltage, less than 2 V, applied to its switches.

The following figures illustrate several AC coupling capacitor placement options.

In Figure 3, the capacitors are placed between the MUX and the downstream controller, and the MUX is biased by the upstream controller.

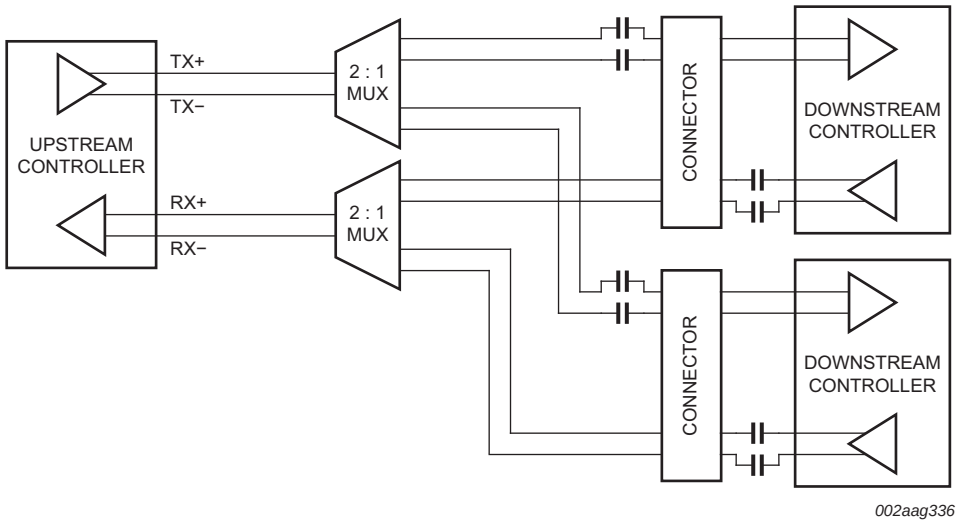

Fig 3. The capacitors are placed between MUX and downstream controller

In Figure 4, the capacitors are placed between the upstream transmitter and the MUX. RX signals on the motherboard sides usually do not require AC coupling capacitors since those capacitors are located on the add-in card. The TX MUX is biased by the downstream controller, and the RX MUX is biased by the upstream controller.

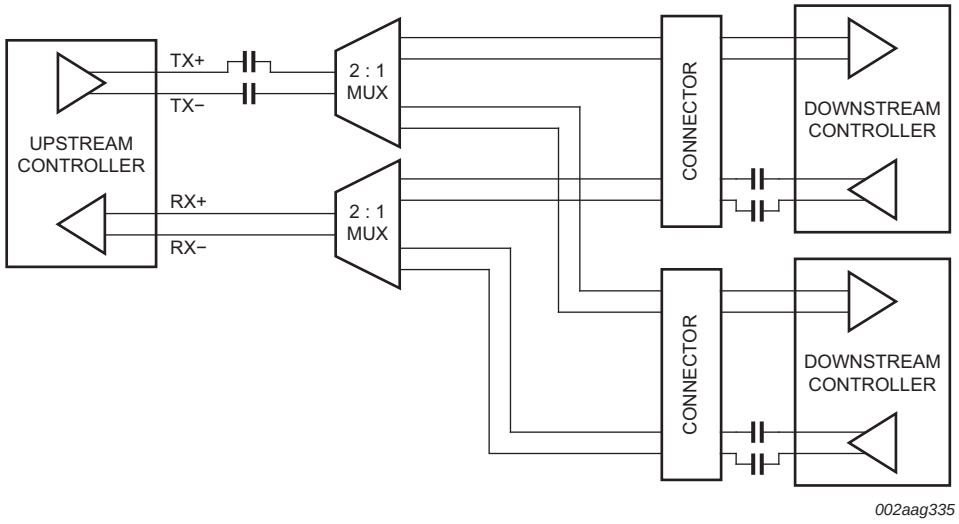

Fig 4. The capacitor is located in between upstream TX and MUX

Remark: Do not place capacitors at both side of MUX, unless a bias voltage is provided.

In case of that both upstream and downstream controllers' common-mode voltage is higher than 2 V, a bias voltage, which is less than 2 V, is needed for CBTL04083A/B. Figure 5 shows an implementation in this case.

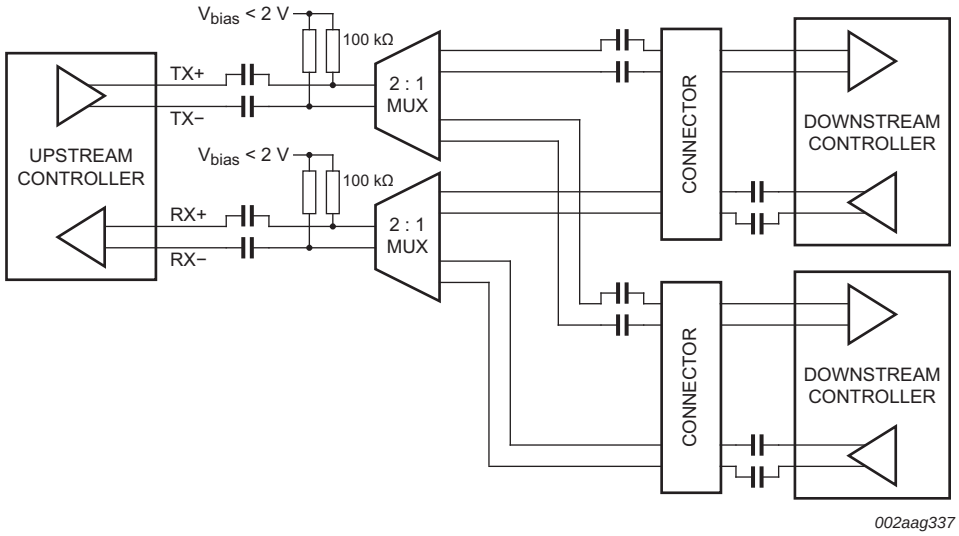

Fig 5. A bias voltage is applied to CBTL04083A/B MUX

4. PCB layout guidelines

4.1 Traces

4.1.1 Impedance

To minimize loss and jitter, the most important considerations are to design the PCB to a target impedance and to keep tolerances small. PCIe, and other high-speed serial link traces need to maintain 100 Ω differential / 50 Ω singled-ended impedance.

4.1.2 Width and spacing

The coupling of the intra-pair differential signals and increased spacing to neighboring signals help to minimize harmful crosstalk impacts and ElectroMagnetic Interference (EMI) effects. The differential trace width and air gap spacing between the two traces of the pair need to be elected to achieve the impedance target.

The spacing between pairs and to all non-PCIe signals should be at least four times the dielectric height. If the non-PCIe signals have significantly higher voltage levels or edge rate than the PCIe signal, the space should increase to ever further in order to avoid cross coupling.

4.1.3 Length and length matching

Trace length greatly affects the loss and jitter budgets of the interconnection. The PCB trace may introduce 1 ps to 5 ps of jitter and 0.7 dB to 0.8 dB of loss per inch (2.54 cm) at PCIe Gen3 speed.

CBTL04083A/B also brings in extra insertion loss to the system. CBTL04083A/B has −1.3 dB loss at 4 GHz, which is equivalent to about 1.5 inch (3.81 cm) to 2 inch (5.08 cm) PCB loss. The system designers need to take this MUX insertion loss into account when planning the system loss budget.

Long distance traces should be routed at an off-angle to the X-Y axis of a PCB layer, in order to distribute the effects of fiberglass bundle weaves and resin-rich areas of the dielectric.

The two traces of a pair should be symmetrically routed, and trace length needs to match. Any asymmetric or mismatch will cause common mode distortion.

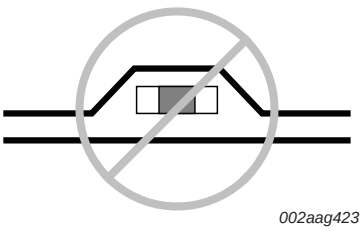

Fig 6. Non-symmetrical routing should be avoided

The length mismatching between a differential pair should be limited to 5 mils (0.127 mm) maximum. Length matching is required per segment, and any length added (typically a 'serpentine' section) for the sake of matching a pair should be added near the location where the mismatch occurs.

The length matching between TX pair and RX pair is not required.

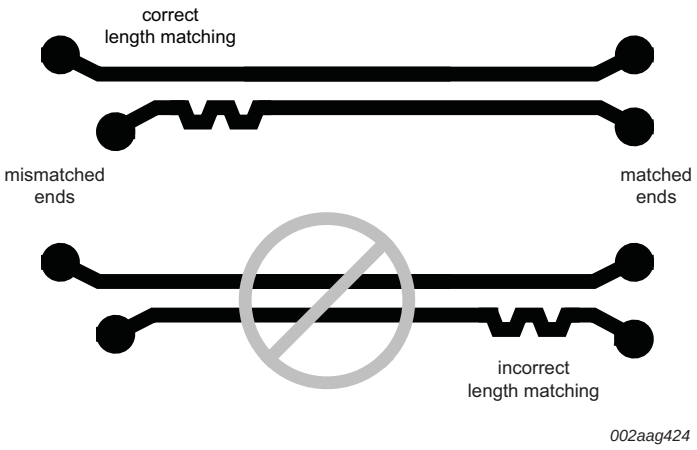

Fig 7. Length matching near location of mismatch

4.2 Test points, vias and pads

Signal vias affect the overall loss and jitter budgets. Each via pair may contribute 0.25 dB of loss in some corner cases. Vias may limit the achievable maximum routing length.

A maximum of two via pairs can be used on a differential pair. Vias should have a pad size of 25 mils (0.635 mm) or less, and a finished hole size of 14 mils (0.356 mm) or less. Two vias must be placed as a symmetric pair in the same location.

Test points and probe pads should be placed symmetrically in series. Stubs should not be introduced on differential pairs. Refer to Figure 8 for illustrations of correct and incorrect placements.

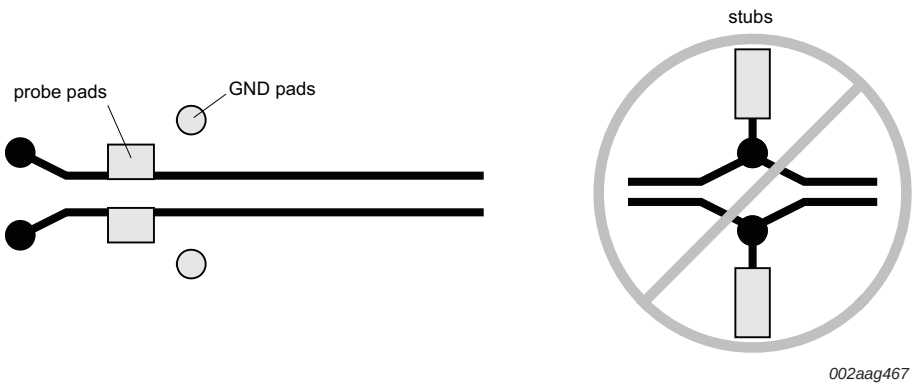

Fig 8. Test points and probe pads

4.3 AC coupling capacitors

PCIe, DP, USB3, and SATA require AC coupling between transmitter and receiver. The AC coupling capacitors for both differential pair signals must be the same value, same package size, and have symmetric placement. If possible, TX traces should route on the top layer.

The 0402 or smaller package size is preferred, and 0603 is acceptable. C-pack is not allowed. The breakout into and out of capacitors should be symmetrical for both signal lines in a differential pair. The trace separation for routing to pads must be minimized in order to optimize tight coupling between the signal pairs.

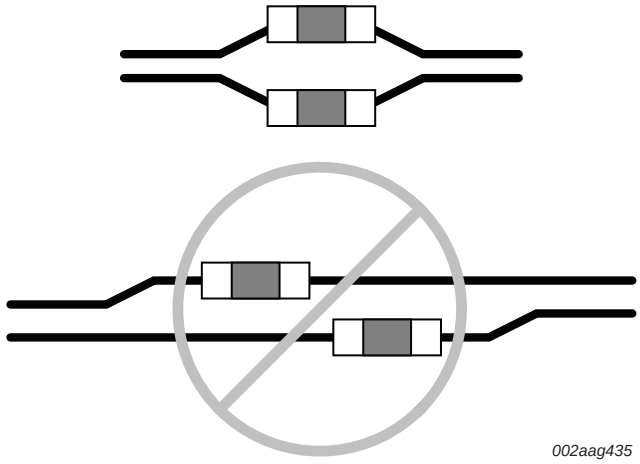

Fig 9. Placement of AC coupling capacitors

4.4 Reference plane

The high-speed differential signals should be referenced to the ground plane. Any discontinuities in the reference plane, such as splits and voids, should be avoided. Never route a trace so that it straddles a plane split.

If it is necessary to change reference to power plane, capacitors with low ESR values should be placed at locations where the PCIe signals are changing layers, and between power and ground planes to minimize the negative impact of EMI and signal integrity performance caused by reference plane changing.

When a signal changes layers, the ground stitching vias should be placed close to the signal vias to provide a current return path. A minimum of 1 to 3 stitching vias per pair of signals is recommended.

Do not route high-speed traces under power connectors, other interface connectors, crystals, oscillators, clock synthesizers, or magnetic devices that use and/or duplicate clocks.

5. Summary

NXP's CBTL04083A/B is a high bandwidth multiplexer/de-multiplexer specially designed for switching the high-speed serial interface signals, up to 8 Gbit/s, such as PCIe Gen 3, DisplayPort 1.2, USB 3.0, and SATA 6 Gbit/s. The high data rate requires some specific implementations in the PCB design. The following is the summary of guideline:

- Maintains 50 Ω ± 15 % single-ended and 100 Ω ± 20 % differential impedance.
- The differential pair must be routed symmetrically. The length mismatching within the differential pair should be less than 5 mils (0.127 mm).
- Do not route high speed signals over any plane split; avoid any discontinuities in the reference plane.
- Avoid any discontinuity for signal integrity. Differential pairs should be routed on the same layer. The number of vias on the differential traces should be minimized. Test points should be placed in series and symmetrically. Stubs should not be introduced on the differential pairs.
- PCB design should account for the insertion loss by the multiplexer, and plan the total trace length accordingly.
- Implement AC coupling capacitors for high-speed link, and provide bias voltage, less than 2 V, to the MUX.

6. Abbreviations

Table 1. Abbreviations

Acronym	Description
DP	DisplayPort
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
MUX	multiplexer
PCB	Printed-Circuit Board
PCIe	PCI Express
PCI	Peripheral Component Interconnect
RX	Receive
SATA	Serial Advanced Technology Attachment
TX	Transmit
USB	Universal Serial Bus

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