AN10872

TL application with UBA2014

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Document information

Info	Content
Keywords	UBA2014, half-bridge, ballast, tube lamp
Abstract	This application note describes the design of an application using the UBA2014 to drive T5 and T8 fluorescent tubes.

Revision history

Rev	Date	Description
v.1	20101209	initial version

Contact information

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1. Introduction

The function of an electronic ballast is to preheat, ignite and control a fluorescent Tube Lamp (TL) and to monitor its condition. If there is no ignition, or the lamp reaches an End Of Life (EOL) condition, the ballast must shut down immediately to avoid damage to the ballast, and/or overheating of the lamp caps.

The application described here is built using a UBA2014 IC, which is a monolithic integrated circuit designed to electronically drive ballasted fluorescent TLs using mains voltages of up to 277 V RMS (nominal value).

The circuit uses a 650 V bipolar CMOS DMOS (BCD) power-logic process. The IC provides a drive function for two discrete power MOSFETs and includes:

- Level-shift circuit
- Oscillator
- Lamp voltage monitor
- Current control
- Timer
- Protection

1.1 Features

- Adjustable preheat time
- Adjustable preheat current
- Current controlled operation
- Single ignition attempt
- Adaptive non-overlap time control
- Integrated high voltage level shift function
- Power-down function
- Protection against damage due to lamp failures or lamp removal
- Capacitive mode protection

2. Scope and structure of document

2.1 Scope

This application note describes the use of a UBA2014 half-bridge driver IC in HF-TL applications. It covers single tube applications only. For support and/or examples of multiple lamp applications please consult your local NXP Semiconductors support office.

The circuits described in this application note are intended to be supplied with a fixed DC voltage provided by a Power Factor Controller (PFC). Alternatively, instead of the DC input, a charge pump, or valley fill topology can be used, but these topologies are not covered in this document.

2.2 Structure of the application note

The information in this application note is set out in discrete sections. Where possible, typical values are given. A block diagram is shown in Figure 1

Section 1 “Introduction”.

Section 2 “Scope and structure of document”.

Section 3 “Pin description” - gives an IC pin overview with a summary and description of the IC pin functions and their typical voltage and current levels.

Section 4 “Series resonant single lamp application circuit” describes the building blocks of a T8 36 W typical application, explains the development steps of the individual sub circuits and gives component values.

Section 5 “Start-up sequence states” - gives preheat, ignition/operating state diagrams of the UBA2014 and shows which IC blocks are active in which state.

Section 6 “EOL detection/protection” - gives an overview of possible additional protection circuits that can be used to avoid damage to the ballast, or the lamp electrodes due to overheating in the case of a degraded lamp.

Section 7 “Debugging a UBA2014 ballast” - gives a sequential procedure for incrementally powering up a ballast, rather than applying full power immediately.

Section 8 “PCB design and layout guidelines” - gives the layout of the PCB to ensure that any ballast will function correctly. Suggestions for placing of components is given together with indication of the current loops that should be kept small.

Section 9 “Inductive mode heating” - shows that Inductive mode heating is achieved by using two small extra windings on the resonant tank coil. Together with a small capacitor in series, these secondary windings are placed across the filament. Values are given for the resonance tank coil and capacitor, secondary inductance and secondary capacitance for TL5/TLD lamps operated in an Inductive mode topology.

2.3 Related documents and tools

Further information and design tools can be found on the NXP Semiconductors internet Product Information Page (PIP) of the UBA2014, or through the local sales office.

3. Pin description

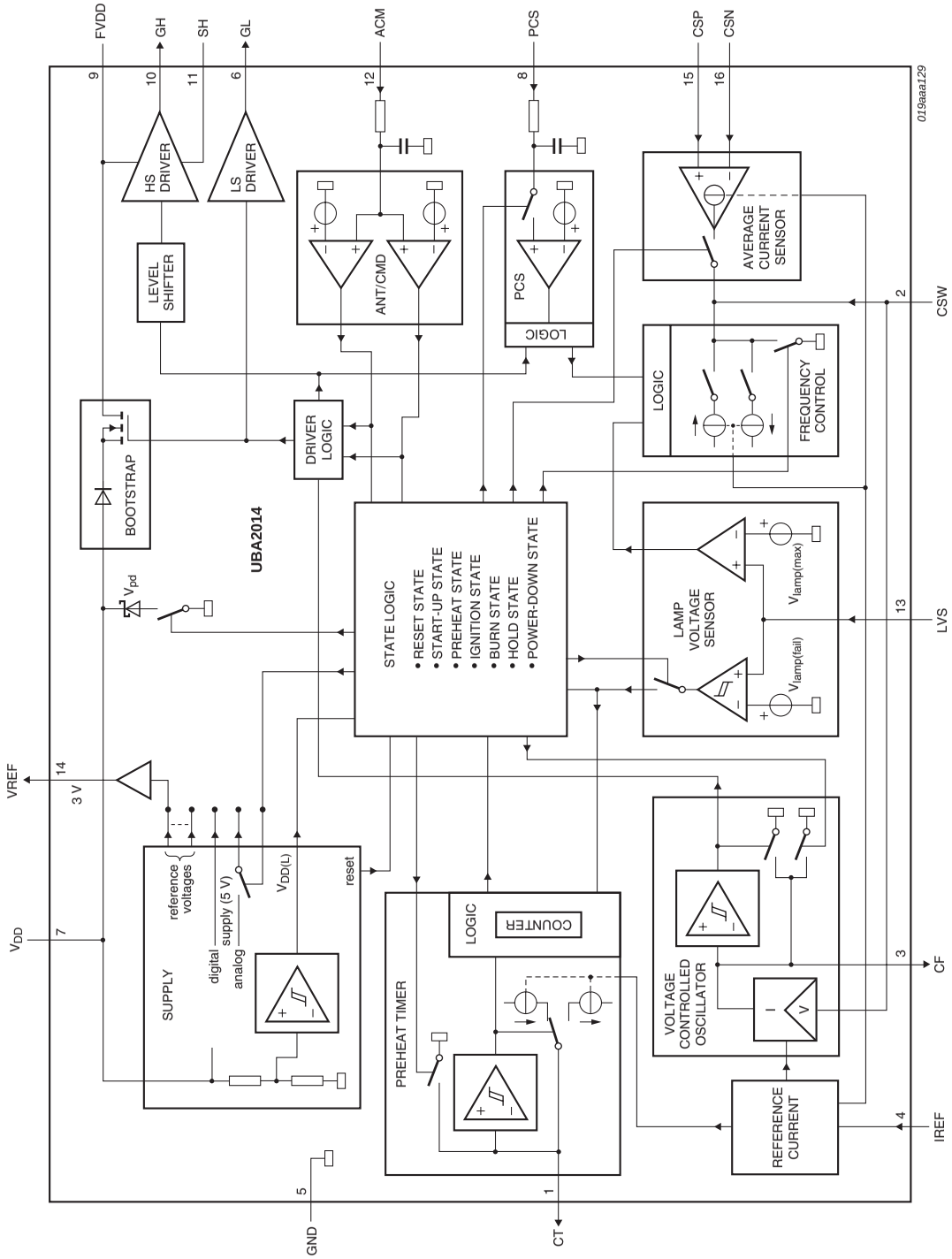


Fig 1. Block diagram

Table 1. UBA 2014 pin functionality

Pin	Name	Function description summary
1	CT	Preheat timer output: A capacitor to ground is connected to the CT pin. The preheat timer (PRT) block determines the preheat and ignition times. The preheat time is determined by a capacitor connected to the CT pin and a resistor (typically 33 kΩ) connected to the IREF pin. The maximum ignition time t_{ign} is one period at CT, and the preheat time t_{ph} is seven periods. The PRT circuit is operational during IC start-up and in the event of a fault condition, is triggered by the Lamp Voltage Sensor via the LVS pin. The preheat time begins when the VCO starts oscillating. The ignition state follows the preheat state as shown in formulas below: $t_{ph} = 1.8 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}}$ $t_{ign} = 0.26 \times \frac{C_{CT}}{330 \times 10^{-9}} \times \frac{R_{IREF}}{33 \times 10^{3}}$
2	CSW	Voltage controlled oscillator output: The capacitor connected to the CSW pin together with the capacitor connected to the CF pin determine the running frequency. If the voltage on the CSW pin is 0 V (start-up condition), the frequency is then at the maximum the controller can produce (which is determined by the CF capacitor value). The capacitor will be charged after start-up, lowering the operating frequency until the correct preheat frequency is reached. After preheat, the capacitor on the CSW pin is again charged until the minimum frequency of the controller is reached. The value of the capacitor on the CSW pin governs the speed of the ramp down from the preheat frequency to the minimum frequency for ignition, which is important for correct ignition. During operation of the lamp, the value of the capacitor on the CSW pin determines the speed with which the frequency changes. The UBA2014 uses the feedback control loop, with the CSP and CSN pins as input for this loop. For full lamp power only, a 220 nF 50 V capacitor connected to ground is normally used. For deep dimming, an RC network can be used to increase the small signal frequency response. If the UBA2014 detects capacitive mode the CSW capacitor is discharged instantly.
3	CF	Oscillator timing capacitor pin: The VCO generates a sawtooth shaped voltage between 0 V and 2.5 V. The frequency is determined by the value of the capacitor connected to the CF pin, the resistor connected to the IREF pin and the voltage at the CSW pin. The maximum frequency (f_{max}), at which the circuit starts oscillating, is 2.5 times the minimum frequency (f_{min}). The driver logic drives the HS and LS drivers at a frequency half of the VCO frequency. A 5 % tolerance, 50 V CP dielectric type capacitor is recommended. A suitable value would be 100 pF which gives a switching frequency f_{min} = 40 kHz, f_{max} = 100 kHz $f_{min} = 40.5 \times 10^{3} \times \frac{100 \times 10^{-12}}{C_{CF}} \times \frac{33 \times 10^{3}}{R_{IREF}}$ $f_{max} = 2.5 \times f_{min}$

Table 1. UBA 2014 pin functionality

Pin	Name	Function description summary
4	IREF	Internal reference current input: Connect with 33 kΩ resistor (1 % tolerance) to ground.
5	GND	Ground
6	GL	Gate output for the low-side switch: The gates of the power MOSFETs are connected to the GH and GL pins. Connect this pin to the gate directly, or via a gate resistor of up to 47 Ω. The level of the GL pin switches between GND and V_{DD}. On the first switching cycle, the drive signal for the LS-driver is extended to enable the bootstrap to charge the externally connected bootstrap capacitor (between pins FVDD and SH).
7	V_{DD}	Low-voltage supply: It is essential that this voltage remains below 14 V at all times. During standby, an internal Zener diode is active; during operation, the design should ensure this voltage is not exceeded.
8	PCS	Preheat current sensor input: This pin is to be connected to a sense resistor in the source of the lower half-bridge MOSFET. At start-up the capacitor connected to the CSW pin is connected to the input of the VCO and will be charged, ensuring a defined frequency sweep which will start at the maximum frequency. By charging the capacitor with a constant current controlled by the PCS, the frequency will decrease until the preheat voltage measured at the PCS pin exceeds an internally fixed voltage of 0.6 V.
9	FVDD	Floating supply voltage: supply for high-side switch
10	GH	Gate output for the high-side switch: The gates of the power MOSFETs are connected to pins GH and GL. Connect this pin to the gate directly, or via a gate resistor of up to 47 Ω. The level of this pin switches between the voltage on pin SH and pin SH voltage plus V_{DD}.
11	SH	Ground (MOSFET source) reference for the high-side switch supply voltage, connect to the half-bridge output.
12	ACM	Capacitive mode detection input: When operating correctly, the voltage at pin ACM consists of a positive pulse with a minimal amplitude of 100 mV during the rising slope of the half-bridge, and a pulse below −85 mV during the falling edge of the half-bridge. It is typically measured across an externally connected resistor in the V_{DD} generation circuit. These pulses input to the Adaptive Non-overlap Timer (ANT) block, which ensures that both power MOSFETs have the same on-time, independent of the frequency. The same signal is used to avoid hard switching (adaptive non-overlap) and to detect Capacitive mode (see Figure 1 “Block diagram”).

Table 1. UBA 2014 pin functionality

Pin	Name	Function description summary
13	LVS	Lamp voltage sensor input: Used to monitor lamp behavior and trigger protections if required. The lamp voltage must be monitored to ensure that if the lamp does not ignite, or the lamp fails during operation, the ballast will not subsequently be damaged. Two voltage levels are defined: $V_{lamp(fail)}$ (0.8 V) and $V_{lamp(max)}$, (1.5 V) measured at pin LVS. The ignition level of a properly functioning lamp should be between these two levels. Passing the $V_{lamp(fail)}$ level starts the ignition timer (re-using the CT timer). If the lamp ignites, the lamp voltage will drop and the voltage measured at the LVS pin will also drop. If the lamp does not ignite, the UBA2014 in its ignition state, will limit the frequency ramp down, so that $V_{lamp(max)}$ is not exceeded, and will hold this level for the maximum time allowed by the ignition timer. If the lamp has not ignited at the end of the ignition timing, the UBA2014 will switch to standby, and will stay in this state until a power cycle is done. During lamp operation, the LVS pin protects the ballast against worn or defective lamps. As soon as $V_{lamp(fail)}$ is exceeded (e.g. worn lamp), the UBA2014 goes to standby after a time-out period of one CT cycle. If during operation $V_{lamp(max)}$ is exceeded (e.g. broken filaments), the UBA2014 will immediately go to its initial state and restart.
14	VREF	Reference voltage output (2.95 V): Can be used to set the desired lamp current level on the CSP pin, and for lamp End Of Life (EOL) detection.
15	CSP	Positive input error amplifier and average current sensor: This is the desired lamp current level. It can come from a microprocessor with a Dali interface, or from a galvanic separated 0 V to 10 V interface, or from a potentiometer. If no dimming is required, it can be a fixed voltage derived from V_{ref}.
16	CSN	Negative input error amplifier and average current sensor: The average lamp current measurement is usually achieved by developing a voltage across a resistor and applying this to the CSN pin. The output voltage of the ACS block is fed to the VCO regulating the switching frequency and, as a result, the lamp current. If CSP is higher than CSN the ACS circuit will lower the frequency in order to increase the lamp current until the level set by CSP. If CSP is lower than CSN, the ACS circuit will increase the frequency in order to reduce the lamp current. During lamp operation, the capacitor on the CSW pin determines the speed with which the frequency is changed by the feedback control loop.

4. Series resonant single lamp application circuit

When the resonant tank inductor is used, the lamp electrodes and a capacitor in series give the easiest and most economical application. This is commonly known as the series resonant topology. Figure 2 gives the series resonant configuration using a TL8 36 W lamp as an example.

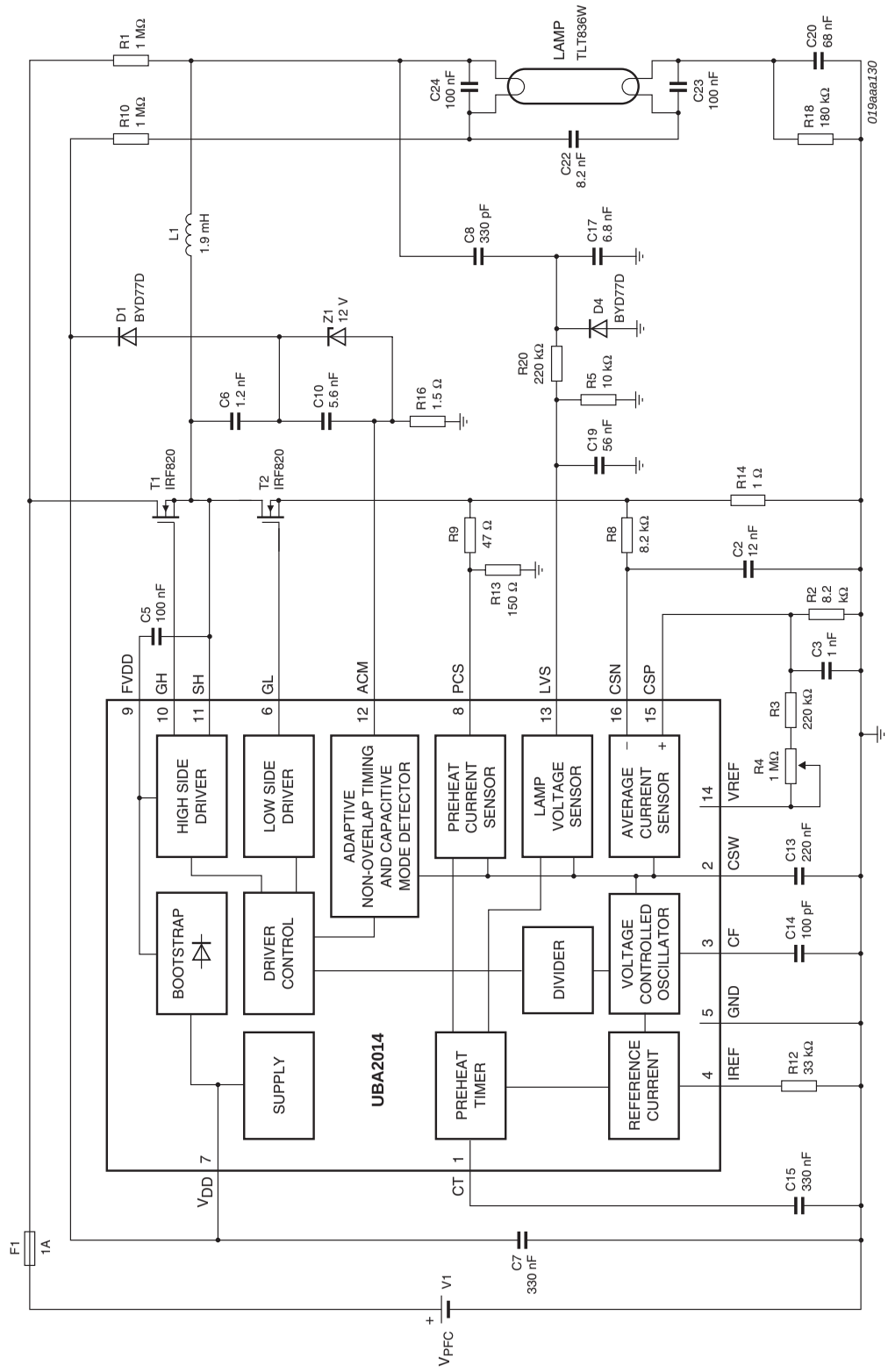


Fig 2. Application diagram: series resonant topology

4.1 Resonant tank

Coil L1 and capacitor C22 form the resonant tank. The combination of these two components generates the ignition voltage, and will ensure correct operation and preheat current for the lamp. The two power MOSFETs T1, T2 driven by the UBA2014 generate the square wave that drives the resonant tank.

The performance of the MOSFETs plus the resonant tank, should be such that at minimum frequency, the UBA2014 can generate (f_{min}), and output approximately 10 % more than the required operating power for the lamp. This allows the feedback control system enough margin to ensure proper operation. The coil should not saturate at the maximum ignition voltage allowed by the overvoltage protection circuit. The choice of capacitor C22 should be one with low dielectric losses at 50 kHz.

Capacitor C20 is used for DC blocking. Its value should be such that there is minimum possible ripple voltage. A capacitor of 68 nF is suitable for most ballasts. Resistor R18 is used to avoid striation.

4.2 Over voltage/no ignition protection sub circuit

The small signal voltage input to the LVS at pin 13 is derived from the voltage on the lamp connector via a voltage reduction divider circuit comprising C8, C17, R20, R5 and D4.

4.3 Feedback control loop for lamp power sub circuit

The voltage across resistor R14 due to the lamp current is applied to the CSN pin. The input to the CSP pin is obtained from the reference voltage of 2.95 V via the dimming combination of potentiometer R4 and resistor R3.

Resistor R8 and capacitor C2 filter any HF noise from the CSN pin input. Resistors R8 and R2 have the same value to cancel out bias current offset in the error amplifier.

4.4 V_{DD} supply sub circuit

The V_{DD} supply uses components Z1, D1, C6, C10 during lamp operation. During start-up, the resistors R1, R10 raise V_{DD} until V_{start} (if a tube is inserted). In this way, the ballast will restart itself after the tube is replaced.

Adaptive non-overlap and Capacitive mode are controlled via resistor R16.

4.5 UBA2014 ballast controller configuration components

Timing capacitors C13, C14, C15 and reference resistor R12 (at pins 2, 3, 1 and 4 respectively) are required for correct circuit operation (see Table 1 for functional details).

4.6 Resonant tank values for series resonant (TL5/TL8 lamps)

Figure 3 is a simplified circuit set-up for the lamp, showing the resonant capacitor, resistor and inductor. A set of suggested values for the most commonly used TL5 and TL8 lamp families is given in Table 2.

Figure 4 shows a simplified circuit set-up for the lamp with inclusion of a PTC thermistor. Table 3 gives a set of suggested values.

For some burners it is not possible to find a capacitor value whereby the voltage at the burner is not too high during preheat, where there is sufficient preheat current, and not too much current through the filament during lamp operation. For these burners a circuit with a PTC as in Figure 4 can be used.

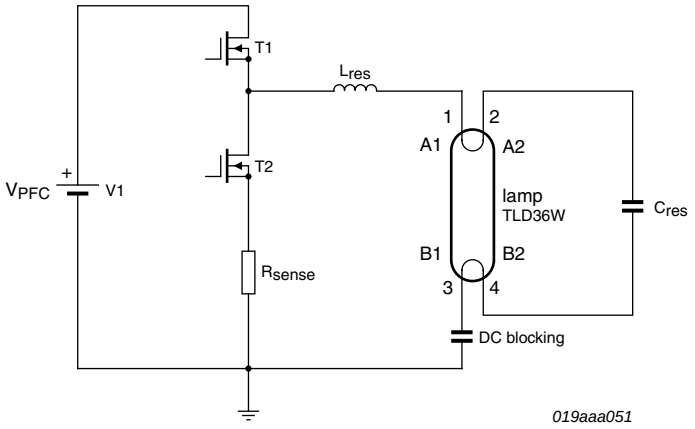


Fig 3. Simplified TL lamp series resonant circuit

Table 2. Suggested resonant tank values for different lamp types[1]

Lamp	L_{res} (mH)	C_{res} (nF)	$f_{preheat}$ (kHz)	R_{sense} (Ω)	V_{bus} (V)	Preheat current (RMS) (mA)	V_{lamp} during preheat (V)	Preheat time - t_{ph} (s)
TLD 36 W	1.9	8.2	70	1	400	600	230	1.7
TLD 58 W	1.4	10	60	0.82	400	700	170	1.7
TL5 HE 14 W	3.9	5.6	54	3.3	400	225	180	1.5
TL5 HE 21 W	3.7	5.6	54	3.3	400	225	180	1.5
TL5 HE 21 W	4.0	3.9	58	3.3	400	225	230	1.5
TL5 HE 35 W	4.0	3.9	58	3.3	400	225	230	1.5
TL5 HO 39 W	2.0	10	52	1	400	560	240	1.5
TL5 HO 49 W	2.6	6.8	52	2.2	400	370	240	1.5
TL5 HO 54 W	1.5	10	55	0.75	400	800	330	1.5

[1] Frequency for nominal power = 42 kHz.

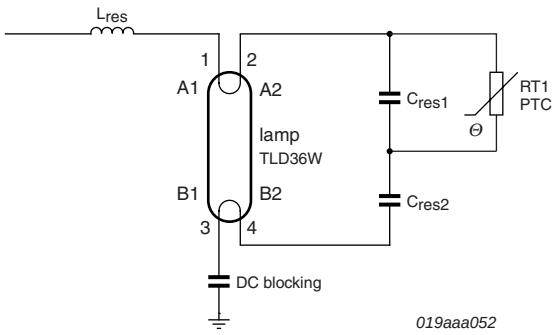


Fig 4. TL lamp series resonant circuit with PTC thermistor

Table 3. Suggested values for resonant tank for different lamp types

Lamp	L_{res} (mH)	C_{res1} (nF)	C_{res2} (nF)	R_{sense} (Ω)	V_{bus} (V)	Preheat current (RMS) (mA)	V_{lamp} during preheat (V)	PTC type	Preheat time - t_{ph} (s)
TLD 18 W	2.3	22	15	1.2	400	530	180	150E	1.7
TLD 32 W	2.2	22	12	0.82	400	610	280	150E	1.7

4.7 Preheat circuit

The preheat current through the electrodes and the lamp capacitor is controlled by the preheat current sensor circuit (PCS, pin 8 of the controller, see also Figure 2), and is determined by the values of resistors R14, R13 and R9. The controller generates a preheat frequency so the voltage on pin 8 reaches 0.6 V peak at the end of the lower gate drive MOSFET ‘on time’.

The RMS value of a sine wave shape current, is the peak divided by √2 for a triangle √3. In most cases, as short as possible a preheat time is chosen so that the current will be close to a sine wave. In the example of Figure 2 the peak current is 0.788 A giving an RMS preheat current of 0.56 A.

4.8 Feedback loop control

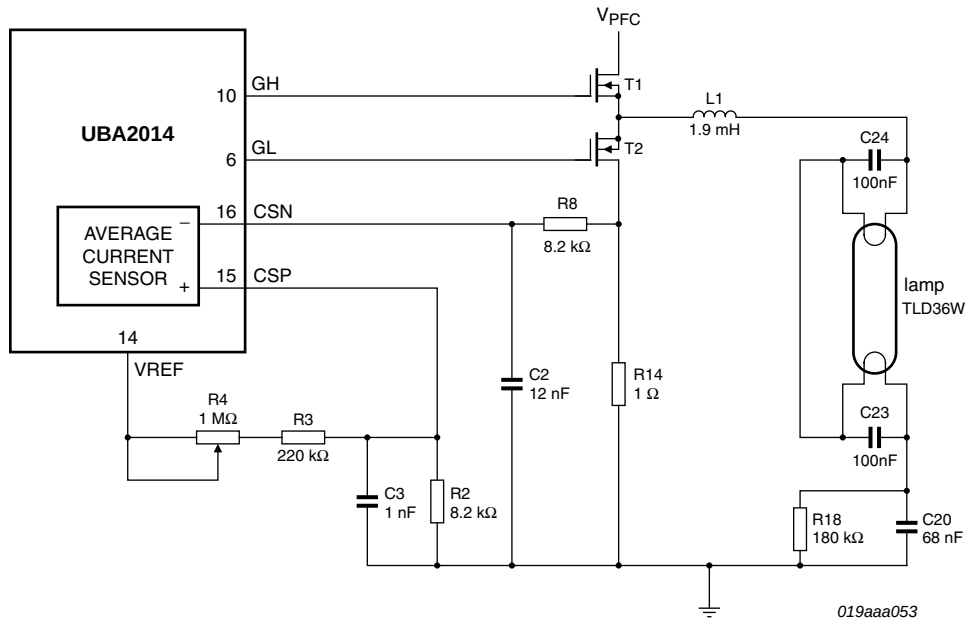


Fig 5. LC tank with signals CSN and CSP

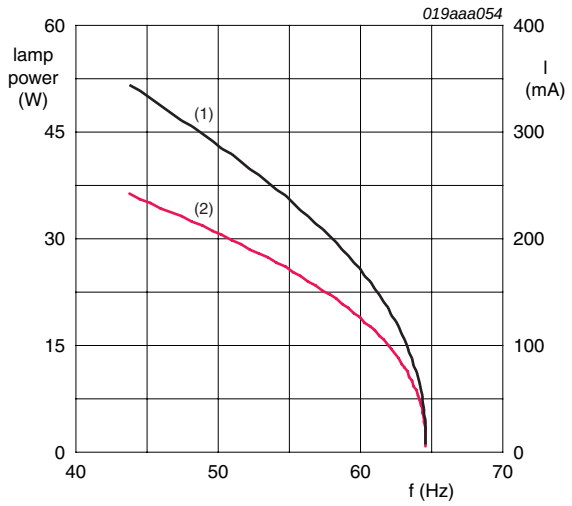
The lamp power can be controlled by the ballast frequency. The feedback control loop inside the UBA2014 adjusts the frequency so that the voltage at the CSN pin is equal to the voltage on the CSP pin. The UBA2014 control loop regulates the current, so there is a linear relationship between the voltage on pin CSP and the lamp current.

Resistor R8 (recommended value 8.2 kΩ), and capacitor C2 (recommended value 12 nF) form a low pass filter which results in a DC voltage for the CSN pin. The circuit can use either a potentiometer or fixed resistors for dimming. V_{ref} is divided to provide the voltage for CSP that matches the voltage on R_{sense} at the desired dimming level. The nominal voltage on pin CSN is equal to the lamp current times R_{sense}, therefore, for full operational lamp power, the voltage at the CSP pin must be equal to this voltage.

Care must be taken to ensure that there is some allowance for component tolerance on f_{min}, so the nominal operating frequency should be about 3 kHz to 5 kHz above f_{min}.

The frequency at which the lowest dimming level is reached, should be lower than f_{max}. If it is not, the L and C values must be changed. The values in the Table 2 and Table 3 will ensure dimming down to 10 %.

Taking the L, C and V_{bus} (DC) values from the T8 36 W lamp example of Figure 2 (L = 1.9 mH, C = 8.2 nF, V_{bus} (DC) = 400 V respectively), a power versus frequency graph can be calculated as shown in Figure 6. 10 % dimming is reached below f_{max} and operating power is reached just above f_{min}.



(1) Power.

(2) Current.

Fig 6. Power and current as functions of frequency (series resonant)

4.9 V_{DD} supply and Capacitive mode protection

4.9.1 IC voltage supply (see Figure 7)

Before start-up, the V_{DD} supply capacitor C7, is charged via the start-up resistors, R1, R10 (Figure 2) up to the DC bus voltage. The IC circuit action begins when the supply voltage exceeds $V_{DD(start)}$. The half-bridge starts to switch, and the IC is supplied via the dV/dt capacitor C6, connected to the half-bridge. The value of this capacitor is determined by the MOSFETs used. To drive larger MOSFETs, the IC will require a greater supply current, which in turn requires a larger dV/dt capacitor. However, if the dV/dt capacitor is too large, the half-bridge may be hard-switching at the higher frequencies. This capacitor also helps to reduce the reactive current flow through the bulk diode of the MOSFET into the buffer capacitor, and then back via the R_{on} of the MOSFET. In most use cases, a capacitor of between 1 nF and 1.5 nF is a good compromise. Fine tuning is done by simulation or experimentation.

As there can be an initial high voltage overload of the start-up resistors, if Surface Mounted Devices (SMD) are used, the voltage should be reduced by a factor of 2 or 3. The maximum permissible voltage overload of a typical 0805 size SMD resistor is 200 V.

The current through the dV/dt capacitor C6, is fed to the V_{DD} supply capacitor via diode D1. This device should have a fast recovery time. A suitable type would be the 1N4148 or BYD77D. The voltage is clamped by a 0.5 W Zener diode, Z1.

Typically during ignition, more power will be pulled from the V_{DD} supply capacitor C7, than is put in, so when MOSFETs with a relative large gate capacitance are used, the value of this capacitor must be increased. A typical value of 330 nF 25 V is generally sufficient.

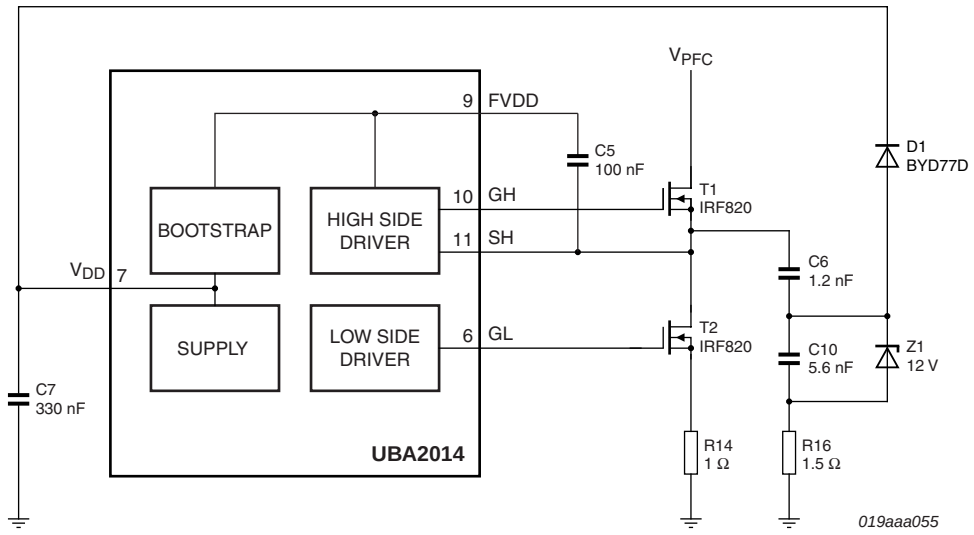


Fig 7. IC supply circuit

4.9.2 Capacitive mode

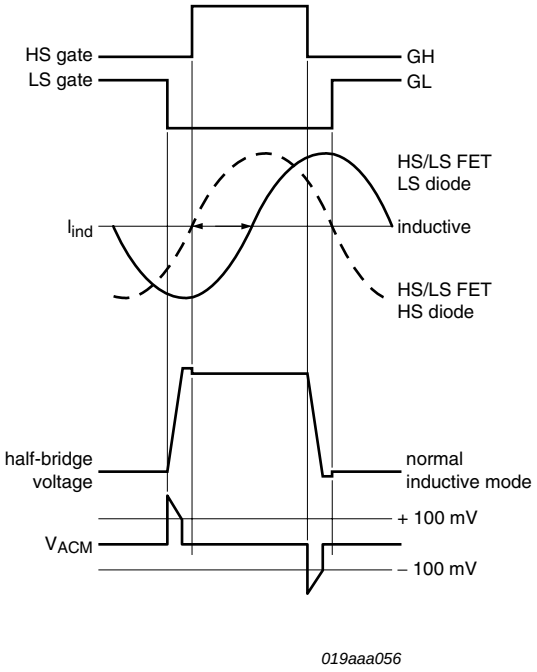
If the load (resonant tank plus lamp), monitored by the half-bridge (voltage and frequency), is sensed to be capacitive, the body diode of one of the MOSFETs is conducting current at the moment the other MOSFET is switched on (see Figure 8d).

Capacitive mode operation of the resonant tank will cause damage to the ballast. Capacitive mode (even with a well designed ballast) can occur when the input voltage is too low (failure of the PFC circuit or the direct rectified mains), or because of a lamp failure. The UBA2014 is designed to detect Capacitive mode and prevent damage caused as a result.

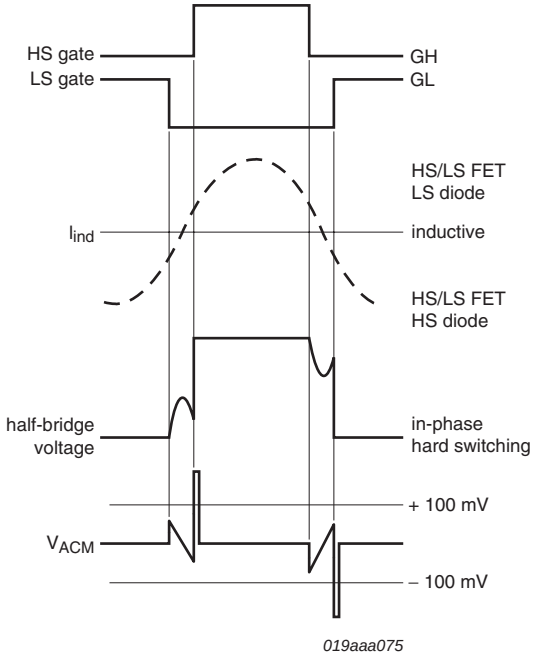
The Capacitive mode detection with the UBA2014 is as follows:

- After the preheat phase, the signal R_{ACM} across resistor R16 (Figure 2), (input at pin ACM) gives information about the switching behavior of the half-bridge.
- Capacitive mode (see Figure 8) is only detected in the ignition or burn states (not during preheat), when one of the following error situations occur:
  - The voltage on the ACM pin does not exceed the +100 mV at any time during the non-overlap between LS off and HS on,
  - The voltage on the ACM pin does not go below −100 mV during the non-overlap time between HS off and LS on,
- The frequency will immediately increase to the maximum, bringing back the Inductive mode condition, and thereby avoiding component damage in the application.

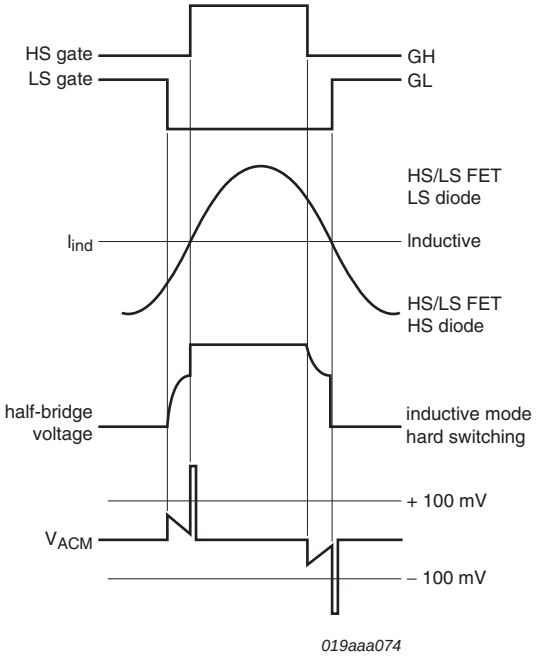
Figure 8 shows the possible operating modes of the half-bridge.



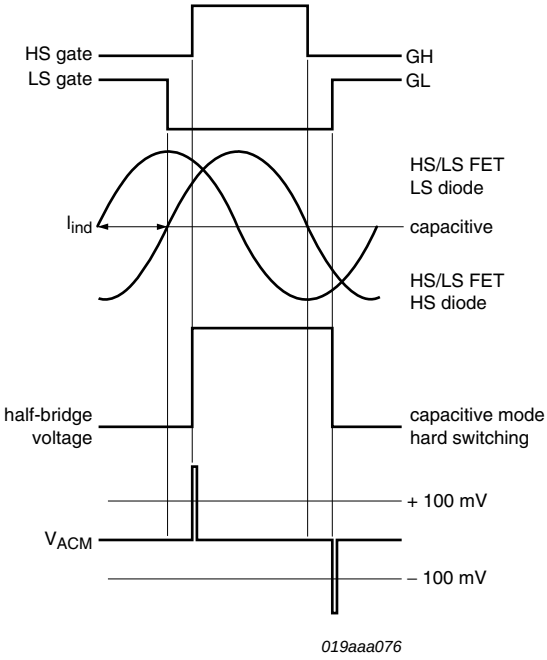
a. Normal/good - Inductive mode



b. Inductive mode - hard switching



c. Indeterminate/interim situation



d. Capacitive mode

Fig 8. Half-bridge modes of operation

The gate drive signals are GL (pin 6) and GH (pin 10). The half-bridge voltage VR_{pre} is the voltage at the intersection of the two MOSFETs is the ACM input, across sense resistor R16 (see Figure 2 “Application diagram: series resonant topology”).

The normal/good Inductive mode of operation is shown In Figure 8a. The adaptive non-overlap timing of this IC will switch on the power MOSFETs when V R_{ACM} returns to zero. This is a unique feature of this IC. Other controllers have a fixed non self adaptive dead time. With the adaptive non overlap, the MOSFETs are switched on at the optimal time to reduce the current through the body diode to a minimum.

In Figure 8b the circuit is still in Inductive mode, but with very small coil energy during non-overlap, making it impossible to pull the half-bridge point from ground level to the DC-supply rail or back. This causes hard-switching.

The situation shown in Figure 8c cannot occur due to the adaptive non-overlap timing. The moment of switching is determined by either the crossing of the positive pulse at the ACM pin through zero, or at the end of the minimum non-overlap time, when the minimum non-overlap time has not yet been reached.

Figure 8d shows the Capacitive mode. A voltage pulse at V R_{ACM} is present during the low to high and high to low transition, but only after the gate drive has become active, not during the dead time.

The typical value of R_{ACM} is 1.5 W. In designs with a high bus voltage (multiple lamp in series may run at voltages of > 500 V), and MOSFETs with a high gate drive capacitance (requiring a higher charge pump capacitor value for V_{DD} generation), the value of R_{ACM} should be reduced, to avoid exceeding the IC's maximum rating during the ballast start-up.

4.10 Choosing values for the UBA2014 timing components

4.10.1 Preheat (Pin 1)

The preheat time has to be selected to meet the requirements of the lamp. Typical times are 1.5 s to 1.7 s for a series resonant topology as shown in Figure 3 and 1 s to 1.2 s for the inductive heating topology as described in Section 9.

The value for the capacitor C15 between pin 1 (CT) and ground can be calculated by the formula in the data sheet and the pin description, see Table 1.

4.10.2 CSW (Pin 2)

The value of the CSW capacitor C13 has to be chosen to meet conflicting requirements. It must be large enough for the resonant tank to build up the ignition voltage and the stability of the control loop. It must also be a small enough value to avoid visible fluctuations in the lamp current.

A value of 220 nF will be adequate for most applications. For deep dimming applications an RC network can be used instead of a single capacitor (see an example drawing in Section 9), to increase the small signal loop response time. It is advised to keep V_{CSW} 10 % below 2.7 V in order to have the loop regulating at nominal lamp power.

4.10.3 CF (Pin 3)

Capacitor C14 determines CF f_{min} and f_{max}. The typical value of 100 pF will give an f_{min} of 40 kHz and an f_{max} of 100 kHz.

4.10.4 IREF (Pin 4)

The value of resistor R12 (IREF) must be 33 kΩ. This value is critical to internal voltages/currents and must not be changed.

5. Start-up sequence states

The sequence for correct ballast operation as shown in Figure 9 is:

1. Preheat
2. Ignition
3. Operation

The UBA2014 has a built in state machine to match this.

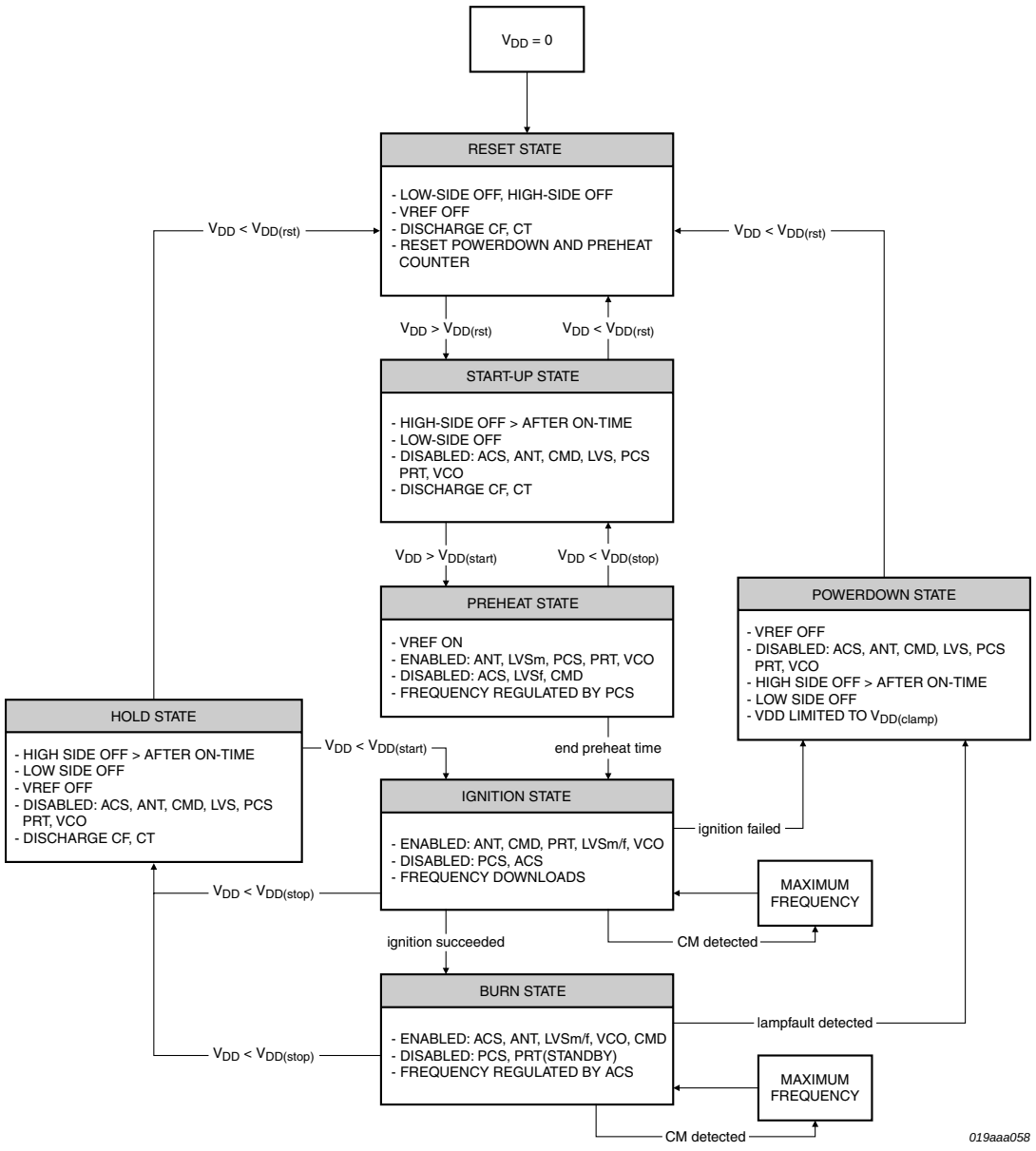


Fig 9. UBA2014 flowchart

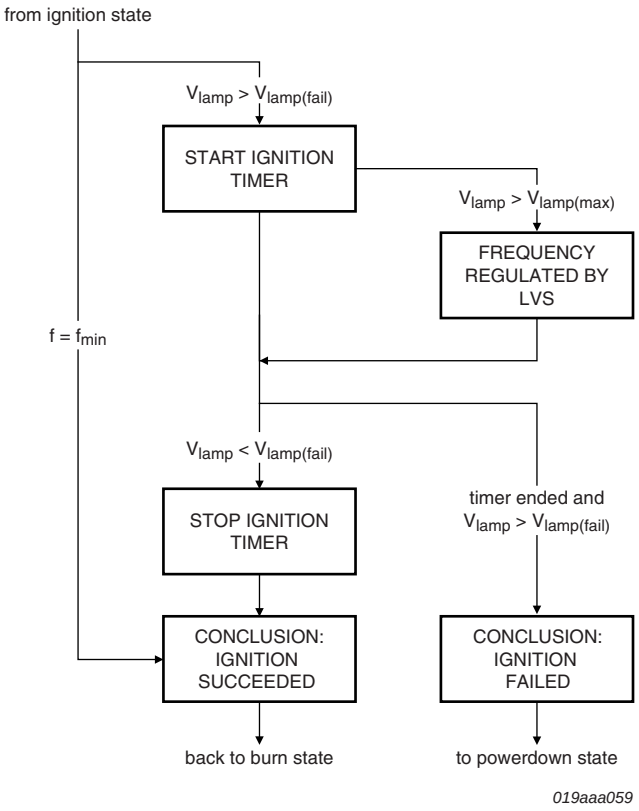


Fig 10. Ignition detection (LVS, ignition state)

5.1 Reset state

After a negative DC voltage is applied to the rail, capacitor C7 (C_{VDD}) connected to the V_{DD} pin is charged through start-up resistors R_{start} (R1 in Figure 2) and R_{VDD} (R10 in Figure 2). With the configuration as shown in Figure 2, this will only occur if a lamp (cathode) is present. First the digital supply is initially established. If the voltage at the V_{DD} pin is below the reset level ($V_{DD(rst)}$), the logic, the power-down and the preheat counter are reset. In the rest and start-up of the circuit both half-bridge MOSFETs are non-conductive.

If the UBA2014 is suddenly stopped due to tube arcing detection, the V_{DD} can be pulled down via a resistor of 100 Ω to allow the state machine time to shut down safely without causing cross conduction.

5.2 Start-up state

The voltages of capacitors C15 (CT, pin 1) and C13 (CF, pin 3) are kept at zero during the start-up state. Capacitor C13 (CSW, pin 2), which is the input of the voltage controlled oscillator, is actively discharged, ensuring a defined start of the frequency sweep at the maximum frequency.

In the start-up state, the reset has ended and the IC is ready to start. If the low voltage supply at the V_{DD} pin rises further and reaches the value of $V_{DD(start)}$, the internal analog supply is activated and the circuit will begin to oscillate.

5.3 Preheat state

Oscillation starts with a long first stroke of approximately 50 μs on the lower half-bridge MOSFET to ensure that the bootstrap capacitor is fully charged.

The preheat time begins at the moment the circuit starts oscillating. Capacitor C13 (CSW) is charged from a constant source-current controlled by the preheat current sense block, thereby decreasing the frequency until the preheat voltage level at the PCS pin is exceeded.

The preheat current sensor then starts to discharge capacitor C13 (CSW) with an average current that is equal to the opposite of the charge current, thus raising the frequency with the same sweep rate. The preheat is therefore regulated around a predefined level until the end of the preheat time. During this time, the average current sensor circuit is disabled.

There is an internal filter of 30 ns at the PCS pin to improve immunity from hard switching noise or from ringing by parasitic inductances.

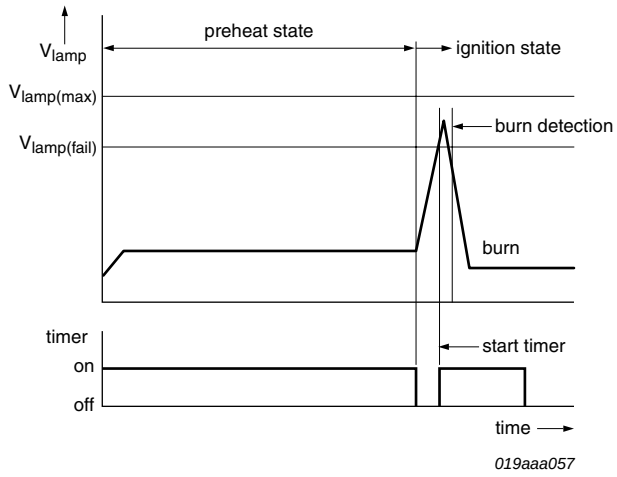
5.4 Ignition state

After the preheat time, the ignition state is entered and the frequency sweeps further down, due to charging of the capacitor at the CSW pin with an internally fixed current. During this continuously decreasing frequency, the circuit approaches the resonance frequency of the load. This will cause a high voltage across the lamp, which will then normally ignite.

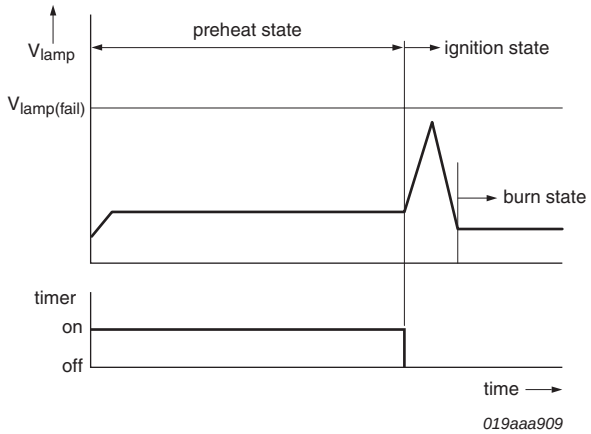
The ignition voltage of a lamp is normally above the $V_{lamp(fail)}$ level. If the lamp voltage passes the $V_{lamp(fail)}$ level the ignition timer is started (see Figure 11a). The lamp can also ignite without exceeding the $V_{lamp(fail)}$ level (see Figure 11b)

Lamp ignition is detected by the lamp voltage sensor (LVS). When a lamp ignites, the voltage normally drops from a value at ignition, to a much lower burn level, and so the voltage at the LVS pin drops below the $V_{lamp(fail)}$ level again. The circuit will enter the burn state.

This decision process is graphically represented in Figure 9. If the lamp ignites after preheat, and before the $V_{lamp(fail)}$ level is reached, the voltage at the CS pin will continue to increase until the minimum frequency is reached. The logic will now assume that the lamp has ignited, and the circuit will enter the burn state. This can result in a small light flash.



a. failure mode during ignition



b. normal ignition

Fig 11. Ignition states

5.5 Burn state

During the Burn state the Average Current Sensor (ACS) is enabled. The load current, which reached a maximum during ignition, will decrease, and therefore so will the averaged voltage across R_{sense}. As soon as this voltage, measured at the input CSN pin, reaches the reference level at CSP pin, the control loop is closed, and the average current sensor will take over the control of the load current. By comparing both inputs, the ACS controls/changes the frequency of the oscillator and thereby the half-bridge.

The averaged voltage across R_{sense} is a measure of the power dissipated in the system. If we assume negligible power losses in the switches and the lamp coil, the power dissipated in the lamp can therefore be controlled by regulating the average current through R_{sense}. This current can be varied by changing the half-bridge frequency, thereby changing the operating point on the LC curve and so the load current/lamp power. Dimming is possible by decreasing the reference voltage on the CSP pin of the ACS.

During the ramp down in frequency for ignition, the state machine shown in Figure 10 is active to avoid lamp over voltage.

The lamp voltage is monitored during lamp operation, and the UBA2014 will be switched to standby if the lamp fails (see Figure 12).

In Figure 2 an example LVS circuit can be seen. C6 and C7 first divide the voltage down by a factor of 20, after which the voltage is divided again by low pass filter R20, R5 and C19. The values of the filter components are chosen so that a voltage of 1.5 V is present at pin LVS at the maximum ignition voltage of the burner.

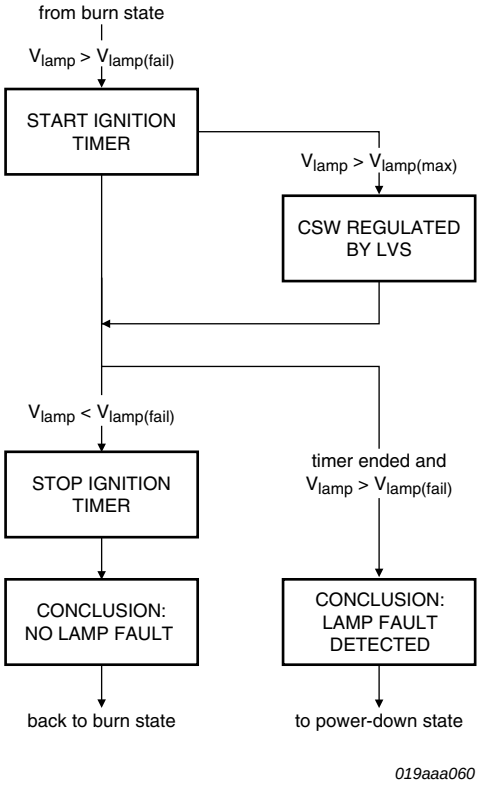


Fig 12. Lamp fault detection (LVS, burn state)

5.6 Power down state

The power-down state is entered if the lamp voltage becomes too high for too long a time period (one CT timer tick) during the ignition state or burn state. When the lamp fails to ignite or its voltage becomes too high during lamp operation (symmetrical aging) the UBA2014 stays in the power-down state until a power cycle has taken place.

6. EOL detection/protection

6.1 IEC requirements

When a lamp reaches its EOL, a tube can show electrical characteristics that can cause overheating of the filament and/or damage to the ballast. Ref. 1 requires the proper operation of the ballast under the following conditions.

1. The lamp, or one of the lamps, is not inserted.
2. The lamp does not start because one of the electrodes is broken.
3. The lamp does not start, although the electrode circuits are intact (de-activated lamp).
4. The lamp operates, but one of the electrodes is de-activated or broken (rectifying effect).
5. A short circuit of the starter switch, if present (not applicable for an HF ballast).

List item 1, List item 2 and List item 3 are already covered by the standard application schematic (Figure 2). The rectifying effect (List item 4) can best be understood by reference to the EOL lamp replacement schematic, Figure 13.

List item 5 is not applicable.

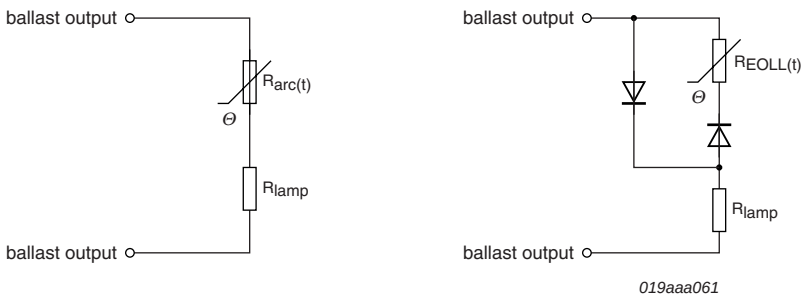


Fig 13. EOL lamp replacement circuit for arcing and rectification

For simulating the end of lamp life effects, Ref. 1 describes three tests:

- Asymmetric pulse test
- Asymmetric power dissipation test
- Open filament test.

6.2 Bringing the UBA2014 into power-down

The UBA2014 can be brought into standby state by putting a 0.8 V pulse for one CT timer tick (about 150 ms depending on the preheat time) on its LVS input pin. The LVS pin detects and protects against “no ignition” failure, and additionally EOL detection is added.

The UBA2014 can also be stopped instantly by pulling V_{DD} to ground. Use a resistor of about 100 Ω so the IC is not allowed to finish the shutdown procedure via the hold state as described in the flowchart (Figure 9).

This immediate power down without timeout can be used for arcing protection if the lamp connector is made of lower quality heat resistive plastic, for example. The UBA2014 will restart though if the filament used for lamp detection (R1, R10 path shown in Figure 2) is still in place. What happens is that after this instant stop, and the consequent restart, the broken lamp will not ignite and subsequently the UBA2014 will run into time-out and enter the power-down state. The only way to leave the power down state is via a power cycle.

6.3 UBA2014 EOL circuits

There are many options for detecting the EOL of a lamp. This application note only features circuits for some of the many implementations available.

Example circuits:

- Circuit based on rectification (using DC blocking voltage).
- Circuit based on arcing/restriking and over power
- Circuit based on over power

6.4 Overpower detection

The voltage on the sense resistor, used for preheat current sensing (R14 in Figure 2 and R5 in Figure 21), can also be used to detect overpower. With a single diode and a resistor added to the standard application diagram, the ballast can be switched off if the current through this sense resistor is too high for too long. This overpower protection protects the ballast electronics, but is not guaranteed to prevent local overheating of a filament (see Figure 17).

6.5 Rectification detection

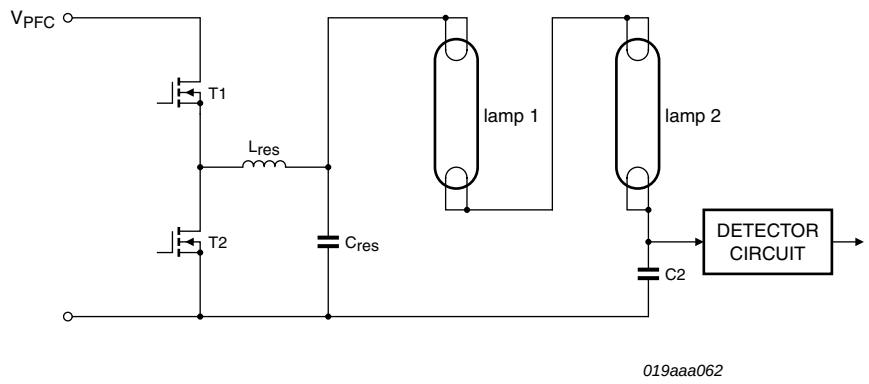


Fig 14. EOL DC blocking capacitor voltage

The voltage on the DC blocking capacitor indicates the asymmetric power by an asymmetric voltage across C2 (see Figure 14).

If the lamp has a rectifying effect (EOL), the voltage on DC blocking capacitor C2 will no longer be V_{PFC} / 2, but higher or lower. This voltage can be monitored with a circuit (see Figure 15). If the DC blocking capacitor voltage becomes too high or low, the ballast switches off.

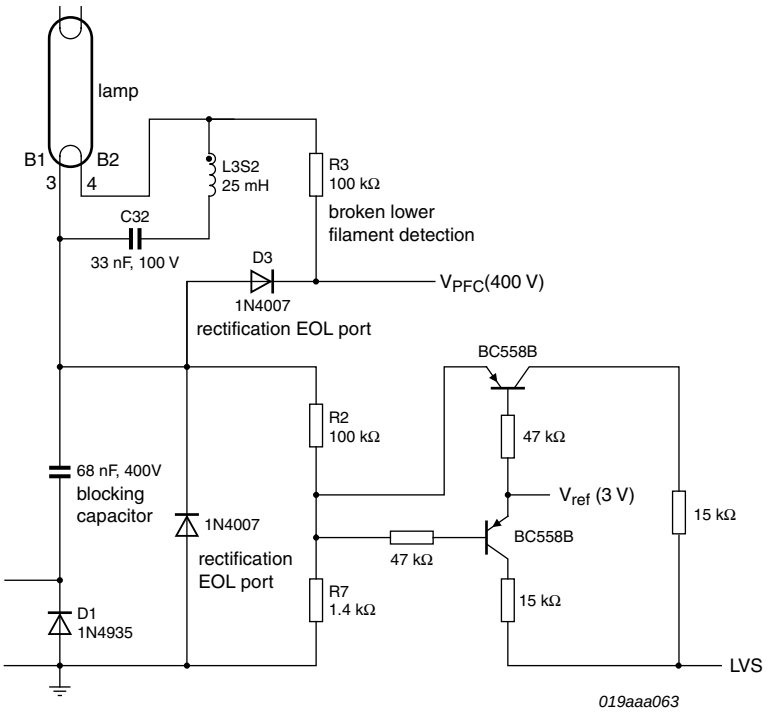


Fig 15. UBA2014 rectification EOL detection circuit

Figure 15 shows that the DC blocking voltage (normally V_{PFC} / 2), is divided with two resistors to 3 V. The circuit in Figure 15 is for a 400 V V_{PFC}. If a different PFC voltage is used, the two resistors values should be chosen according to Equation 1

$$\frac{V_{PFC} \times R1}{2 \times (R1 + R2)} = 3V \quad (1)$$

Two transistors monitor the divided DC blocking capacitor voltage, and if it rises above 3.7 V, or falls below 2.3 V, the circuit will trigger the IC protection. For a 400 V operated V_{PFC}, this means the “window “is between 170 V and 230 V.

The asymmetrical power as defined in Ref. 1 is given in Equation 2

$$P_{EOL} = \frac{abs(2 \times V_{CDC} - V_{bus}) \times I_{lamp}}{2} \quad (2)$$

For T5 tubes 7.5 W and for T4 5 W maximum asymmetrical power is allowed. No IEC specification exists for T8 tubes, but 10 W is a good limiting value.

The same circuit as in Figure 15 can be used with a difference reference voltage that can be made easily from V_{DD} to get a smaller detection window.

It is difficult to acquire/prepare a tube with rectification. For this purpose the IEC has made a test diagram, see Figure 16.

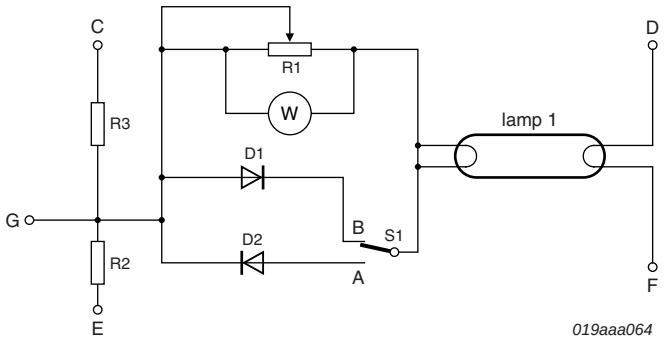
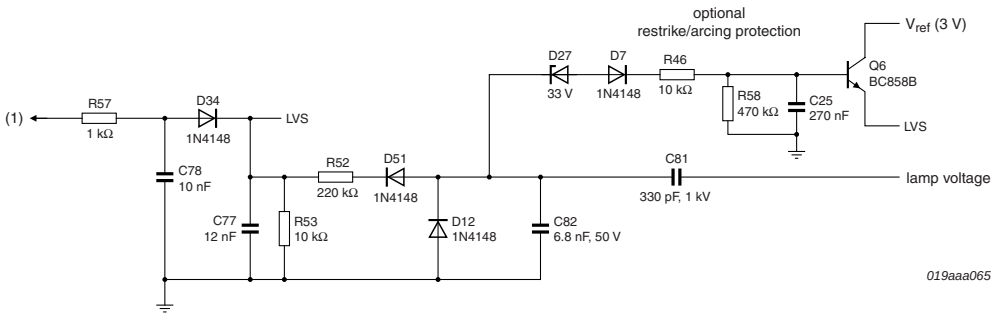


Fig 16. IEC EOL simulation circuit

6.6 Arcing/restriking detection

A lamp that is arcing/restriking will show spikes on the lamp voltage. Monitoring these spikes is the easiest way to detect arcing.



(1) R14 (see Figure 2)

Fig 17. Arc/restrike detection combined with overpower

The lamp voltage is connected to C81. It is first divided by C81 and C82 and then divided again by R52, R53 to match the range of the UBA2014 LVS pin. The circuit D27, D7 and R46 detects large spikes and charges C25. Resistor R58 discharges C25. If there are too many restrikes (or arcing) in too short a time, the ballast will go to into standby.

An alternative is to put the Zener diodes D14 and D6 in series with the resistor R24, so the circuit with Q5, R34, R38 and C24 is then not required. The time constant of C41, R27 should not be changed so much that the control loop inside the UBA2014 (used to limit the lamp voltage in case of no ignition), does not work properly.

6.6.1 Additional tests

In addition to more complex circuits from the IEC, one very simple test should be done with each new design. This test is to disconnect the lamp electrode wires one by one. This should be done at start-up, and during lamp operation. As a result, either the lamp keeps on running without damage to the ballast, or overheating of the electrodes, or the ballast switches into low power Standby protection mode.

7. Debugging a UBA2014 ballast

If a prototype ballast PCB application is switched on at full power, any design or layout soldering error can cause a large part of the circuit to be destroyed.

Limiting the power by using a current limited DC supply will only partly help as there is a minimum amount of power needed for tube ignition. This is more than enough power to damage the board.

The following steps that can be used to progressively debug a newly designed ballast PCB.

1. Connect a 13 V Zener (13.6 V, two times 6.8 V) across the UBA2014 V_{DD} supply. Use a 100 mA current limited 20 V lab supply to feed V_{DD} via a 470 Ω resistor. See Figure 18. The UBA2014 should be seen to start running at around 100 kHz. Depending on the protection circuit, it can stop after preheat or continue running. The gate drive on the low side MOSFET should be present.

   Remark: Do not continue with the following steps until this is observed.

2. Attach the 20 V DC supply to the half-bridge (instead of the PFC voltage). A square wave should be seen on the half-bridge and on the drive of both MOSFETs. The current in the resonant tank (even though small) can be measured.
3. Optional - The preheat capacitor can be grounded to CT (pin 1). The UBA2014 will stay in Preheat mode (the Capacitive mode protection is disabled in this state). Apply a voltage from a lab supply of 0.5 V to CSW (pin 2) via a 4.7 KΩ resistor. Remove the 20 V lab supply and the 470 Ω resistor mentioned in List item 1.
   Attach a high voltage scope probe on the lamp connector (LC resonance point). Apply the full DC V_{PFC} voltage. The half-bridge should be observed running at approximately 80 kHz, and with some preheat current in the burner.
4. Using a lab supply, the UBA2014 frequency can be changed, the lamp can even be ignited, but extreme care must be taken to increase the frequency slowly, so that if the lamp does not ignite, the maximum voltage of the resonance capacitor is not exceeded. The frequency must not be increased to below the resonance frequency, as this will cause Capacitive mode hard switching, and possible subsequent damage to the ballast. To avoid such a situation, the resonance capacitance should be doubled for this experiment. With this doubled value it is safe to bring the ballast frequency all the way down to f_{min} without causing any damage.

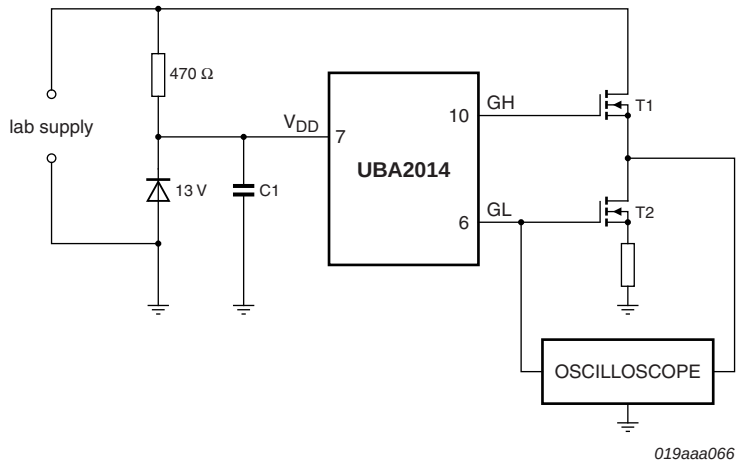


Fig 18. Debugging circuit

8. PCB design and layout guidelines

The following design considerations must be observed to ensure a good PCB layout.

1. Keep the high current loops short (see Figure 19).
2. Do not use the same ground PCB track that carries the large signal current for CT, CSW, CF and IREF (pins 1 to 4). This will inject noise into these pins, and that can cause a malfunction. Make the connection as shown in Figure 19.
3. Place the bulk capacitor close to the half-bridge. A PFC only charges this bulk capacitor, a resonant converter will have a current flow out but also back into the bulk capacitor (the current through the resonant capacitor C_{res} is reactive current). See Figure 19.

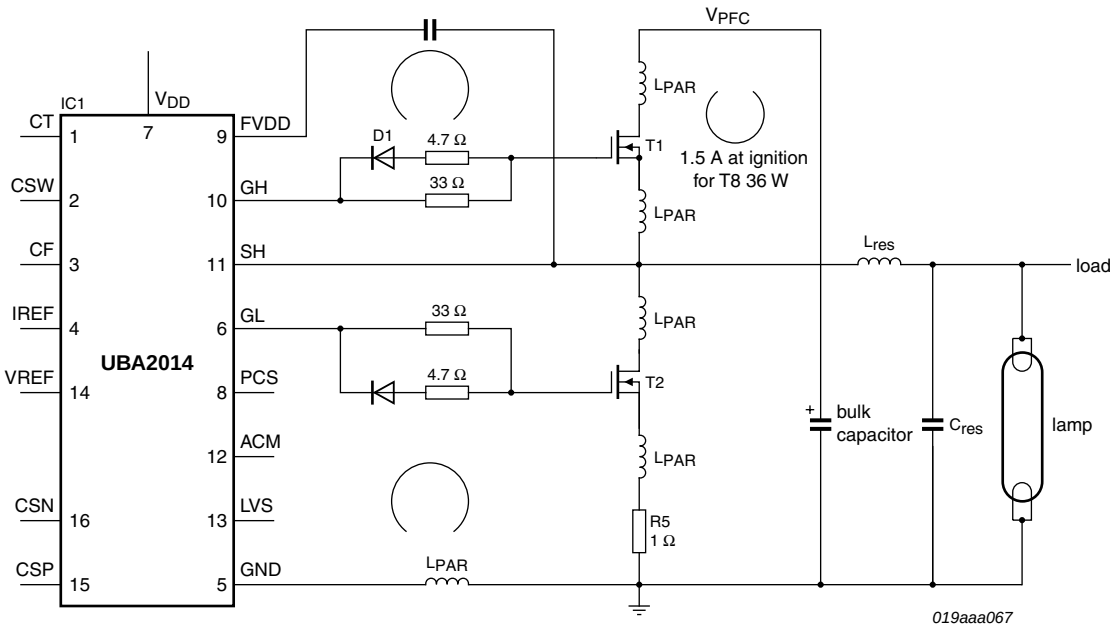


Fig 19. PCB layout circuit diagram

Overshoots and undershoots on gate and drain voltage should be limited in order to avoid damage to the UBA2014 and the MOSFETs. It is advisable to leave a 25 V to 50 V margin in the MOSFET breakdown voltage for this. So a half-bridge running on 400 V should have 450 V MOSFETs. Figure 20 shows an example board. The large buffer capacitor is C34 and Q2, Q3 (= T1, T2) are the half-bridge MOSFETs, on the top pins 8 to 16 of the UBA2014T.

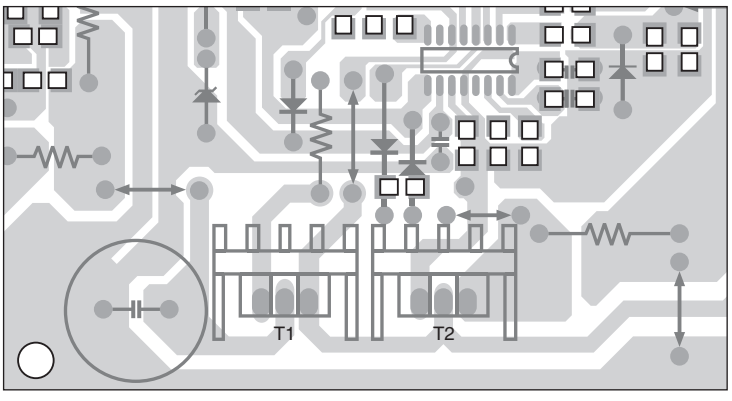


Fig 20. PCB: top view (partial)

8.1 Gate resistors

The gate drive circuit is an RLC series circuit. For an RLC series circuit, the condition giving no oscillation in case of a step response, is as given in Equation 3

$$R2C2 - 4LC > = 0 \quad (3)$$

The resistor R should be low enough so the gate drive does not open itself due to the Miller capacitance. The capacitance is known from the MOSFET specification, the inductor is the result of layout plus parasitic inductance of the MOSFET. Spice simulation is the most effective method to achieve optimal starting component values. Measurement is needed to verify/fine tune these values.

8.2 Coil air gap and windings

Do not place sensitive tracks, such as the ones to/from pins 1 to 4 of the UBA2014, close to the air gap of the resonant coil. This is a very noisy area (the location of the air gap depends on the specific coil design). Connecting the half-bridge to the inner winding of the coil will cause less radiated emission.

8.3 High dV/dt traces

The tracks driving the MOSFETs and the half-bridge signal can have a high dV/dt (particularly when hard switching). Leave 200 μm or more distance around these tracks to avoid capacitive coupling (or shield them with ground).

9. Inductive mode heating

In addition to the series resonant, inductive mode heating is also commonly used. Figure 21 shows the Inductive mode configuration with a TL8 36 W lamp. This topology is also known (mainly in the USA) as “Voltage mode”.

The main difference with the series resonant topology is that in the Inductive mode heating topology two secondary windings L1a and L1b are made on the resonant coil L1. So, in series resonant it the resonant inductor is a coil, in Inductive mode a transformer. As the secondary windings have little inductance (usually in the range 5 μH to 25 μH) the primary winding is dominant for the resonant tank. Figure 21 includes the optional EOL protection. The IEC requires either arcing or rectification, and either one can be used.

Capacitors are connected in series with the secondary windings, to make the transformer a voltage transformer, rather than a current transformer.

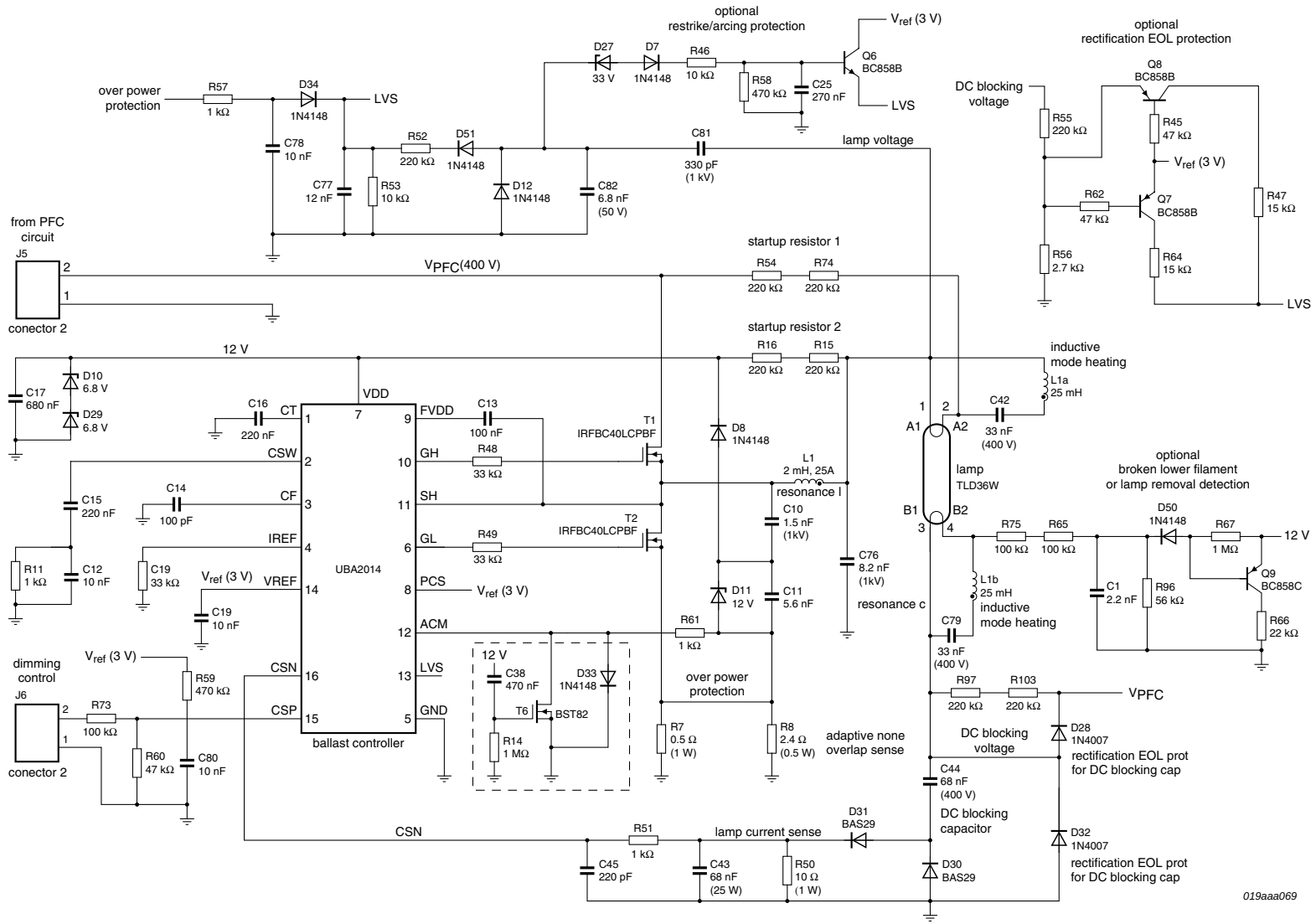


Fig 21. Application diagram: Inductive mode heating (Voltage mode)

9.1 Inductive mode preheat

A high end ballast has a short preheat time, less than 1.5 s. So, it is desirable to generate as much preheat energy as possible given a secondary inductance and capacitance, as this shortens the preheat time needed to fulfill the burner specifications.

Running at the maximum frequency of the UBA2014, f_{max} will give the highest preheat energy (using the Inductive mode topology). The circuit around T3 in Figure 21 is optional. It disables adaptive non-overlap during preheat, and by doing that, increases the preheat energy, thus allowing a shorter preheat time. Inductive mode heating typically gives a constant preheat energy, while the series resonant topology gives a constant preheat current. Burner specifications give both energy and current values.

9.1.1 Lamp electrode operating currents

The value of the secondary inductance and capacitance determine the currents through the electrodes during operation. These currents have a minimum, target and maximum value of the Sum of Squares (SoS). In Figure 22 the lamp discharge current $I_D = I_{LH} - I_{LL}$.

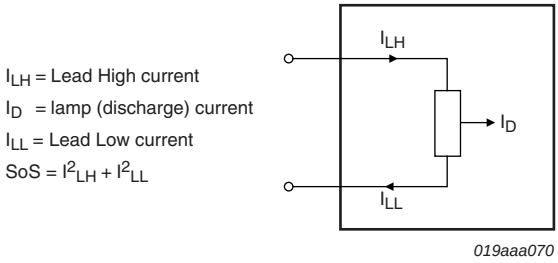


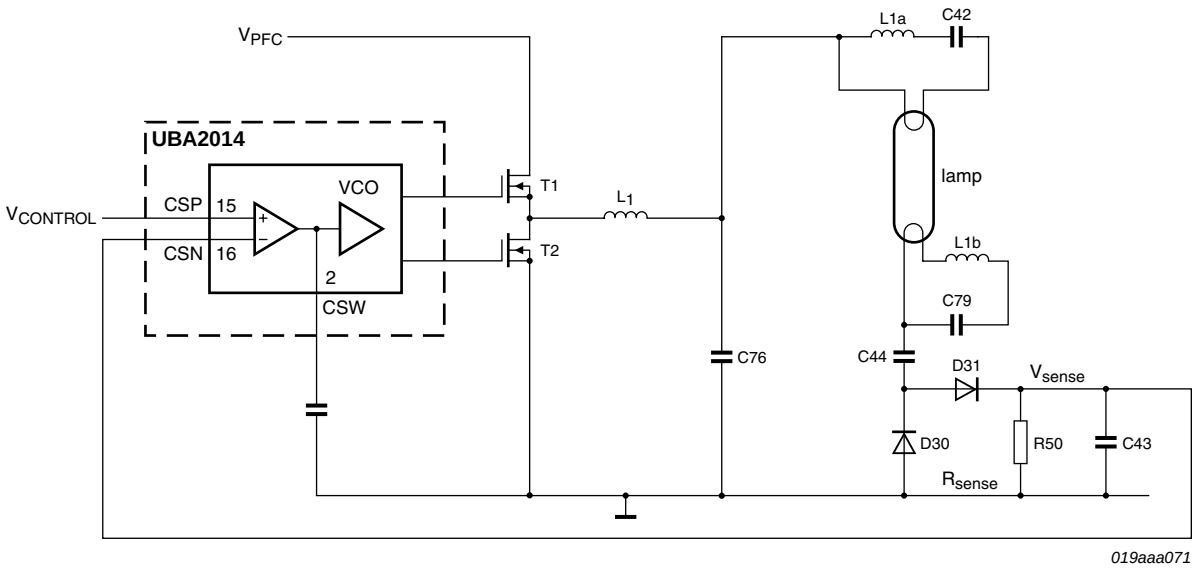
Fig 22. Sum of Squares (SoS) definition

Table 4 lists the most commonly used T5 and T8 lamps with primary/secondary inductance and capacitance values that will ensure operation close to the target specifications of the tube lamps.

The polarity of the secondary windings indicated in the Figure 21 must be correct or the SoS will be higher. **The polarity does not make a difference for preheat but does during lamp operation.**

9.1.2 Lamp current measurement

The UBA2014 has a feedback control loop based on lamp current measurement. With Inductive mode heating, the lamp current alone can be measured (with series resonant, the sense resistor measures the lamp current plus the resonant capacitor current). As (only) the lamp current is measured, Inductive mode heating allows deeper dimming than series resonant.



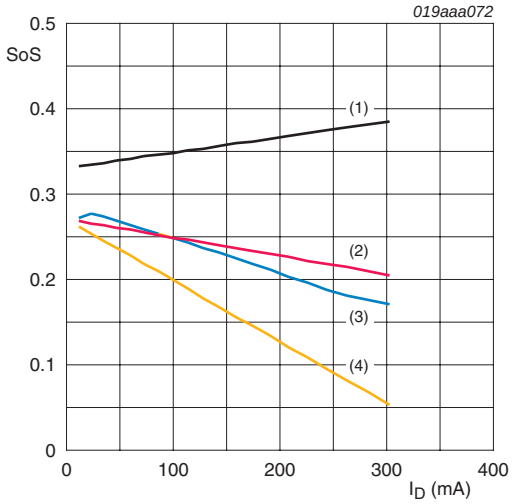
Component numbers also relate to components in Figure 21

Fig 23. Current feedback control loop

The lamp current is rectified and measured across a sense resistor. The measured value is compared with a control voltage applied to the CSP pin. The control loop changes the half-bridge frequency until the measured voltage is equal to the control voltage. The advised full scale input of the CSN pin is 2.5 V. R_{sense} is given by Equation 4:

$$R_{sense} = \frac{4}{I_{lamp(RMS)}} \quad (4)$$

After R_{sense} has been picked from the E series, the CSP circuit can be optimized. For example 0 V to 10 V input the ratio of input voltage to CSP voltage can be calculated such that at 10 V input the maximum lamp current is reached. Many operating frequencies versus resonant tank coil and capacitor combinations are possible that will give the correct power. Table 4 gives suggested values for various TL5 and TLD lamps. The values given in Table 4 and shown in Figure 24 are such, that over the full lamp operation range, the SoS is close to the SoS target. The nominal full power frequency is around 45 kHz. If there is no need for deep dimming, a much lower secondary inductance (range 1 μH to 4 μH) and a much higher secondary capacitance (100 nF to 220 nF) can also be used.



(1) SoS_{max}
(2) SoS_{target}
(3) SoS_{actual}
(4) SoS_{min}

Fig 24. SOS lines for the values of the TLD (T8) 36 W lamp, as shown in Table 4; C(dV/dt) (capacitance on the half-bridge for V_{DD} power supply) = 1 nF.

Table 4. Suggested values for resonant tank for different lamp types

Lamp	Resonant coil (mH)	Resonant capacitor (nF)	Secondary inductance (µH)	Secondary capacitance (nF)	V_{bus} (V)	Preheat energy (J)	Preheat time (s)
TLD 18 W	2.14	4.7	11	39	400	4	1.2
TLD 36 W	1.9	8.2	14	33	400	4.6	1.2
TLD 58 W	1.38	8.2	14	27	400	5	1.2
TLD 70 W	1.3	8.2	17	27	400	6.5	1.2
TL5 HO 24 W	2	4.7	10	33	400	3.2	1.2
TL5 HO 39 W	1.8	4.7	10	27	400	3	1.2
TL5 HO 54 W	1.3	4.7	8	33	400	3.8	1.2
TL5 HO 49 W	2.7	4.7	20	15	450	2.8	1.2
TL5 HO 80 W	1.1	8.2	15	22	400	5.8	1.2
TL5 HE 14 W	3.65	4.7	18	22	400	2.2	1.2
TL5 HE 21 W	3.56	4.7	18	22	400	2.2	1.2
TL5 HE 28 W	3.83	4.7	16	22	450	2.2	1.2
TL5 HE 35 W	3.88	4.7	16	22	480	2.2	1.2

10. References

[1] IEC 61347-2

11. Legal information

11.1 Definitions

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12. Contents

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