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Power management for the LPC900 family

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Document information

Info	Content
Keywords	Power management for the LPC900 family.
Abstract	This document will describe different ways to reduce power consumption on the LPC900 parts.

PHILIPS

Revision history

Rev	Date	Description
01	20050329	Initial version

Contact information

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1. Introduction

The purpose of this document is to explain the different power management methods for the LPC900 family.

Many applications will have strict power requirements, and there are several methods of lowering the rate of power consumption without sacrificing performance. Calculating the predicted power use is important to characterize the system's power supply requirements. The LPC900 peripherals can be put into low power modes by setting some bits in the registers. The utility of these low power modes depends on the specific application.

The basic explanation of this note is based on the LPC935 tested with a limited sample, but it is applicable to all of the LPC900 general purpose devices.

2. Power management modes

CMOS digital logic device power consumption is affected by supply voltage and clock frequency. The amount of current consumption is directly proportional to the voltage of the power. The power consumption depends on the number of active peripherals, and also depends on whether the oscillator is On or Off and whether the CPU is On or Off.

The P89LPC935 is designed to run at 12 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to '1' to lower the power consumption further. On any reset, CLKLP is '0' allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

The P89LPC935 supports three different power reduction modes as determined by SFR bits PCON.1-0 shown in the following section.

2.1 Idle mode

In Idle mode the core is turned off, peripherals can still run or can be powered down with the PCONA SFR. Any enabled interrupt source or reset will terminate Idle mode.

2.2 Power-down mode

Power-down mode stops the oscillator in order to minimize power consumption. Only the System Timer / RTC, the Comparators, the Brown-out Detect and the WDT can still run (if enabled in PCONA). The LPC900 can exit Power-down mode via any reset, or certain interrupts - external pins INT0/INT1, brownout Interrupt, keyboard interrupt, real time clock (system timer), watchdog, and comparators.

Waking up by reset is only enabled if the corresponding reset function on pin P1.5 is enabled, and waking up by interrupt is only enabled if the corresponding interrupt is enabled and the EA SFR bit (IEN0.7) is set. When the processor wakes up from Power-down mode, the LPC900 will start the oscillator immediately and begin execution when the oscillator is stable. Oscillator stability is determined by counting 1024 CPU clocks after start-up when one of the crystal oscillator configurations is used, or 256 clocks after start-up for the internal RC or external clock input configurations.

2.3 Total power-down mode

In total Power-down mode the CPU and oscillator will be turned off. Only the System Timer / RTC and the WDT can still run (if enabled). The following are the wake-up options supported: Watchdog Timer (can generate Interrupt or Reset), External interrupts INT0 / INT1, Keyboard Interrupt, and Real Time Clock/System Timer.

2.4 Power management modes summary

Table 1 shows the different power management modes.

Table 1: LPC900 power management modes

LPC900 mode	Crystal Oscillator	CPU	Peripherals
Normal	On	On	On (individual peripherals can be powered down with PCONA)
Idle	On	Off	On (individual peripherals can be powered down with PCONA)
Power-down	Off[1]	Off	System timer / RTC, Comparators, BOD, WDT can run when enabled
Total Power-down	Off[1]	Off	System timer / RTC, WDT can run when enabled

[1] The crystal oscillator is turned on in Power-down mode if the RTC is enabled and a crystal is selected as the clock source.

3. Measuring lowest power consumption modes

Since power consumption is affected by supply voltage and clock frequency, lowering the clock frequency and operating voltage will lower the power consumption.

The oscillator frequency OSCCLK of the LPC900 family can be divided down, by an interger, up 510 times by configuring the dividing register DIVM The output of the frequency CCLK of the divider is according the formula CCLK = OSCCLK/2N. Where N is the value of DIVM. The CCLK frequency can be in the range of OSCCLK to OSCCLK/510. For N = 0 CCLK = OSCCLK.

The source for OSCCLK depends on the selecting in the UCFG register and can be from an internal oscillator with an external crystal, Internal RC oscillator or internal watchdog oscillator.

The LPC900 family has 2.4 V to 3.6 V VDD operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V). The following samples include lower frequency and supply voltage to lower the power consumption.

3.1 Current consumption in Idle mode

In Idle mode the core is turned off, peripherals can still run or can be powered down with the PCONA SFR. Any enabled interrupt source or reset will terminate Idle mode.

3.1.1 Measurement configuration

- When using external crystal 32.768 kHz the capacitor C1=C2=33pF
- When using external crystal 11.0592 MHz the capacitor C1=C2=22pF
- All ports have been set as Quasi-bidirectional except P1.2,P1.3,P1.5 and at high level

- After this, the MCU is put into idle mode
- Hardware configuration as in Figure 1.

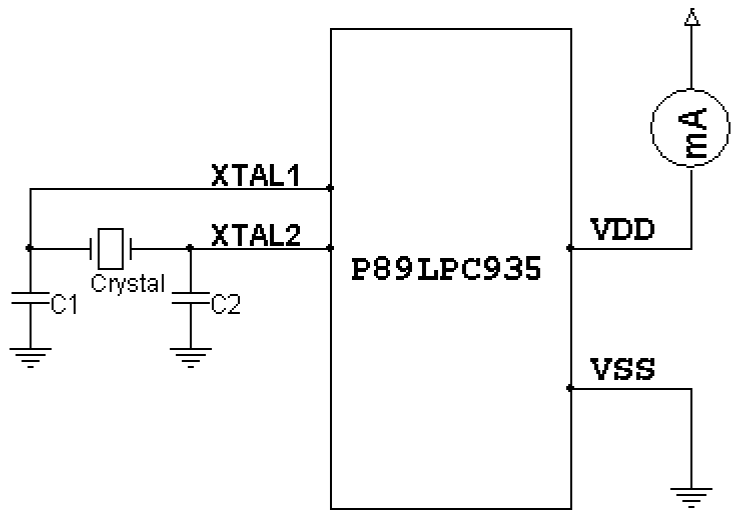

Fig 1. Current measurement configuration

3.1.2 Software example

```
#include<reg935.h>
void delay(int x)
{
 int j=0;
 while(x>=0)
 {
  for (j=0; j<1100; j++)
  {
  }
  x--;
 }
}
void main(void)
{
 P0M1 = 0x00;  //set P0 as Quasi-bidirectional
 P0M2 = 0x00;
 P1M1 = 0x20;
 P1M2 = 0x00;
 P2M1 = 0x00;
 P2M2 = 0x00;
 P3M1 &= 0xfc;
 P3M2 &= 0xfc;
 P0  = 0xff;
 P1  = 0xff;
 P2  = 0xff;
```

```
 P3  = 0xff;
 RTCCON&=0xfe; //stop RTC
 WDCON=0x00;  //stop WDT
 //DIVM=0x64;
 AUXR1|=0x80;// reduces power consumption in the clock circuits
           // if CCLK is 8 MHz or slower,
 P2=0xfe;
 delay(100);
 P2=0xff;
 PCONA|= 0xff;  // turn off all peripherals that can be turned off
 PCON|=0x21;    // enter Idle mode
 while(1);
}
```

3.1.3 Measurement results in Idle mode

The following tables and graphs show the measurement results of the LPC900 family in Idle mode.

Table 2: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	32.768 kHz	62.7 µA	72.5 µA	90.2 µA
Idle DIVM = 0Ah	1.6384 kHz	57.5 µA	64.8 µA	77.2 µA
Idle DIVM = 64h	0.16384 kHz	56.8 µA	64.1 µA	76.9 µA
Idle DIVM = FFh	0.06 kHz	55.8 µA	64.1 µA	76.2 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

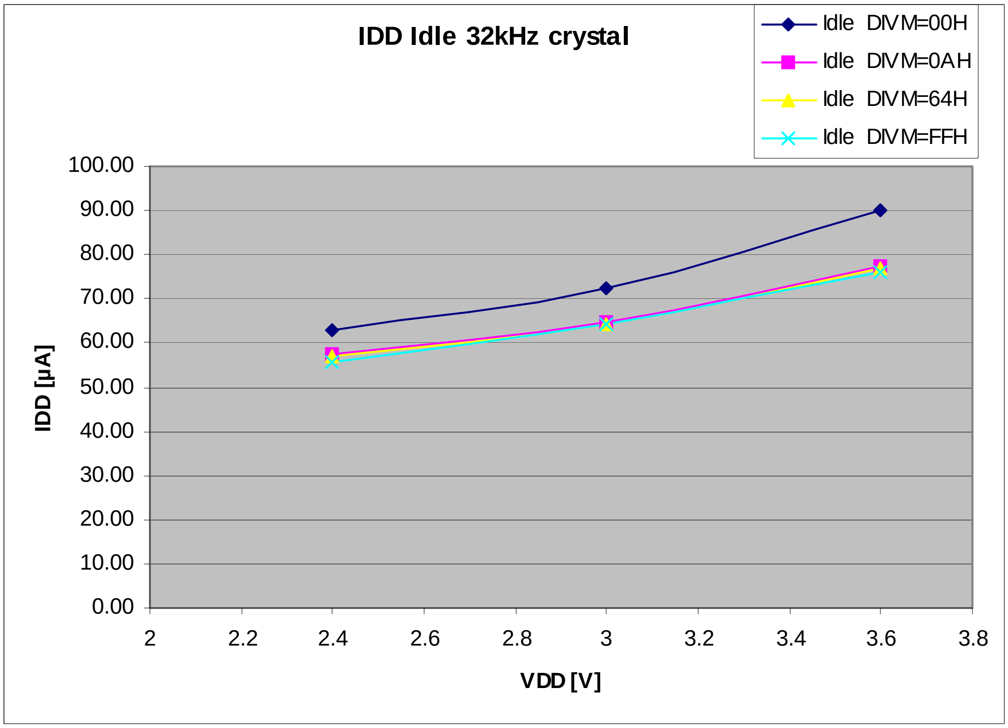

Fig 2. IDD Idle with a 32 kHz crystal

Table 3: Current consumption IDD high frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	11.059 MHz	2.50 mA	3.61 mA	4.80 mA
Idle DIVM = 0Ah	553 kHz	0.71 mA	1.09 mA	1.45 mA
Idle DIVM = 64h	55.3 kHz	0.63 mA	0.93 mA	1.28 mA
Idle DIVM = FFh	21.7 kHz	0.62 mA	0.92 mA	1.27 mA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

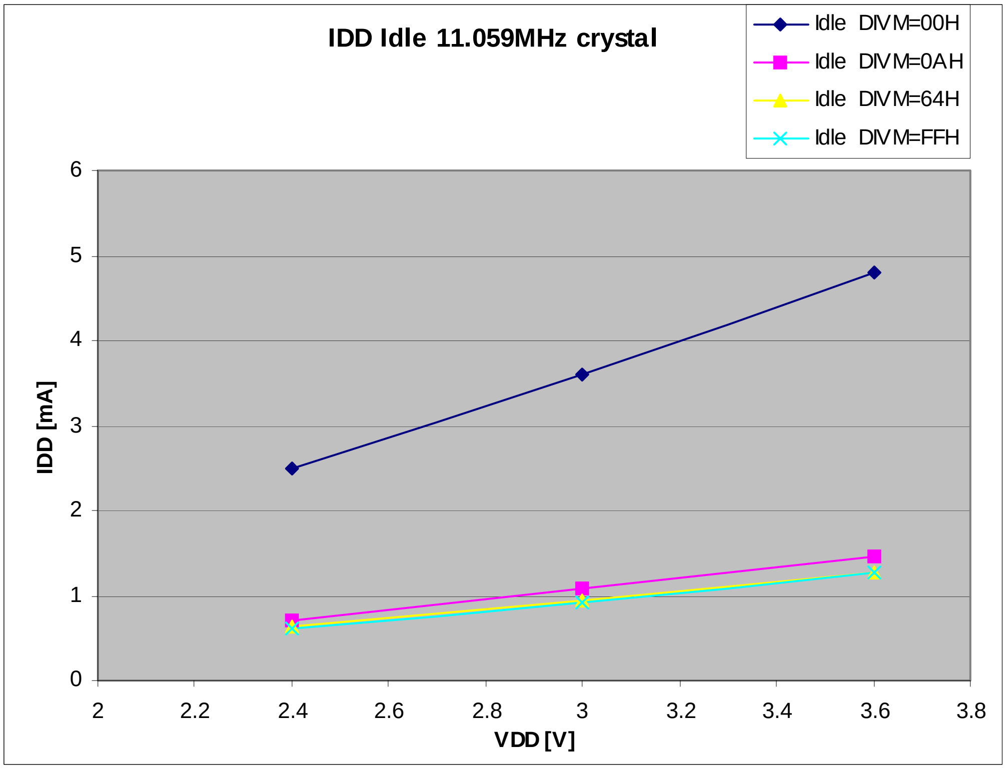

Fig 3. IDD Idle with a 11.059 MHz crystal

Table 4: Current consumption IDD internal oscillator

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	7.3728 MHz	1.54 mA	2.12 mA	2.80 mA
Idle DIVM = 0Ah	369 kHz	0.35 mA	0.44 mA	0.54 mA
Idle DIVM = 64h	36.9 kHz	0.29 mA	0.36 mA	0.43 mA
Idle DIVM = FFh	14.5 kHz	0.29 mA	0.35 mA	0.43 mA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

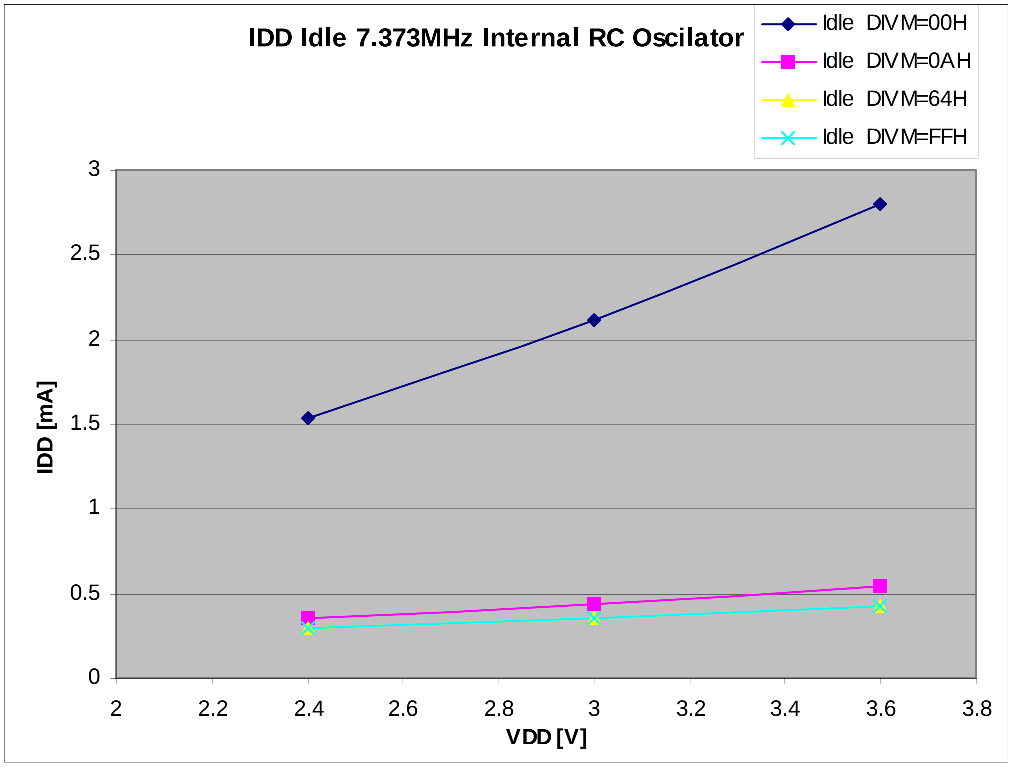

Fig 4. IDD Idle with a 7.37 MHz Internal oscillator

Table 5: Current consumption IDD watchdog oscillator

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	400 kHz	159.8 µA	202.8 µA	256.8 µA
Idle DIVM = 0Ah	20 kHz	84.7 µA	99.6 µA	117.5 µA
Idle DIVM = 64h	2 kHz	81.1 µA	94.5 µA	110.9 µA
Idle DIVM = FFh	0.784 kHz	80.9 µA	94.2 µA	110.5 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

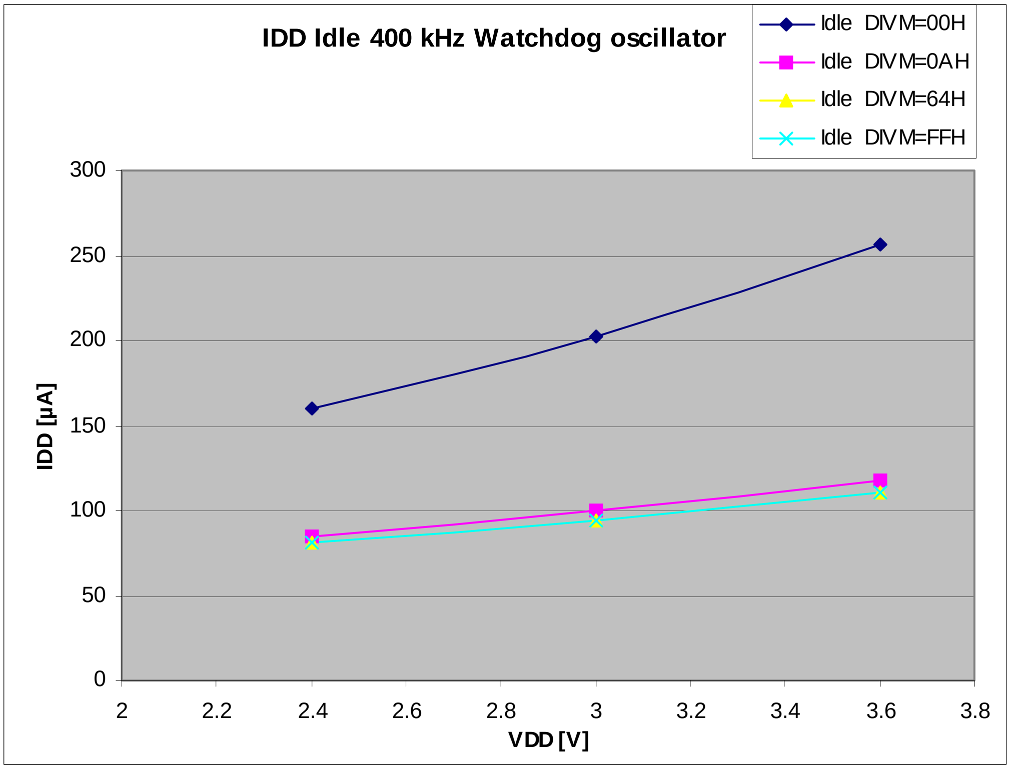

Fig 5. IDD Idle with a 400 kHz internal Watchdog oscillator

3.2 Current consumption in Power-down mode

This example provides a static method of measuring the current consumption by the microcontroller in Power-down mode and without any I/O activity, while the voltage comparators are active.

3.2.1 Measurement configuration

- When using external crystal 32.768 kHz the capacitor C1=C2=33pF
- When using external crystal 11.0592 MHz the capacitor C1=C2=22pF
- All ports have been set as Quasi-bidirectional except P1.2,P1.3,P1.5 and at high level
- Enable analog voltage comparator
- After this the MCU is put into Power-down mode
- Hardware configuration as Figure 1.

3.2.2 Software example

```
#include<reg935.h>
void delay(int x)
{
 int j=0;
 while(x>=0)
```

```
 {
  for (j=0; j<1100; j++)
  {
  }
  x--;
 }
}
void main(void)
{
 P0M1 = 0x00;  //set P0 as Quasi-bidirectional
 P0M2 = 0x00;
 P1M1 = 0x20;
 P1M2 = 0x00;
 P2M1 = 0x00;
 P2M2 = 0x00;
 P3M1 &= 0xfc;
 P3M2 &= 0xfc;
 P0  = 0xff;
 P1  = 0xff;
 P2  = 0xff;
 P3  = 0xff;
 RTCCON&=0xfe; //stop RTC
 WDCON=0x00;  //stop WDT
 //DIVM=0x64;
 AUXR1|=0x80;// reduces power consumption in the clock circuits
            // if CCLK is 8 MHz or slower,
 P2=0xfe;
 delay(100);
 P2=0xff;
 PCONA|= 0xff;  // turn off all peripherals that can be turned off
 PCON|=0x22;    // enter Power-down mode
 while(1);
}
```

3.2.3 Measurement results in Power-down mode

This example provides a static method of measuring the current consumption by the microcontroller in Power-down mode and without any I/O activity, while the voltage comparators are active.

Table 6: Current consumption IDD in Power-down mode

Mode	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Power-down mode	51.9 μA	54.6 μA	58.1 μA
Power-down while Comparators are active	66.5 μA	69.3 μA	73.2 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample. Brownout is disabled, RTC and watchdog timer are turned off.

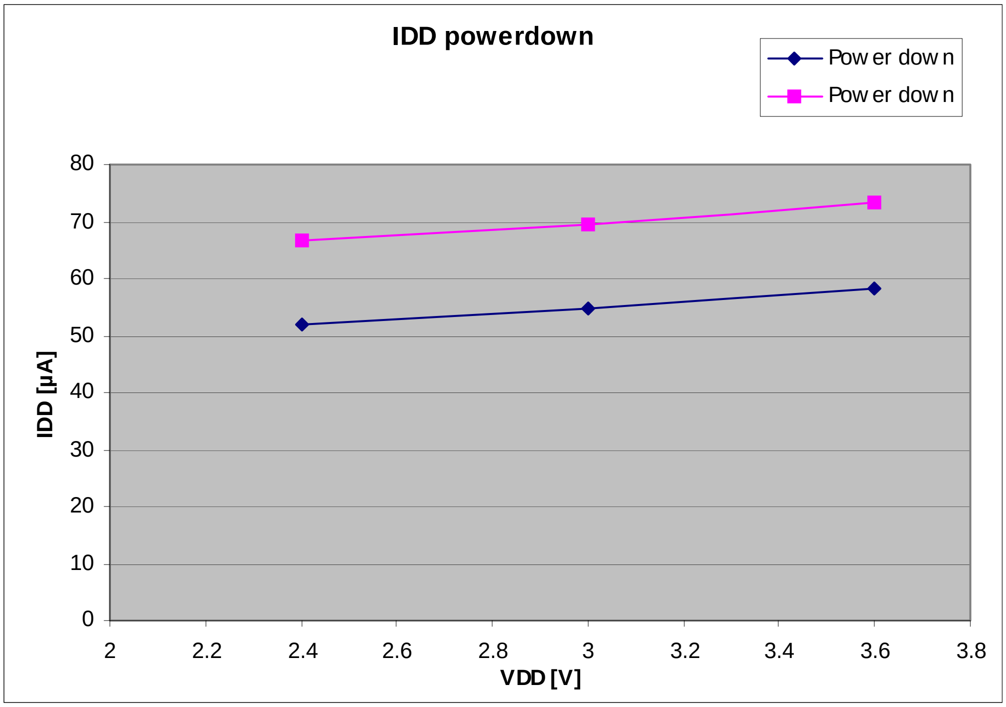

Fig 6. IDD Power-down

3.3 Current consumption in total Power-down mode

This example provides a static method of measuring the current consumed by the microcontroller in total Power-down mode, without any I/O ports and any peripherals active.

3.3.1 Measurement configuration

- When using an external crystal 32.768 kHz the capacitor C1=C2=33pF
- When using an external crystal 11.0592 MHz the capacitor C1=C2=22pF
- All ports have been set as Quasi-bidirectional except P1.2,P1.3,P1.5 and at high level
- After this, the MCU is put into total Power-down mode
- Hardware configuration as Figure 1.

3.3.2 Software example

```
#include<reg935.h>
void delay(int x)
{
 int j=0;
 while(x>=0)
 {
  for (j=0; j<1100; j++)
  {
  }
```

```
  x--;
 }
}
void main(void)
{
 P0M1 = 0x00;  //set P0 as Quasi-bidirectional
 P0M2 = 0x00;
 P1M1 = 0x20;
 P1M2 = 0x00;
 P2M1 = 0x00;
 P2M2 = 0x00;
 P3M1 &= 0xfc;
 P3M2 &= 0xfc;
 P0  = 0xff;
 P1  = 0xff;
 P2  = 0xff;
 P3  = 0xff;
 RTCCON&=0xfe; //stop RTC
 WDCON=0x00;  //stop WDT
 //DIVM=0x64;
 AUXR1|=0x80;// reduces power consumption in the clock circuits
            // if CCLK is 8 MHz or slower,
 P2=0xfe;
 delay(100);
 P2=0xff;
 PCONA|= 0xff;  // turn off all peripherals that can be turned off
 PCON|=0x23;    // enter total Power-down mode
 while(1);
}
```

3.3.3 Measurement results in total Power-down mode

This example provides a static method of measuring the current consumed by the microcontroller in total Power-down mode, without any I/O ports and peripherals is active.

Table 7: Current consumption IDD in total Power-down mode

Mode	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Power-down mode	1 μA	1 μA	1 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C). Brownout is disabled, RTC and watchdog timer are turned off.

3.4 Current consumption in active mode using DIVM

This example provides a static method of measuring the current consumed by the micro-controller in different power management modes.

3.4.1 Measurement configuration

- When using external crystal 32.768 kHz the capacitor C1=C2=33pF

- When using external crystal 11.0592 MHz the capacitor C1=C2=22pF
- All ports have been set as Quasi-bidirectional except P1.2,P1.3,P1.5 and at high level
- After this, the MCU is put into different power management mode
- Hardware configuration as Figure 1.

3.4.2 Software example

```
#include<reg935.h>
void delay(int x)
{
 int j=0;
 while(x>=0)
 {
  for (j=0; j<1100; j++)
  {
  }
  x--;
 }
}
void main(void)
{
 P0M1 = 0x00;  //set P0 as Quasi-bidirectional
 P0M2 = 0x00;
 P1M1 = 0x20;
 P1M2 = 0x00;
 P2M1 = 0x00;
 P2M2 = 0x00;
 P3M1 &= 0xfc;
 P3M2 &= 0xfc;
 P0  = 0xff;
 P1  = 0xff;
 P2  = 0xff;
 P3  = 0xff;
 RTCCON&=0xfe; //stop RTC
 WDCON=0x00;  //stop WDT
 //DIVM=0x64;
 AUXR1|=0x80;// reduces power consumption in the clock circuits
            // if CCLK is 8 MHz or slower,
 P2=0xfe;
 delay(100);
 P2=0xff;
 PCONA|= 0xff;  // turn off all peripherals that can be turned off
 while(1);
}
```

3.4.3 Measurement results in Active mode

In active mode, the CPU is still running and the peripherals are turned off in PCONA.

Table 8: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	32.768 kHz	73.9 µA	88.1 µA	115.0 µA
Active DIVM = 0Ah	1.6384 kHz	61.7 µA	67.2 µA	84.8 µA
Active DIVM = 64h	0.16384 kHz	60.3 µA	66.6 µA	83.6 µA
Active DIVM = FFh	0.06 kHz	59.1 µA	66.3 µA	83.1 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

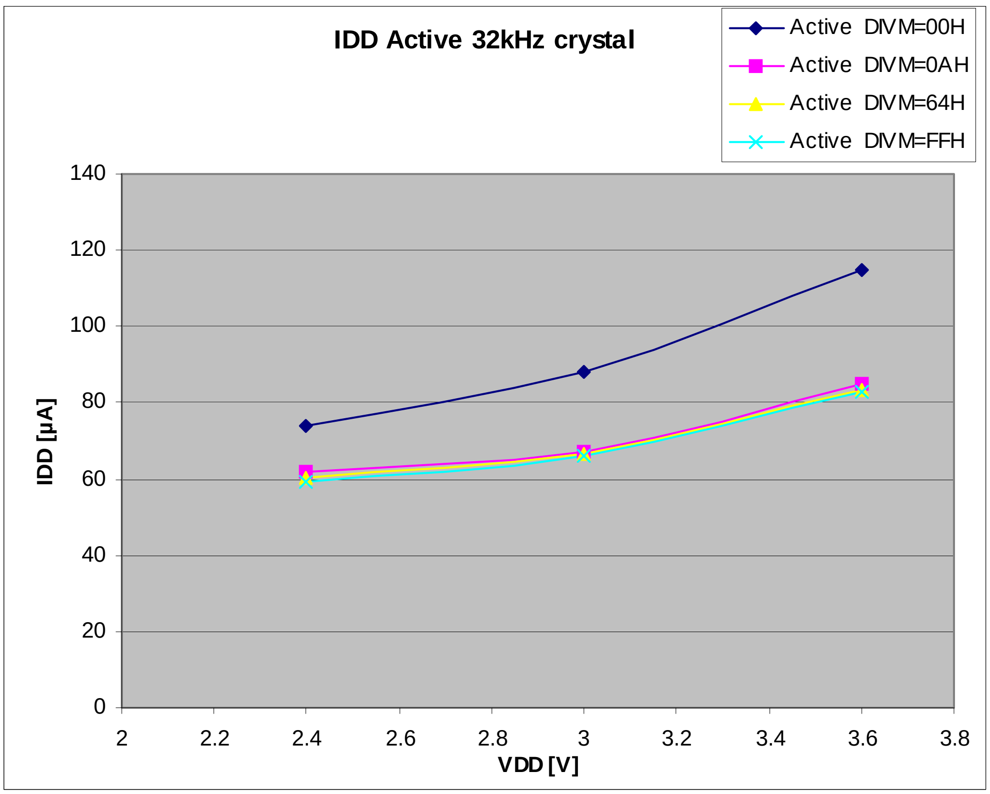

Fig 7. IDD Active with a 32 kHz crystal

Table 9: Current consumption IDD high frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	11.059 MHz	4.56 mA	6.78 mA	8.83 mA
Idle DIVM = 0Ah	553 kHz	0.85 mA	1.41 mA	1.70 mA
Idle DIVM = 64h	55.3 kHz	0.67 mA	1.15 mA	1.35 mA
Idle DIVM = FFh	21.7 kHz	0.65 mA	1.14 mA	1.33 mA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

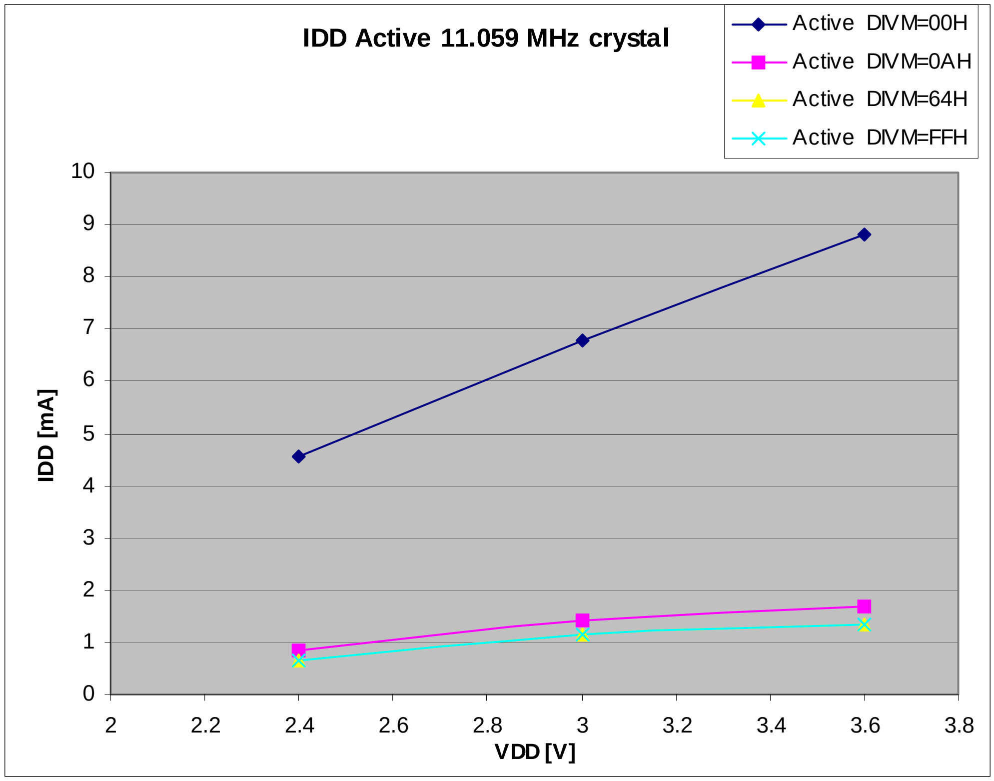

Fig 8. IDD Active with a 11.059 MHz oscillator

Table 10: Current consumption IDD internal oscillator

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	7.3728 MHz	2.97 mA	4.0 mA	5.3 mA
Idle DIVM = 0Ah	369 kHz	0.43 mA	0.54 mA	0.68 mA
Idle DIVM = 64h	36.9 kHz	0.31 mA	0.38 mA	0.48 mA
Idle DIVM = FFh	14.5 kHz	0.29 mA	0.37 mA	0.44 mA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

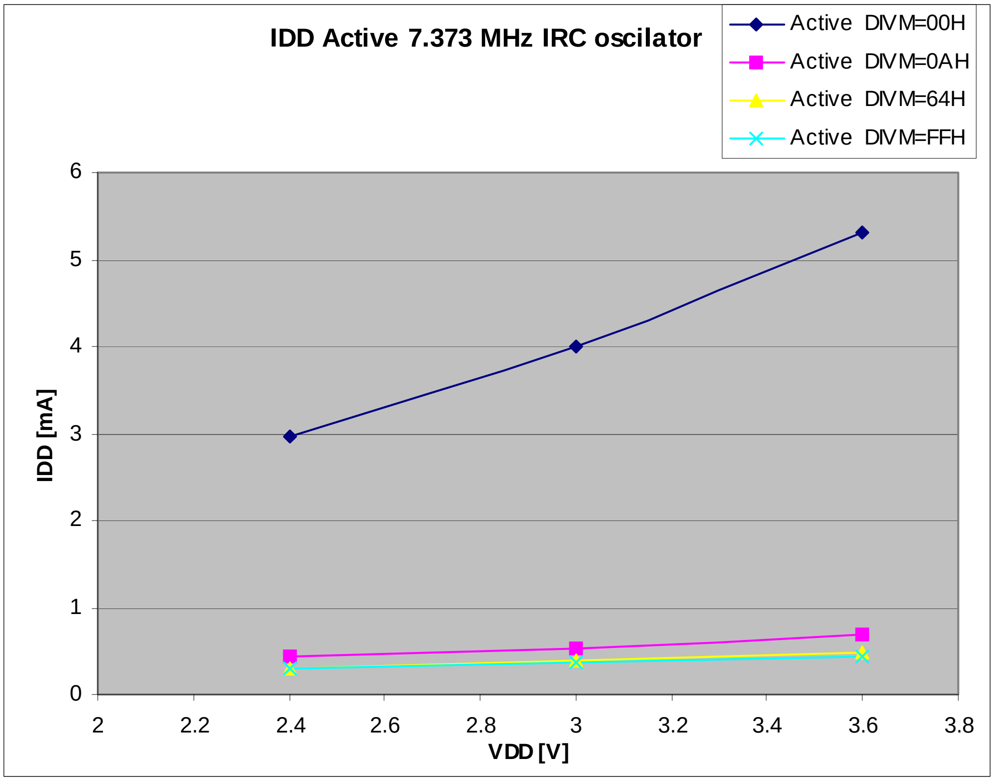

Fig 9. IDD Active with a 7.373 MHz Internal RC oscillator

Table 11: Current consumption IDD watchdog oscillator

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Idle DIVM = 00h	400 kHz	249.5 µA	333.5 µA	420 µA
Idle DIVM = 0Ah	20 kHz	87.1 µA	110.5 µA	166.5 µA
Idle DIVM = 64h	2 kHz	85.7 µA	104.9 µA	128.0 µA
Idle DIVM = FFh	0.784 kHz	84.8 µA	103.6 µA	127.2 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample.

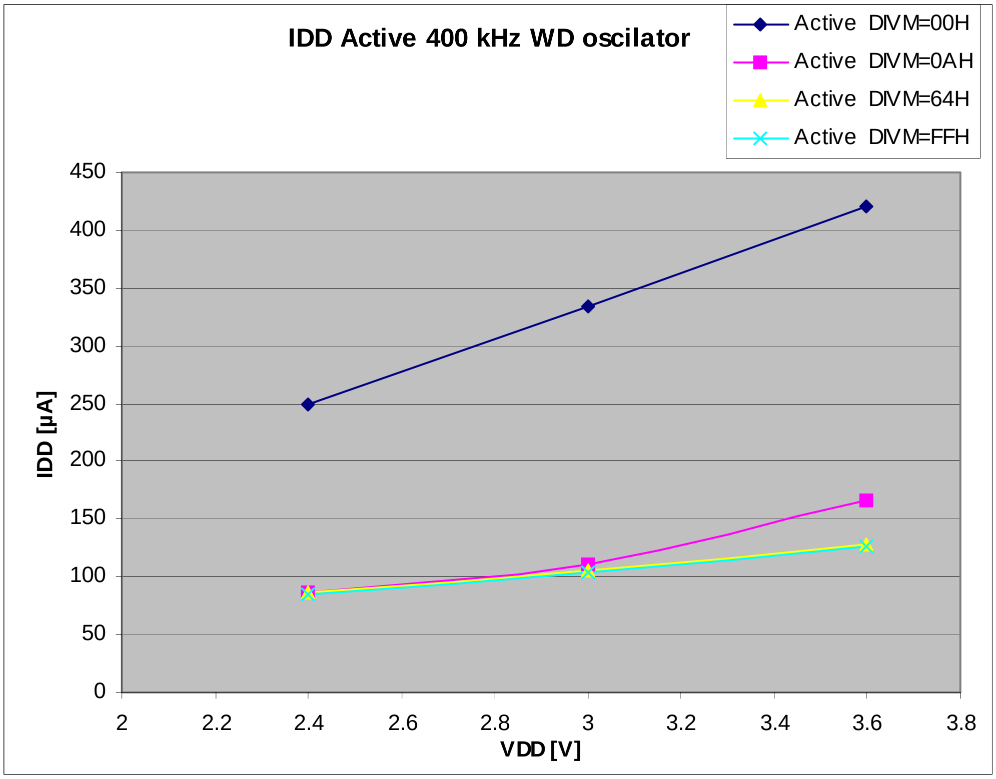

Fig 10. IDD Idle with a internal Watchdog oscillator

3.5 Current consumption in Power-down with RTC

This example provides a static method of measuring the current consumed by the RTC.

We will measure power consumption of RTC using 32.768 kHz crystal and slow

down the clock frequency of the CPU when using internal RC oscillator.

3.5.1 Measurement configuration

- When using an external crystal 32.768 kHz the capacitor C1=C2=33pF
- All ports have been set as Quasi-bidirectional except P1.2,P1.3,P1.5 and at high level
- Internal RC oscillator is used for the core
- Hardware configuration as Figure 1.

3.5.2 Software example

```
#include<reg932.h>
#include<intrins.h>
int RTC_Timer_Counter;
void delay(int x)
{ int j=0;
  while(x>=0)
 {for (j=0; j<1100; j++);
  x--; }
}
}
void RTC_ISR() interrupt 10
{  RTC_Timer_Counter++;
  if (RTCCON&0x80==0x80 )
    {
    RTCCON&=0x63;   // reset RTC interrupt flag
    if(RTC_Timer_Counter++>10)
      {
      P2=~P2;
      RTC_Timer_Counter=0;
      }
    }
}
void main(void)
{
  P0M1 = 0x00;
  P0M2 = 0x00;
  P1M1 = 0x20;
  P1M2 = 0x00;
  P2M1 = 0x00;  // set P2 to Quasi-bidirectional mode
  P2M2 = 0x00;
  P0  = 0xff;
  P1  = 0xff;
  P2  = 0xff;
  RTCCON&=0xfe;
  WDCON=0x00;
  // DIVM=0x64;
  AUXR1|=0x80;  // reduces power consumption in the clock circuits.
  RTCCON&=0x7F;
  RTCH=0x0f;
  RTCL=0xff;
  RTCCON|=0x43;
  EWDRT=1;
  PCONA|= 0x7f; // turn off all peripherals that can be turned off
  P2=0xfe;
  delay(100);
  P2=0xff;
   EA=1;         //enable all interrupt
   PCONA|= 0x7f; //turn off all peripherals except RTC
  PCON |= 0x23;  // switch to total Power-down mode
  _nop_();
```

```
  _nop_();
 while(1) {
         PCONA|= 0x7f;
         PCON |= 0x23;  // switch to total Power-down mode
         _nop_();
         _nop_();
         }
}
```

3.5.3 Measurement results RTC running

Table 12 shows the results of the power consumption when the RTC is running.

Table 12: Current consumption IDD Power-down RTC running on low speed crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	32.768 kHz	105.1 µA	118.2 µA	138.9 µA
Active DIVM = 01h	16.384 kHz	96.2 µA	105.2 µA	116.5 µA
Active DIVM = 02h	8.192 kHz	96.0 µA	104.6 µA	116.3 µA
Total Power-down	0.0	6.4 µA	10.2 µA	18.0 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample. Brownout is disabled, RTC is enabled and watchdog timer is turned off.

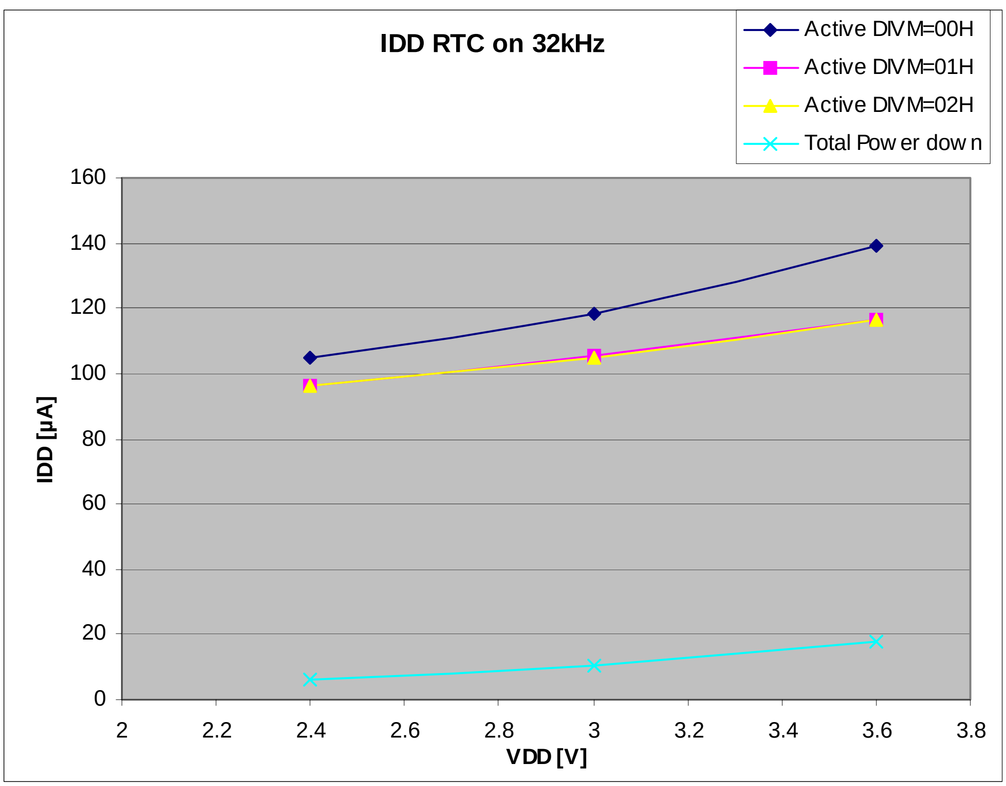

Fig 11. IDD RTC enabled using a 32 kHz crystal

Table 13: Current consumption IDD Power-down RTC running on low speed crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	7.3728 MHz	3.02 mA	4.13 mA	5.36 mA
Active DIVM = 0Ah	369 kHz	0.47 mA	0.58 mA	0.72 mA
Active DIVM = 64h	36.9 kHz	0.35 mA	0.41 mA	0.49 mA
Active DIVM = FFh	14.5 kHz	0.34 mA	0.40 mA	0.48 mA
Total Power-down	0.0	6.6 μA	10.8 μA	19.0 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C) with a limited sample. Brownout is disabled, RTC is enabled and watchdog timer is turned off.

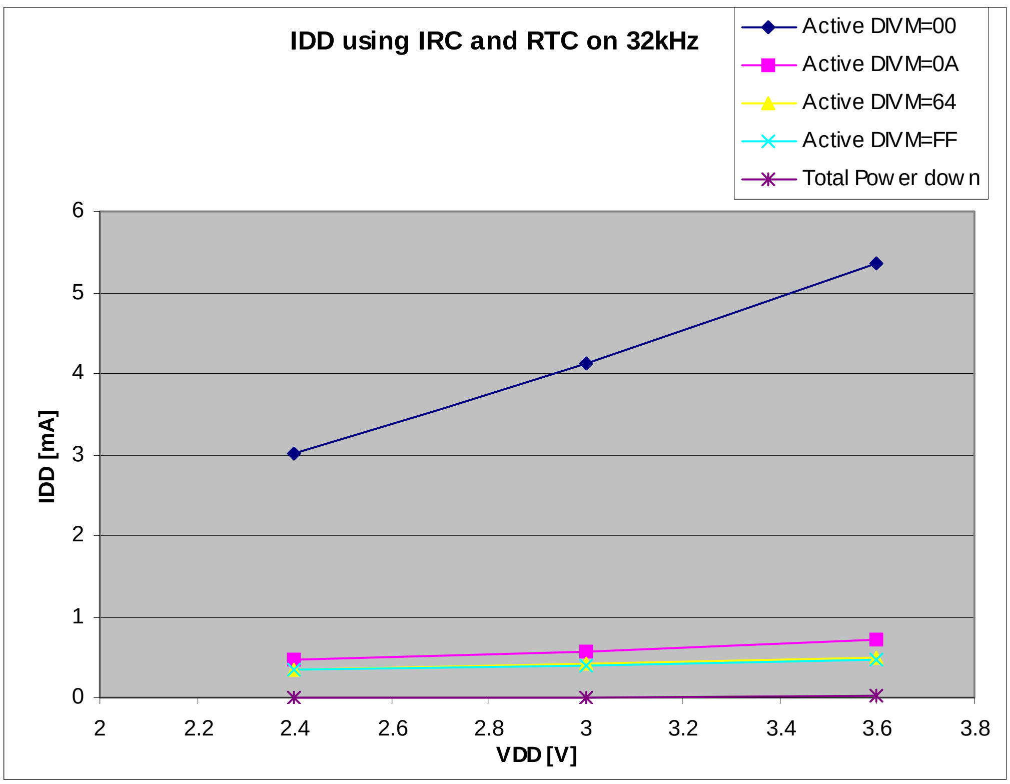

Fig 12. IDD core using Internal RC oscillator RTC enabled using a 32 kHz crystal

4. Summary

In the summary all the power measurement numbers will be put together in tables for each clock source. The power consumption for the different modes can be seen clearly for each clocks source.

4.1 32 kHz crystal

A 32 kHz crystal can be used to get very low power consumption with a very accurate clock source. When an application does not need to execute code or at a slow speed, the power consumption can be even further reduced with power savings modes.

4.1.1 Power consumption with a 32 kHz crystal

Table 14 shows the power consumption in different modes when using a 32 kHz crystal.

Table 14: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	32.768 kHz	73.9 μA	88.1 μA	115 μA
Active DIVM = 0Ah	1.6384 kHz	61.7 μA	67.2 μA	84.8 μA
Active DIVM = 64h	0.16384 kHz	60.3 μA	66.6 μA	83.6 μA
Active DIVM = FFh	0.06 kHz	59.1 μA	66.3 μA	83.1 μA
Idle DIVM = 00h	32.768 kHz	62.7 μA	72.5 μA	90.2 μA
Idle DIVM = 0Ah	1.6384 kHz	57.5 μA	64.8 μA	77.2 μA
Idle DIVM = 64h	0.16384 kHz	56.8 μA	64.1 μA	76.9 μA
Idle DIVM = FFh	0.06 kHz	55.8 μA	64.1 μA	76.2 μA
Power-down	0 Hz	51.9 μA	54.6 μA	58.1 μA
Power-down comp	0 Hz	66.5 μA	69.3 μA	73.2 μA
Total Power-down	0 Hz	1 μA	1 μA	1 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C).

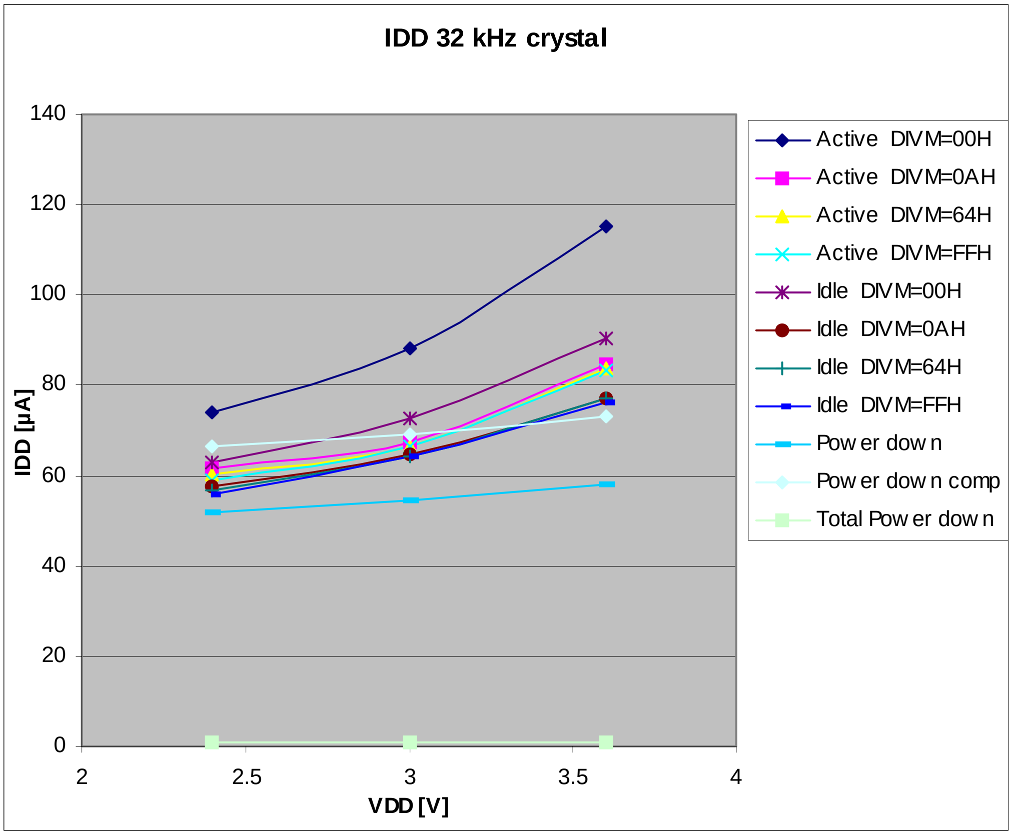

Fig 13. IDD with a 32 kHz crystal

4.1.2 Conclusion

The 32 kHz crystal uses very low power. When using DIVM it makes little difference if the value is 0AH, 64H or FFH. In other words, a 25 times performance increase over DIVM = FF with very similar power numbers.

In Power-down modes having the analog comparators active will have most current consumption, while having the brownout active will be slightly less. For the most power savings, go into total Power-down mode.

4.2 11.059 MHz crystal

A 11.059 MHz crystal can be used to get high performance with a very accurate clock source. Table 15 shows the current consumption when using a 11.059 MHz crystal. When the performance of the 11.059 MHz crystal is not needed different power savings modes can be used.

4.2.1 Power consumption with a 11.059 MHz crystal

Table 15 shows the power consumption in different modes when using a 11.059 MHz crystal.

Table 15: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	11.059 MHz	4560 μA	6780 μA	8830 μA
Active DIVM = 0Ah	553 kHz	850 μA	1410 μA	1700 μA
Active DIVM = 64h	55.3 kHz	670 μA	1150 μA	1350 μA
Active DIVM = FFh	21.7 kHz	650 μA	1140 μA	1350 μA
Idle DIVM = 00h	11.059 MHz	2500 μA	3610 μA	4800 μA
Idle DIVM = 0Ah	553 kHz	710 μA	1090 μA	1450 μA
Idle DIVM = 64h	55.3 kHz	630 μA	930 μA	1280 μA
Idle DIVM = FFh	21.7 kHz	620 μA	920 μA	1270 μA
Power-down	0 Hz	51.9 μA	54.6 μA	58.1 μA
Power-down comp	0 Hz	66.5 μA	69.3 μA	73.2 μA
Total Power-down	0 Hz	1 μA	1 μA	1 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C).

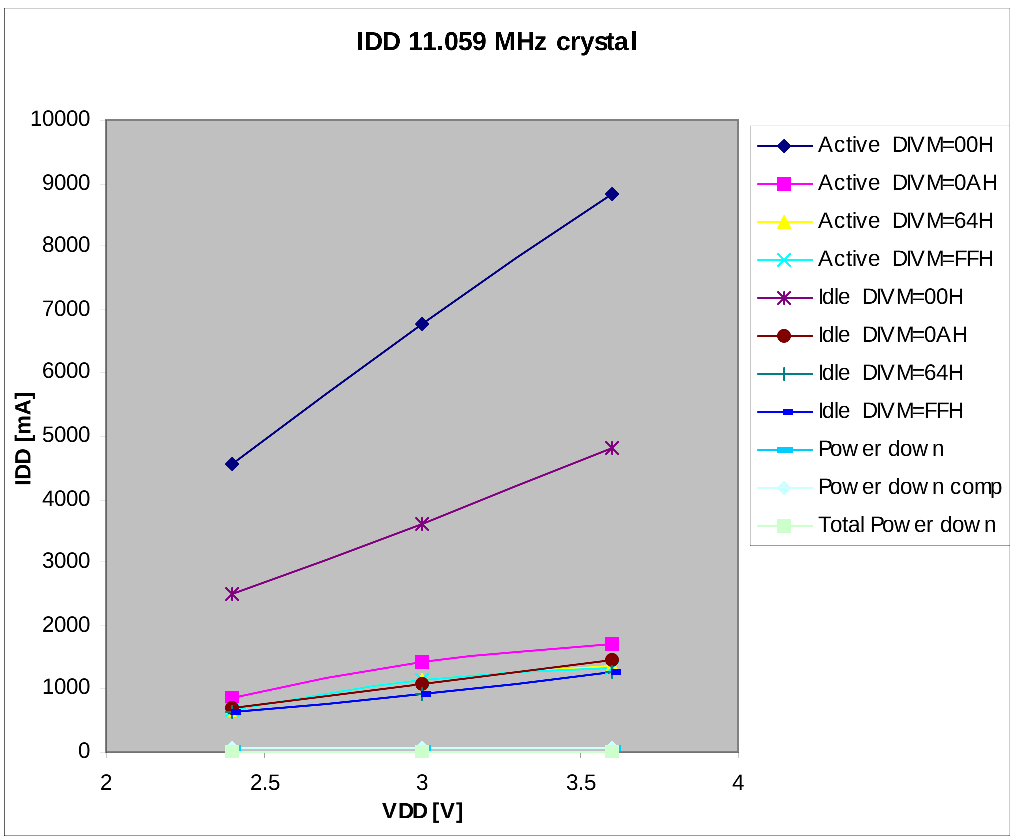

Fig 14. IDD with an 11.059 MHz crystal

4.2.2 Conclusion

The 11.059 MHz crystal has the most performance. When using the DIVM the performance and current consumption goes down. DIVM will be very useful in modes where only low performance is needed. When you are in a routine where you need the maximum performance put the DIVM back to 00h.

For the most power savings go into total Power-down mode. In Power-down mode having the analog comparators active will have most current consumption, while having the brownout active will be slightly less.

4.3 7.373 MHz internal RC oscillator

The internal RC oscillator can be used when both performance and system cost need to be reduced be saving the cost of an external crystal. The ±1 % trimmed internal RC oscillator is not as accurate as an external crystal, but can still be used for UART communications. When the performance of the 7.373 MHz internal RC oscillator is not used different power savings modes can be used.

4.3.1 Power consumption with the 7.373 MHz IRC

Table 16 shows the power consumption in different modes when using the 7.373 MHz internal RC oscillator.

Table 16: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	7.3728 MHz	2970 µA	4000 µA	5300 µA
Active DIVM = 0Ah	369 kHz	430 µA	540 µA	680 µA
Active DIVM = 64h	36.9 kHz	310 µA	380 µA	480 µA
Active DIVM = FFh	14.5 kHz	290 µA	370 µA	440 µA
Idle DIVM = 00h	7.3728 MHz	1540 µA	2120 µA	2800 µA
Idle DIVM = 0Ah	369 kHz	350 µA	440 µA	540 µA
Idle DIVM = 64h	36.9 kHz	290 µA	360 µA	430 µA
Idle DIVM = FFh	14.5 kHz	290 µA	350 µA	430 µA
Power-down	0 Hz	51.9 µA	54.6 µA	58.1 µA
Power-down comp	0 Hz	66.5 µA	69.3 µA	73.2 µA
Total Power-down	0 Hz	1 µA	1 µA	1 µA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C).

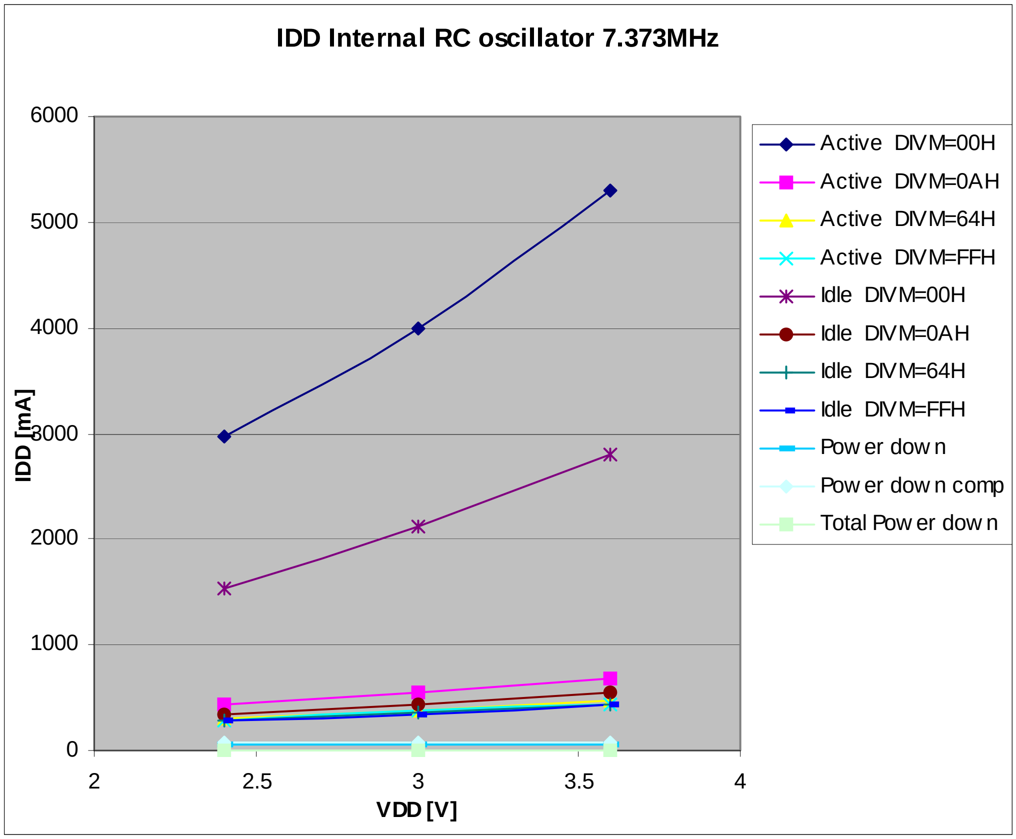

Fig 15. IDD with the 7.3.73 MHz internal RC oscillator

4.3.2 Conclusion

Running at full speed the Internal RC oscillator has high performance. To greatly reduce the power consumption (when this performance is not needed) use DIVM.

In Power-down modes having the analog comparators active will have the most current consumption, while having the brownout active will be slightly less. For the most power savings go into total Power-down mode.

4.4 400 kHz internal watchdog oscillator

The 400 kHz internal watchdog oscillator is a very low power oscillator with a wide tolerance of +20 % –30 %.

4.4.1 Power consumption with a 400 kHz WDT

Table 17 shows the power consumption in different modes when using the internal 400 kHz watchdog oscillator.

Table 17: Current consumption IDD low frequency crystal

Mode\DIVM	fCCLK	IDD at VDD = 2.4 V	IDD at VDD = 3.0 V	IDD at VDD = 3.6 V
Active DIVM = 00h	400 kHz	249.5 μA	333.5 μA	420 μA
Active DIVM = 0Ah	20 kHz	87.1 μA	110.5 μA	166.5 μA
Active DIVM = 64h	2 kHz	85.7 μA	104.9 μA	128 μA
Active DIVM = FFh	0.784 kHz	84.8 μA	103.6 μA	127.2 μA
Idle DIVM = 00h	400 kHz	159.8 μA	202.8 μA	256.8 μA
Idle DIVM = 0Ah	20 kHz	84.7 μA	99.6 μA	117.5 μA
Idle DIVM = 64h	2 kHz	81.1 μA	94.5 μA	110.9 μA
Idle DIVM = FFh	0.784 kHz	80.9 μA	94.2 μA	110.5 μA
Power-down	0 Hz	51.9 μA	54.6 μA	58.1 μA
Power-down comp	0 Hz	66.5 μA	69.3 μA	73.2 μA
Total Power-down	0 Hz	1 μA	1 μA	1 μA

Note: measurements were taken with all peripherals turned off (PCONA = FFh) and at room temperature (T_{amb} = ~25 °C).

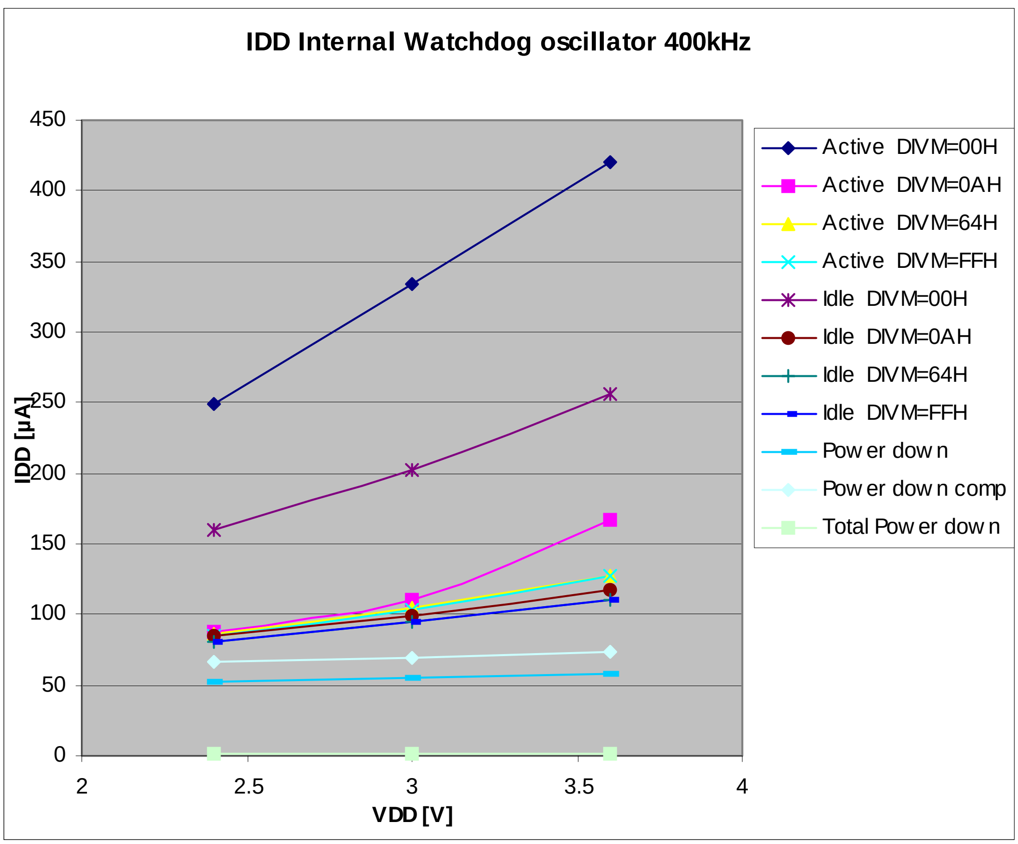

Fig 16. IDD with a 400 kHz internal Watchdog oscillator

4.4.2 Conclusion

The watchdog oscillator consumes very low power. When the DIVM is used it makes little difference with the value is 0AH, 64H or FFH. In other words, a 25 times performance increase over DIVM = FF with very similar power numbers.

In Power-down modes having the analog comparators active will have most current consumption, while having the brownout active will be slightly less. For the most power savings go into total Power-down mode.

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6. Contents

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