APPLICATION NOTE

TDA8020HL/C2
Dual Smart Card Interface

AN10232

Philips
Semiconductors

PHILIPS

Abstract

This application note deals with the dual smart card interface[1] integrated circuit TDA8020HL/C2. The general characteristics are presented and different application examples are described.

[1] It is assumed that the reader of this application note is aware of ISO7816 terminology.

PRELIMINARY APPLICATION NOTE

TDA8020HL/C2
Dual Smart Card Interface

AN10232

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CONTENTS

1 INTRODUCTION

TDA8020HL/C2 is a dual smart card interface device making the electrical interface between a microcontroller and two smart cards. This device supports mainly asynchronous smart cards (microcontroller based IC cards).
The electrical characteristics of TDA8020C2 are in accordance with ISO7816-3 and EMV 2000 (Europay, Mastercard, Visa) normalisation.

TDA8020C2 can be used in various applications such as pay TV, point of sales terminals (P.O.S.), and a lot of conditional access applications (i.e. internet...), and also for Security Access Modules (S.A.M.) in banking applications. As it is a device working under a low voltage power supply, it can also be used in portable applications like electronic purse readers or wallets.

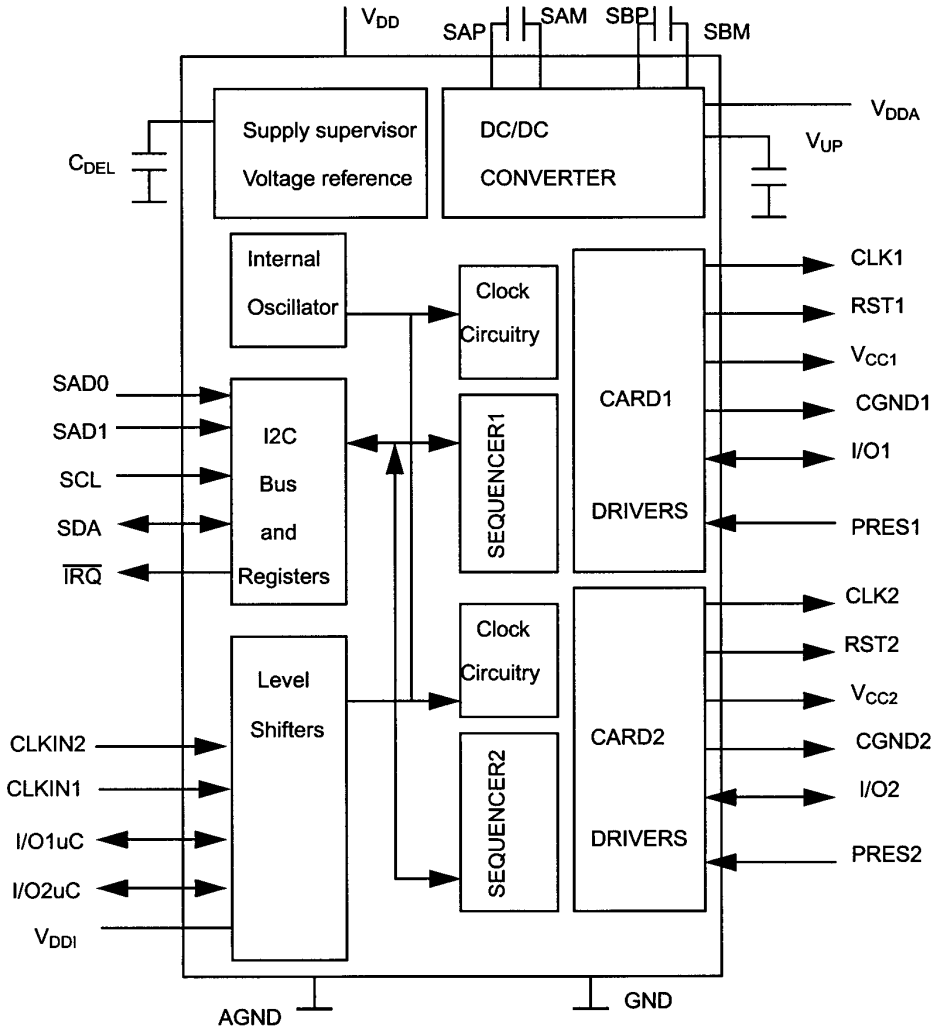
This device does not support smart cards with a programming voltage (VPP) greater than 5 V, because new generations of IC cards do not need such a feature (EEPROM based smart cards).

1.1 Main features

- Two independent smart card interfaces according to ISO 7816-3 and EMV 2000,
- VCC1 and VCC2 regulation 5 V or 3 V +/-5% up to 60mA,
- Asynchronous cards supported,
- Card take-off protection,
- Two protected and buffered pseudo-bidirectional I/O lines (I/Ox referenced to VCCx and I/OxUC referenced to VDDI),
- Clock generation (up to 10 MHz on the smart card side) with synchronous start and frequency doubling,
- Clock STOP LOW, clock STOP HIGH for cards power down mode,
- Automatic activation and deactivation sequences through two independent sequencers,
- Automatic processing of the RST contact with count of the 42 100 CLK cycles for begin of the ATR,
- Warm reset command,
- Supply voltage supervisor for power-on reset, spikes killing and emergency deactivation in case of supply drop-out, overconsumption or overheating (2.5 < VDD < 6.5 V),
- Current limitation in case of short circuit on each CLK, RST, I/O and VCC contacts,
- Integrated step-up converter (doubler, tripler or follower) allowing operation in a 3 or 5 V environment (2.5 < VDDA < 6.5 V),
- Enhanced ESD protections on each smart card side (6 kV minimum),
- Power down mode with current reduction,
- Control from a microcontroller via a 400 kHz slave I2C bus,
- Four parallel devices possible due to 2 sub-address wires,
- Interface signals supplied by an independent voltage (1.5 < VDDI < 6.5 V).

This device is proposed in package LQFP32 (SOT 358-1).

The block diagram of this circuit is presented on the next figure and all the internal blocks will be described in the coming paragraphs.



Block diagram

1.2 I2C interface

The I2C bus interface is used to:

- initiate an automatic activation or a deactivation sequence,
- select the card supply voltage (3V or 5V),
- initiate a warm reset,
- configure the clock card in active mode (CLKIN, CLKIN/2, CLKIN/4 or CLKIN/8) or in power down mode (STOP LOW or STOP HIGH),
- select or deselect the power down mode,
- read the status (card present or not, hardware problem detected, unresponsive card after activation, supply drop-out detected by the voltage supervisor, card powered or not...),
- configure I/OUC and I/O in high-impedance (refer to paragraph 2.6 page 15).

The TDA8020C2 command is structured as follows:

Symbol	Bit	Description
START/STOPN	0	"1" activation sequence initiated "0" deactivation sequence initiated
WARM	1	"1" warm reset procedure initiated (automatically reset by hardware after processing)
3V/5VN	2	"1" VCC = 3 V "0" VCC = 5 V
PDOWN	3	"1" power down mode (CLK frequency defined by CLKPD bit) "0" normal mode
CLKPD	4	"1" CLK STOP LOW "0" CLK STOP HIGH
CLKSEL1	5	CLKSEL1 and CLKSEL2 determine the CLK frequency applied to the card in normal mode
CLKSEL2	6	(*)
I/OEN	7	"1" I/OUC = I/O line "0" I/OUC and I/O high impedance

(*) CLK card in normal mode with CLKSEL1 and CLKSEL2 bits:

CLKSEL2	CLKSEL1	CLK
0	0	CLKIN/8
0	1	CLKIN/4
1	0	CLKIN/2
1	1	CLKIN

The TDA8020C2 status is structured as follows:

Symbol	Bit	Description
PRES	0	"1" card present "0" card absent
PRESL	1	"1" card inserted or extracted (*)
I/O	2	"1" I/O line high level "0" I/O line low level
SUPL	3	"1" supervisor has signalled a fault (*)
PROT	4	"1" overload or overheating during a session
MUTE	5	"1" no ATR after 2 x 42 100 CLK cycles (*)
EARLY	6	"1" ATR between 200 and 370 CLK cycles when RST is low level or ATR between 0 and 370 CLK cycles when RST is high level (*)
ACTIVE	7	"1" card powered "0" card not powered

(*) In these cases, IRQN is pulled low. When the system controller reads out the status register, these bits are reset and IRQN is pulled high.

During a card session, an emergency deactivation is performed in the following situations:

- insertion or extraction card,
- supply dropout,
- short circuits between VCC and others contacts.

Note:
When a card has not answered its ATR (bit MUTE set to logic 1 and IRQN signal set to low level), it is not possible to initiate a warm reset unless a read status operation has been performed.

The bus has 2 addresses, one for each card. So 4 devices may be used in parallel due to the address selections pins SAD0 and SAD1:

Card1 address	Card2 address	SAD1	SAD0
40H	48H	0	0
42H	4AH	0	1
44H	4CH	1	0
46H	4EH	1	1

These addresses are set by hardware (0 means connected to ground and 1 means connected to VDDI).

Example:

SAD0 and SAD1 are connected to GND, thus:

- 40H is the address for writing a command to card 1,
- 41H is the address for reading card 1status,
- 48H is the address for writing a command to card 2,
- 49H is the address for reading card 2 status.

2 BLOCK OVERVIEW

2.1 Power supply and voltage supervisor

The power supply pins are VDD and GND. VDD shall be in the range of 2.5 to 6.5 V. This pin needs a close decoupling 10 µF capacitor.
At power on, the logic is held in reset state until VDD reaches the voltage supervisor threshold V_{th1} (2.25 V typical value).
A voltage supervisor is integrated in order to secure the smart card if the power supply drops below the threshold voltage.
In case of voltage drop, the voltage supervisor delivers a reset pulse (typically tw width = 10 ms if a 22 nF capacitor is connected to CDEL) and a deactivation sequence is initiated if a smart card is powered. During this reset pulse, IRQN line is low level and the I2C bus is unresponsive to any bus access. When TDA8020C2 becomes operational, IRQN goes high and SUPL bit is set.
All the interface signals (CLKIN1, CLKIN2, SAD1, SAD0, IRQN, I/O1UC and I/O2UC) are referenced to VDDI, in the range of 1.5 V to VDD. Consequently TDA8020C2 can be driven by low voltage integrated circuits, which is convenient for portable or low power applications.
The pins SCL and SDA can be referenced to a voltage higher than VDD, which is convenient when others connected I2C peripherals cannot operate at VDDI.

2.2 Step-up converter

The step-up converter is intended to deliver a regulated +5 V or +3 V (according to 3V/5VN bit) on the VCC pin, when the card is activated whatever the supply voltage VDDA is.
The step-up converter pins are VDDA and AGND. The specific supply voltage VDDA shall be within the range of 2.5 to 6.5 V and needs a close decoupling 33 µF capacitor.
Depending on VDD supply voltage and VCC, an automatic step-up configuration (doubler, tripler or follower) is made on the step-up converter in order to optimise the current efficiency of this converter. It is working with an internal oscillator running at 2.5 MHz and needs three external capacitors in order to operate properly. A 220 nF capacitor is necessary between pins SAP and SAM, between SBP and SBM and an other 220 nF capacitor is needed between pin VUP and AGND.
These capacitors shall be placed as close as possible to the pins of the integrated circuit.

2.3 Clock circuitry

The clock signal CLK1 applied to the smart card 1 comes from the CLKIN1 signal and the clock signal CLK2 applied to the smart card 2 comes from the CLKIN2 signal.

During a card session, according to CLKSEL1 and CLKSEL2 bits, CLK can be equal to CLKIN/8 or CLKIN/4 or CLKIN/2 or CLKIN.
But also during a card session, according to CLKPD and PDOWN bits, CLK can be either equal to STOP LOW or STOP HIGH.

A special circuitry has been built so that any frequency change on CLK during a session is made without any spurious pulses as mentioned in the ISO7816-3 normalisation.

During CLK changes between CLKIN, CLKIN/2, CLKIN/4, CLKIN/8, STOPH and STOPL, the first and last pulses around the place of the change have the correct duty cycle.

The duty cycle of the CLK signal is in the range 45%, 55% of the period during stable operation, except with the CLK equal to CLKIN configuration. In this case, the CLKIN signal duty cycle is setting the CLK signal duty cycle.
Rise and fall times of the CLK signal are 8 ns maximum which allows to be fully compliant with the EMV 2000 specification with a maximum value of 10 MHz on CLK signal (tr, tf < 8% of the period).

2.4 VCC generation

The output pin VCC1 is used to supply VCC1 to the smart card 1 and the output pin VCC2 is used to supply VCC2 to the smart card 2.
For an average current of less than 65 mA, the active level of VCC is in the range of 4.75 V / 5.25 V for a 5V card and 2.8 V / 3.2 V for a 3V card.
In case of current pulses (dynamic loads) VCC remains between 4.6 and 5.4 V for a maximum load of 40 nAs for a 5 V card and between 2.76 and 3.24 V for a maximum load of 24 nAs for a 3 V card.
When VCC is shorted to ground, ICC is limited to 100 mA and if during normal operation ICC exceeds 90 mA (overload detection), an automatic deactivation is performed.

If VDD > 3 V, when VCC1 = VCC2 = 5 V, ICC1 + ICC2 $\leq$ 120 mA (2*60 mA).
If VDD > 3 V, when VCC1 = VCC2 = 3 V, ICC1 + ICC2 $\leq$ 110 mA (2*55 mA).
If 2,7 V < VDD < 3 V, when VCC1 = VCC2 = 3 V or 5 V, ICC1 + ICC2 $\leq$ 80 mA.

The slew rate of VCC for 5V card at power on is 0.14 V/µs and 0.09 V/µs for 3V card.
Two decoupling capacitors of 100 nF are necessary on each VCC pin; one shall be placed close to the VCC pin of the integrated circuit and the other shall be placed as close as possible to the VCC contact of the smart card socket.

2.5 Logic circuitry

The logic block is built with a sequencer that enables or disables the different signals whatever the circuit mode is. It manages all the activation and deactivation phases.

2.5.1 Power down mode

This is a reduced consumption mode when the card is activated.
In this mode, all control functions as well as the voltage supervisor are active and the card is said to be in sleep mode. The frequency defined by CLKPD bit is applied on CLK pin.
To enter into this mode, first set the CLKPD bit to the desired value, then the PDOWN bit.
The lowest consumption is reached with CLKIN connected to GND or VDDI and CLK = STOP LOW or STOP HIGH.

2.5.2 Activation sequence

An activation sequence is initiated by setting the START/STOPN bit to logic 1.
The internal sequencer drives the following sequence:

1. Step-up converter starts.
2. VCC rises from 0 to +5 V or from 0 to +3 V (according to 3V/5VN bit).
3. I/O is enabled.
4. CLK is sent.
5. RST is enabled.

Just after CLK is started with RST low, the clock counter counts the CLK cycles until a start bit is detected on I/O line.

- If a start bit is detected during the 200 first CLK cycles, it is not transmitted on the I/OUC line.
- If a start bit is detected between 200 and 42 100 CLK cycles, the IRQN line is pulled low and both the EARLY and MUTE status bits are set. It is up to the system controller to initiate a deactivation sequence (if desired) to reject the card. RST signal will remain low.
- After 42 100 CLK cycles, if no start bit has been detected, the sequencer toggles RST to high, and counts 42 100 CLK cycles again.
- If a start bit is detected between 0 and 370 CLK cycles, the IRQN line is pulled low and the EARLY status bit is set.
- Then, if no start bit has been detected, the IRQN line is pulled low and the MUTE status bit is set.
- But if a start bit has been detected during one of the two 42 100 CLK cycles slots, the counter is stopped, RST is kept without changes and the card session goes on.

The activation sequence is completed in 135 µs maximum.

2.5.3 Deactivation sequence

When a communication is completed, the host microcontroller sets the START/STOPN bit to logic 0 and the circuit starts an automatic deactivation sequence:

1. RST goes to low level.
2. CLK is stopped.
3. I/O is set to low level.
4. VCC falls to low level.
5. Step-up converter stops and CLK, RST, VCC and I/O are set to low impedance to GND.

This deactivation sequence is completed in 110 µs maximum.

2.5.4 Protections

The following fault conditions are monitored by the circuit:

- short circuit or current overload on VCC,
- card removal during a transaction,
- overheating problem,
- supply voltage (VDD) dropping.

When one of these conditions occurs, the circuit pulls the IRQN line to low level, in order to warn the microcontroller, and a deactivation sequence is automatically processed.

According to EMV 2000 and GIE Carte Bancaire specifications, the current on each smart card signal is limited to the following value:

VCC	90 mA
I/O	+/- 10mA
RST	+/- 20 mA
CLK	+/- 70 mA

2.5.5 Presence detection

The PRES contact is giving the card presence information when it is connected to the switch of the card reader socket. This information is then given to the host controller by the means of the status bits PRES and PRESL.

2.6 I/O, I/OUC lines

On TDA8020C2, two I/O lines are available (I/O1, I/O2) and are referenced to VCC (VCC1, VCC2) whereas I/OUC (I/O1UC, I/O2UC) are referenced to VDDI. Consequently operation with VCC < > VDD < > VDDI is allowed.
When I/OEN bit is set to logic 1, the data transmission between I/O and I/OUC is enabled, whereas set to logic 0, I/O and I/OUC lines are independent.
The I/OUC lines can be driven separately from the system controller (and both I/OEN bits are set to logic 1) or driven by the same signal and tied together (and each bit is set or reset according to the addressed card).

3 PINNING AND PIN FUNCTION OF TDA8020C2

TDA8020C2 is available in LQFP32 package.

The following table gives the pin function:

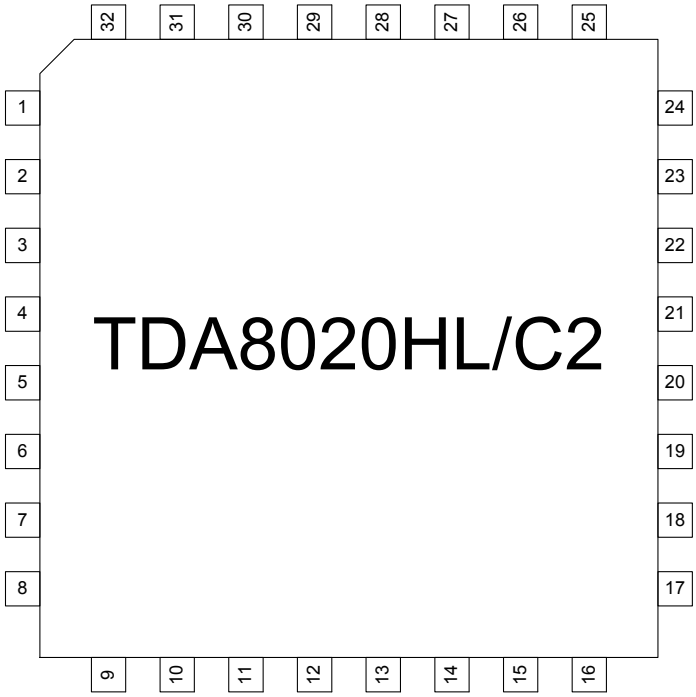
PIN TDA8020C2	SYMBOL	DESCRIPTION
1	PRES1	Card1 presence contact (Active High)
2	CGND1	Ground for card1 (C5 contact)
3	CLK1	Clock output to card1 (C3 contact)
4	VCC1	Card1 supply voltage (C1 contact) (1)
5	RST1	Reset output to card1 (C2 contact)
6	I/O2	Data line from/to card2 (C7 contact) (2)
7	PRES2	Card2 presence contact (Active High)
8	CGND2	Ground for card2 (C5 contact)
9	CLK2	Clock output to card2 (C3 contact)
10	VCC2	Card2 supply voltage (C1 contact) (3)
11	RST2	Reset output to card2 (C2 contact)
12	GND	Ground
13	VUP	Output for DC/DC converter (connected to AGND via 220 nF)
14	SAP	Capacitance for DC/DC converter (connected to SAM via 220 nF)
15	SBP	Capacitance for DC/DC converter (connected to SBM via 220 nF)
16	VDDA	Supply voltage for DC/DC converter
17	SBM	Capacitance for DC/DC converter (connected to SBP via 220 nF)
18	AGND	Ground for DC/DC converter
19	SAM	Capacitance for DC/DC converter (connected to SAP via 220 nF)
20	VDD	Supply voltage
21	SCL	I2C serial clock (4)
22	SDA	I2C serial data (4)
23	SAD0	I2C slave address selection
24	SAD1	I2C slave address selection
25	IRQN	Output interrupt (Active Low) (4)
26	CLKIN1	External clock input for card 1
27	I/O1UC	Data line from/to the system controller (5)
28	I/O2UC	Data line from/to the system controller (6)
29	CLKIN2	External clock input for card 2
30	CDEL	Capacitance for the delay on voltage supervisor
31	VDDI	Supply voltage for the interface signals with the system
32	I/O1	Data line from/to card1 (C7 contact) (7)

Notes:

(1) : decoupling 2 x 100 nF to CGND1 mandatory
(2) : integrated 14K pull-up to VCC2 for I/O2 pin
(3) : decoupling 2 x 100 nF to CGND2 mandatory
(4) : open drain

(5) : integrated 11K pull-up to VDD for I/O1UC pin
(6) : integrated 11K pull-up to VDD for I/O2UC pin
(7) : integrated 14K pull-up to VCC1 for I/O1 pin

Figure 1 presents the pinning of TDA8020HL/C2.



4 SMART CARD INTERFACE APPLICATION

4.1 Introduction

The main applications for TDA8020C2 are pay TV (multi-standards Conditional Access Systems), multipurpose card readers such as in banking applications (S.A.M. interfaces), PC terminals, and also portable applications such as electronic purse.
Different application examples are given in the coming paragraphs.

4.2 External components

The basic external components for TDA8020C2 are:

- a 220 nF capacitor on VUP,
- a 220 nF capacitor between SAP and SAM,
- a 220 nF capacitor between SBP and SBM,
- a 22 nF capacitor on CDEL,
- 2 x 100 nF capacitors on each VCC: one close to pin VCC, the other close to the VCC contact of the card reader socket,
- 2 decoupling capacitors: a 100 nF plus a 33 µF (polarised) between VDDA and AGND,
- 2 decoupling capacitors: a 100 nF plus a 10 µF (polarised) between VDD and GND,
- 2 decoupling capacitors: a 100 nF plus a 10 µF (polarised) between VDDI and GND.

Always use low ESR capacitors (< 100 mR) for these pins.

For layout considerations, the decoupling capacitors on VDD must be as close as possible to VDD pin and the other capacitors (on VUP, SAP, SAM, SBP, SBM, CDEL, VDDI) must be as close as possible to the IC pins.

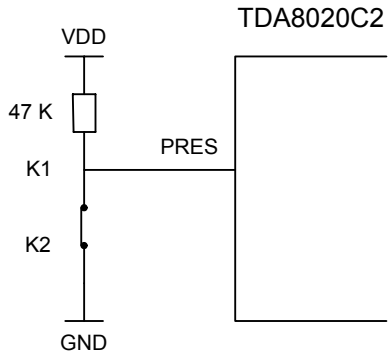
For layout considerations, it is highly recommended:

- **to keep track C3 (CLK card contact) as far as possible from other tracks,**
- **to have straight connection between each CGND and C5 (GND card contact).**
- **The 2 capacitors on C1 (VCC card contact) should be connected to this ground track.**
- **to avoid ground loops between CGND1, CGND2, AGND and GND,**
- **to decouple VDD and VDDA separately; if the 2 supplies are the same in the application, then they should be connected in star on the main track.**

4.3 Presence switch implementation

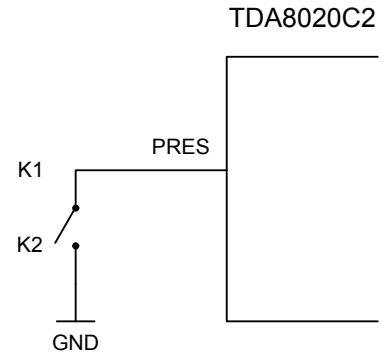
4.3.1 Using Normally Closed card detection switch

When the card is inserted, the switch between K1 and K2 is opened (and when the card is absent, this switch is closed)



4.3.2 Using Normally Open card detection switch

When the card is inserted, the switch between K1 and K2 is closed (and when the card is absent, this switch is opened)



4.4 Activation of TDA8020C2

4.4.1 Asynchronous application

4.4.1.1 Activation sequence

An activation is possible only if a smart card is present.
Figure 2 shows this activation phase:

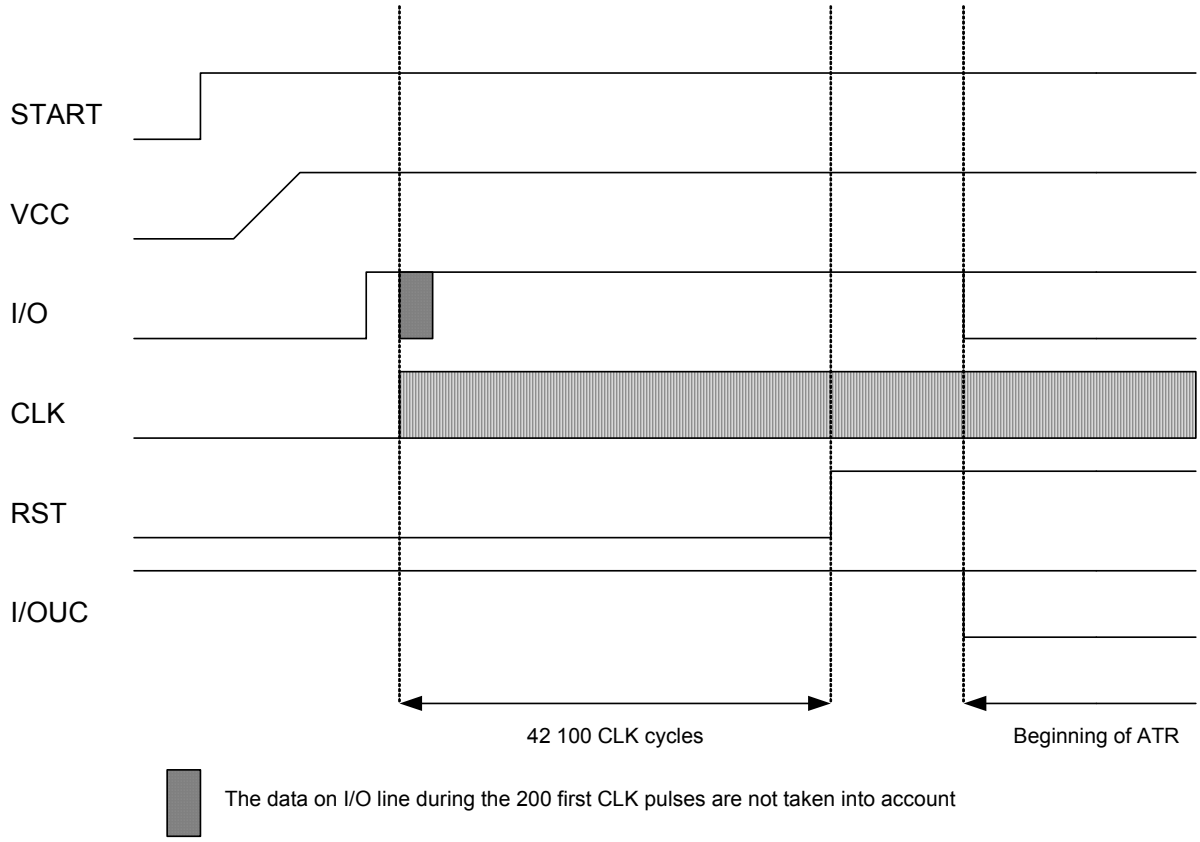


Figure 2

4.4.1.2 Deactivation sequence

Figure 3 shows this deactivation phase:

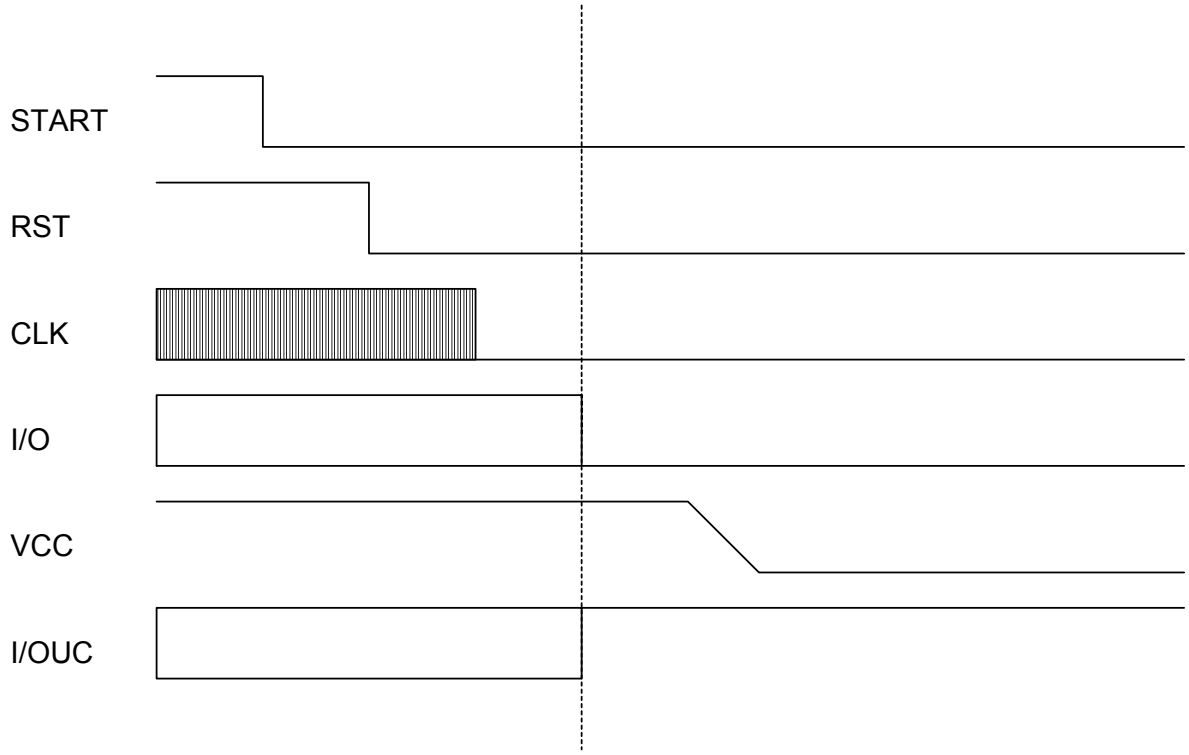


Figure 3

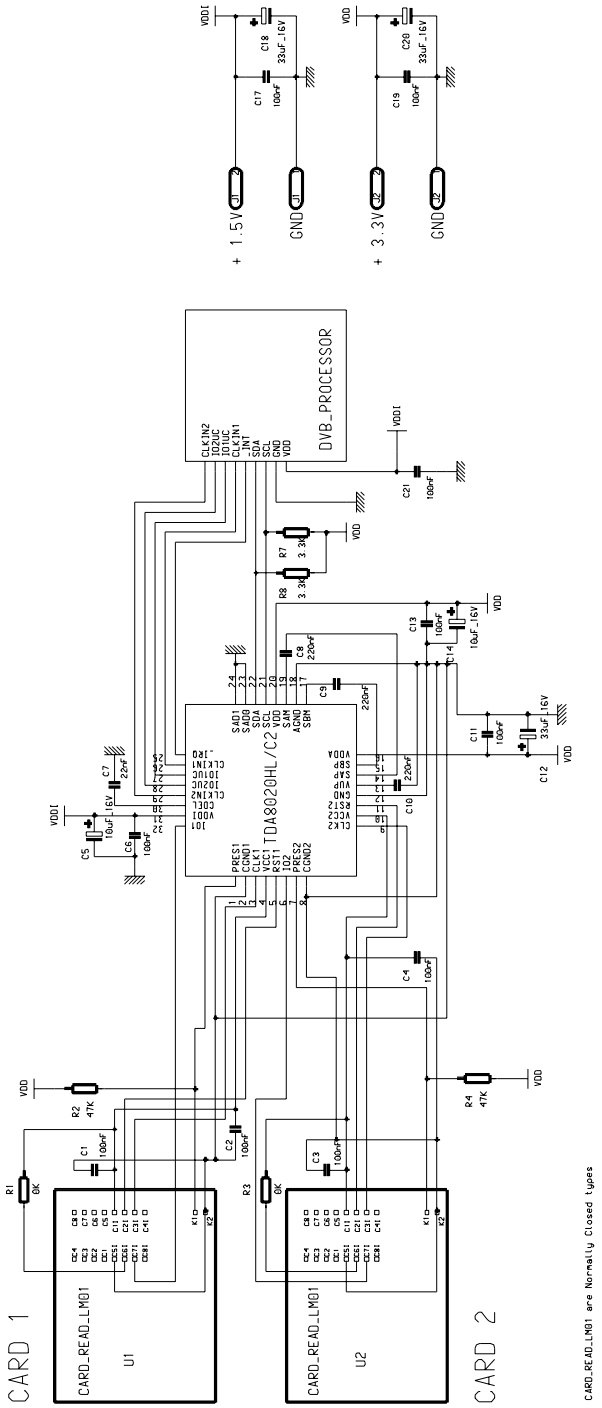
4.5 Application examples

The TDA8020C2 requires only five interface signals to be connected to a microcontroller: SCL, SDA, IRQN, I/O1UC and I/O2UC.

4.5.1 Standard asynchronous application with a DVB processor

In this application, the DVB processor has two CLKIN pins (CLKIN1 and CLKIN2). So two cards working at a different clock frequency can be used at the same time.
Both TDA8020C2 I/OUC lines are connected to two external interrupts IO1UC and IO2UC in order to send or to receive data to/from the smart card. In this case, before an APDU command is sent to a card, both I/OEN bits are set to logic 1.

The I2C bus is controlled from the DVB processor either by hardware or by software through SCL and SDA pins. IRQN line is connected to an external interrupt (INTN). Each time IRQN goes to low level, the DVB processor reads the 2 TDA8020C2 status cards, and reacts accordingly to the happening event (card insertion, card extraction, short circuit, …).

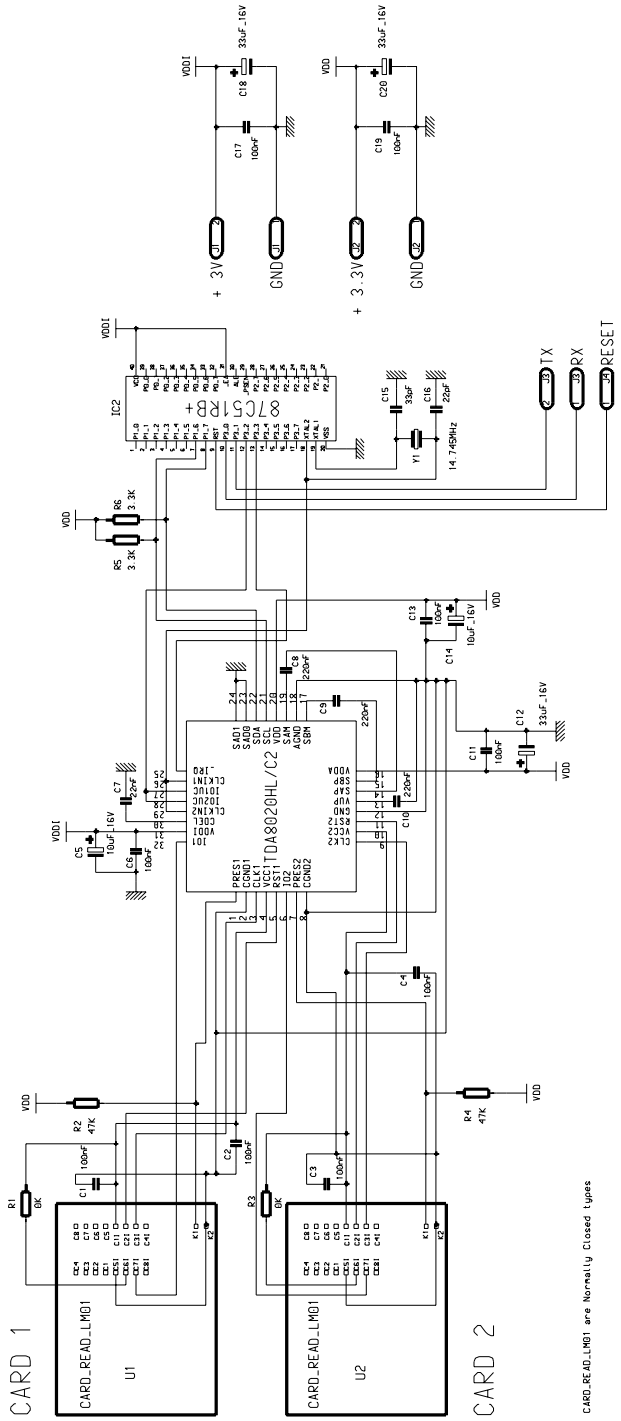

VDD1
VDD
+ 1.5V
GND
+ 3.3V
GND
DVB_PROCESSOR
TDA8020HL/C2
CARD_READ_LM01
U1
U2
CARD 1
CARD 2
CARD_READ_LM01 are Normally Closed types

4.5.2 Standard asynchronous application with a 8XC51 microcontroller

A standard asynchronous application example is given next page:
87C51RB+ is an 8-bit CMOS (low voltage, low power and high speed) microcontroller, with power supply voltage comprised between 2.7 V and 5.5 V.
The I2C bus is controlled by software through P1.6 (SCL) and P1.7 (SDA) pins. IRQN line is connected to external interrupt P3.3 (INT1). Each time IRQN goes to low level, the 87C51RB+ reads the 2 TDA8020C2 status cards, and reacts accordingly to the happening event.
Both I/OUC lines (I/O1UC and I/O2UC) are connected to external interrupt P3.2 (INT0) in order to send or to receive data to/from the smart card. In this case, before an APDU command is sent to card 1, card 1 I/OEN bit is set to logic 1 and card 2 I/OEN bit is set to logic 0.

CLKIN1 and CLKIN2 are connected together and driven from the same signal (XTAL2).

In all these applications, any asynchronous protocol (T=0, T=1) can be used because TDA8020C2 is protocol transparent on the I/O lines. The protocol management is made by software in the system controller.


TDA8020HL/C2
CARD_READ_LM01
CARD 1
CARD 2
U1
U2
IC2
VDD
+ 3V
GND
+ 3.3V
TX
RX
RESET
CARD_READ_LM01 are Normally Closed types

4.5.3 Application with security modules

Some applications, such as banking applications, require that a smart card having some security features concerning the application, is permanently inserted in the smart card reader. These Security Access Modules (S.A.M.) are characterising both the application and the terminal. Depending on the number of applications that is supported by the terminal, there can be more than one S.A.M. in the terminal.
For each type of payment operator (e.g. GIE CB), the terminal has a specific security module in order to validate the transactions.

4.5.3.1 Sextuple smart card reader with TDA8008HL/C2

The TDA8008HL/C2 is a one chip dual smart card coupler with embedded microcontroller and ISO7816 UART suitable for asynchronous and synchronous smart cards.
Its main features are:

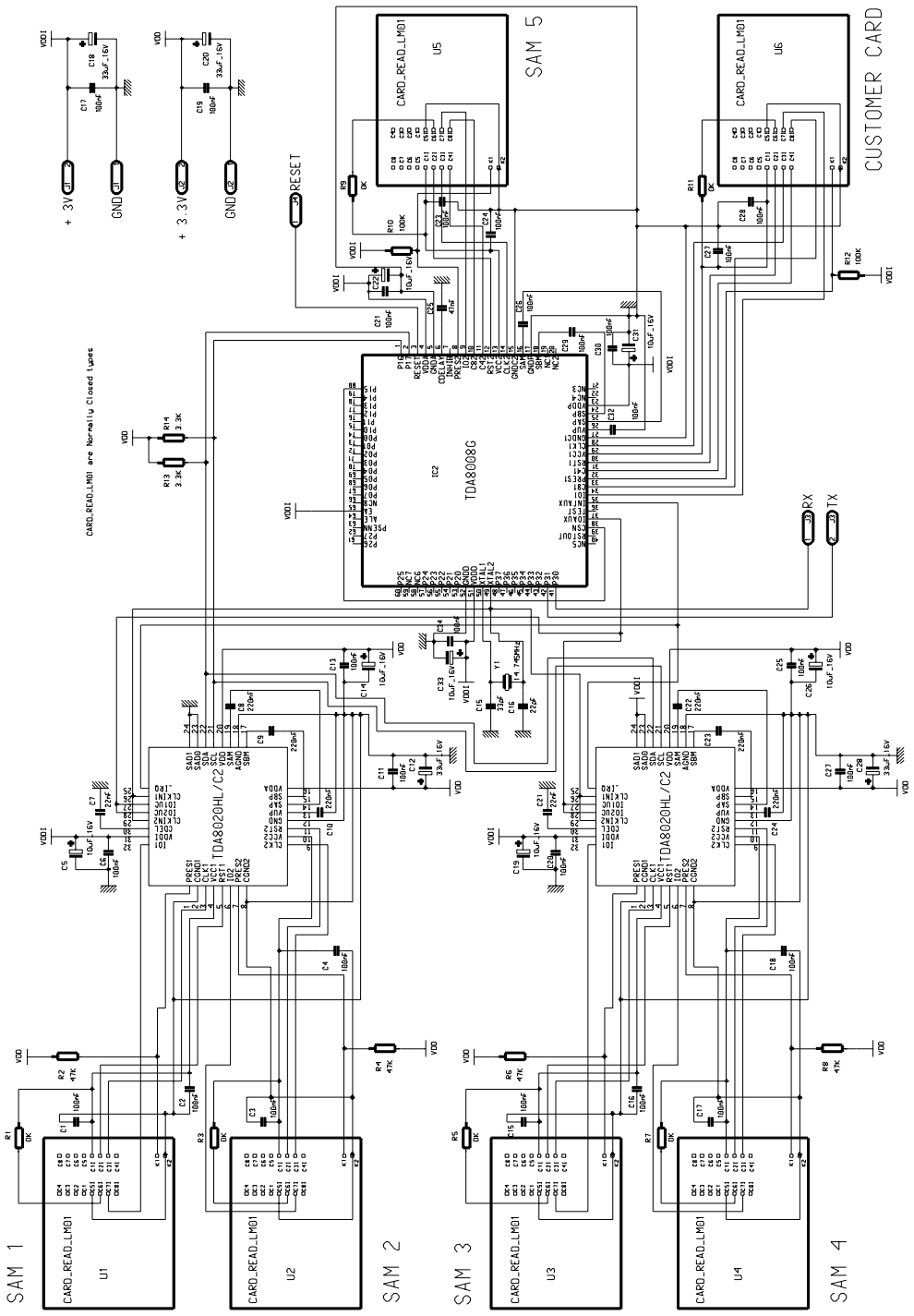
- 8XC51 microcontroller core with 16 kbytes ROM and 256 bytes RAM,
- 512 bytes AUXRAM,
- ISO7816 UART supporting asynchronous protocols T=0 and T=1.

In this application, there are six smart card interfaces: one for the customer card, the others for the security modules.
The customer card, which can be synchronous or asynchronous and can work at high baud rate with either T=0 or T=1 protocol, is handled by TDA8008HL/C2.
The 5 security modules are supplied by the means of 2 TDA8020C2 plus the TDA8008C2 second slot supporting asynchronous cards.

This application is shown on the next page. Both the security and the protocol management are made by TDA8008C2 which can communicate with the host system in charge of the application layer, via a serial interface.

The I2C bus is controlled by software through P1.6 (SCL) and P1.7 (SDA) pins. The 2 IRQN lines are connected to external interrupt INTAUX. Each time IRQN goes to low level, TDA8008C2 reads the 4 TDA8020C2 status cards, and reacts accordingly to the happening event.
The 4 I/OUC lines are connected to external interrupt IOAUX in order to send or to receive data to/from the smart card. In this case, before an APDU command is sent to S.A.M. 1, S.A.M. 1 I/OEN bit is set to logic 1 and S.A.M. 2, S.A.M. 3 and S.A.M. 4 I/OEN bits are set to logic 0.

CLKIN1, CLKIN2, CLKIN3 and CLKIN4 are connected together and driven from the same signal (XTAL2).


CUSTOMER CARD
SAM 1
SAM 2
SAM 3
SAM 4
SAM 5
CARD_READ_LM01
TDA8020HL/C2
TDA8008C
CARD_READ_LM01 are Normally Closed types
RESET
RX
TX
+ 3V
GND
+ 3.3V
GND

5 CONCLUSION

TDA8020HL/C2 is a complete analogue dual smart card interface that complies with ISO7816-3 and EMV 2000 requirements. It is very suitable for many applications (set top boxes, internet terminals and banking applications (S.A.M. interfaces)) and requires few external components but also few microcontroller interface signals.